A CMOS-Compatible Rapid Vapor-Phase Doping Process for CMOS Scaling

Takashi Uchino, *Member, IEEE*, Peter Ashburn, *Member, IEEE*, Yukihiro Kiyota, and Takeo Shiba, *Member, IEEE*

***Abstract*—An advanced CMOS process, which used rapid vapor-phase doping (RVD) for pMOSFETs and solid-phase diffusion (SPD) for nMOSFETs, has been developed. Using the RVD technique, a 40-nm-deep p-type extension with a sheet resistance as low as 400 Ω/sq has been realized. These RVD and SPD devices demonstrate excellent short-channel characteristics down to 0.1 μm channel length and 40% higher drain current, compared with conventional devices with ion implanted source/drain (S/D) extensions, and high-speed circuit performance. We investigate the effect of the S/D extension structure on the device performance and find that a gate extension overlap of 25 nm enables excellent dc and high-speed circuit performance in 0.1-μm devices.**

***Index Terms*—CMOS process, doping, junction, MOSFET.**

I. Introduction

HE KEY subject in the scaling of nanometer-regime CMOS devices is how to improve device performance without any degradation such as short-channel effects and high power consumption. Achieving high performance, however, is becoming increasingly difficult because of the tradeoff between good short-channel characteristics and high current drivability [1]. Moreover, conventional low-energy ion implantation for the shallow source/drain (S/D) extension formation induces high resistance because it degrades carrier activation efficiency, results in only a low carrier concentration at the surface, and reduces the gate-extension overlap [2]. Furthermore, the transient enhanced diffusion (TED) and the channeling effect create difficulties in the forming of the shallow junction. Thus, techniques to form shallow, abrupt, and low-resistance junctions are required to enable further progress. To overcome these problems, thermal doping technologies such as rapid vapor-phase doping (RVD) [3] or solid-phase diffusion (SPD) from phosphosilicate glass (PSG) [4] have been investigated. These technologies are considered to be appropriate for creating shallow junctions in the regime between 20 and 40 nm [5]. However, there are some primary problems of integrating these processes into a CMOS process, because the diffusion source material for one dopant type must be removed prior to formation of the diffusion source material for the second dopant type.

We have developed an advanced CMOS process that meets these needs and does not require ion implantation to form shallow S/D extensions. The fabricated devices use a combination of RVD and SPD, and show a high on-current and excellent threshold voltage rolloff characteristics down to an effective channel length of 0.1 μm. The high performance of the devices is due to the shallow and abrupt diffused S/D extensions. The RVD technique was applied to pMOSFET formation, because the requirement of shallow junction formation for pMOSFETs is more serious than that for nMOSFETs. To confirm the effect of the lateral diffusion on the device performance, SPD was applied to nMOSFET formation. In this paper, we present the device design to obtain high drain on-current. To improve the device performance, the S/D extension structure is investigated, and a CMOS-compatible RVD process is presented. Finally, the device structure for 0.1-μm CMOS devices is optimized to give the best combination of dc and circuit performance.

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II. Fabrication Process

A. Ultrashallow Junction Formation

Two key techniques were used to obtain shallow and abrupt junctions with low extension resistance. The first is RVD for pMOSFETs. This is a form of gas-source diffusion using rapid thermal annealing (RTA), and it enables the formation of shallow and heavily doped abrupt junctions. The RVD was done using hydrogen and B_2H_6 gas around 900 °C for a short time up to 40 s. Hydrogen gas is used to keep the substrate surface clean and reduce boron segregation. Hydrogen gas plays an important role in terminating the dangling bonds and reducing the excessive boron adsorption. These evidences were obtained by using x-ray photoelectron spectroscopy (XPS) and Fourier-transform infrared-attenuated total reflection (FTIR-ATR) [6]. A SIMS profile of an RVD S/D extension is shown in Fig. 1 and compared to a BF_2^+ implanted extension. The RVD extension is less than 30-nm-deep and its abruptness is 3.6 nm/dec. On the contrary, TED and boron channeling were observed in the ion-implanted sample and the tail extends to a depth of 100 nm. The surface doping concentration of the RVD sample is more than 10 times higher than that of the ion-implanted sample. Here, the junction depth was defined as the point at which the doping concentration was equal to 1×10^{18} cm^{-3}.

The second technique is SPD from PSG layers for nMOSFETs. The SPD was done at 1000 °C for 10 s. The SIMS profile of the SPD extension shows a shallow junction with only a small tail, and a junction depth of less than 50 nm (Fig. 2). Like the RVD sample, the SPD sample has its highest carrier concentration at the surface. Some experiments of the n-type shallow junction formation using PH_3 have been done before [7], [8].

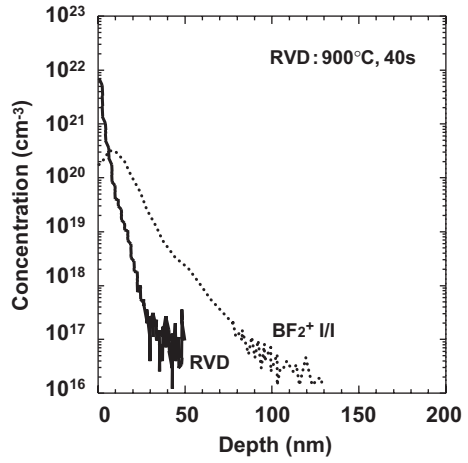

Fig. 1. SIMS profile of rapid vapor-phase doping (RVD). For comparison, the SIMS profile of $BF_2{}^+$ implantation with 10 keV and 5×10^{14} cm^{-2} for conventional devices is shown.

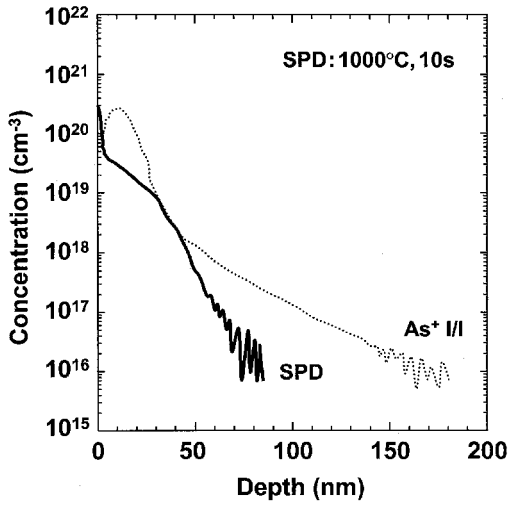

Fig. 2. SIMS profile of solid-phase diffusion (SPD) from phosphosilicate glass. For comparison, The SIMS profile of As^+ implantation with 15 keV and 5×10^{14} cm^{-2} for conventional devices is shown.

We found the upper limit of the n-type doping concentration of RVD is around 10^{19} cm^{-3}. This value is not high enough to form the S/D extension for 0.1-μm device. SPD is the only diffusion technique to form an appropriate n-type shallow junction. These rapid thermal diffusion techniques have allowed isotropically diffused S/D extensions to be formed with appropriate gate-extension overlap maintaining shallow junction.

Fig. 3 shows the plot of the p-type sheet resistance versus the junction depth X_j after RTA at 950 °C for 10 s. High concentration of boron near the surface is electrically activated by the additional annealing. The various junction profiles were obtained by varying B_2H_6 concentration or doping temperature and time. For the RVD sample, a shallow junction depth of 39 nm can be obtained at the same time as a low sheet resistance of 630 Ω/sq. This difference between RVD and ion-implantation was mainly caused by the difference in surface concentration, TED, and the channeling effect.

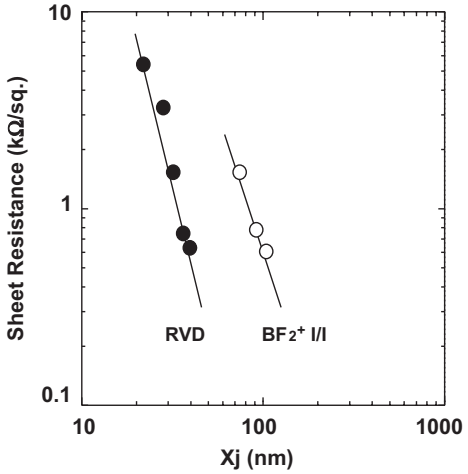

Fig. 3. Dependence of the sheet resistance on the junction depth (X_j) for p-type layers after additional RTA at 950 °C for 10 s. For comparison, data for the conventional junction formation used by $BF_2{}^+$ implantation and RTA are shown.

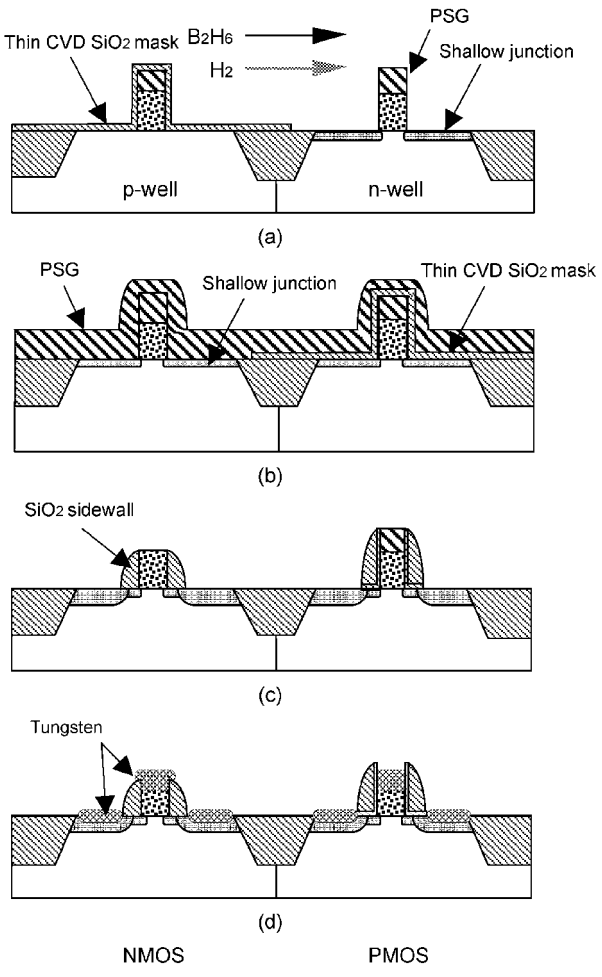

Fig. 4. CMOS process steps with RVD and SPD. (a) S/D extensions of the pMOSFET formed by RVD at 900 °C for 40 s. (b) S/D extensions of the nMOSFET formed by SPD from the PSG film at 1000 °C for 10 s. (c) Deep S/D formation. (d) Selective tungsten deposition.

B. A CMOS-Compatible RVD Process

Fig. 4 shows how the vapor- and solid-phase diffusion techniques were applied in a CMOS process. First, a thin 10 nm

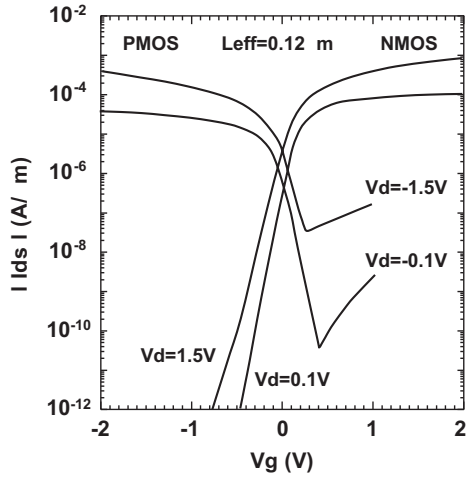

Fig. 5. Subthreshold characteristics of 0.12-μm MOSFETs.

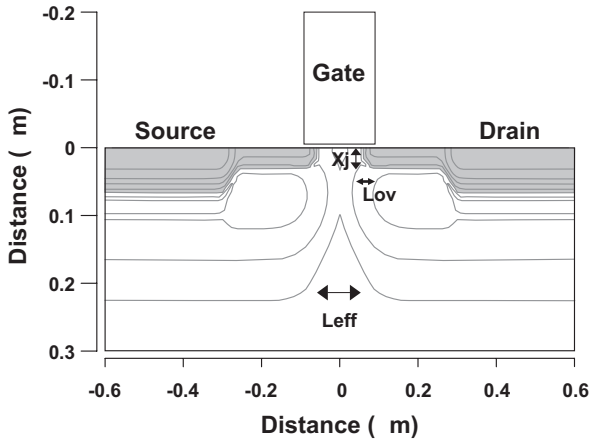

Fig. 6. Schematic cross section of the simulated RVD-pMOSFET. The gate-extension overlap is defined as L_{ov}.

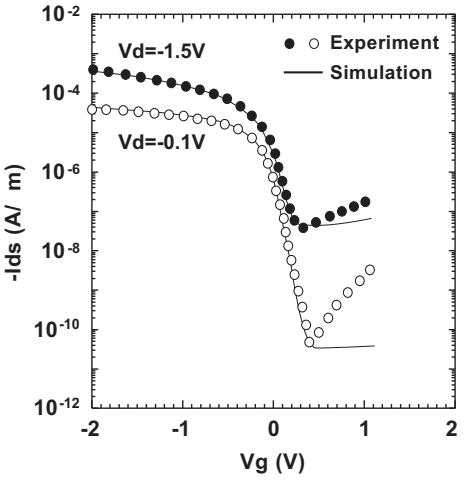

Fig. 7. Measured and simulated subthreshold characteristics of 0.12 μm RVD-pMOSFET.

chemical vapor deposition (CVD) SiO_2 layer was deposited and patterned in the nMOSFET region. The silicon substrate over the pMOSFET region was exposed by using light wet etching. Then RVD was carried out to obtain shallow pMOSFET junctions [Fig. 4(a)]. The 10 nm CVD SiO_2 layer protects the nMOSFET region from the boron diffusion. Next, a thin CVD SiO_2 layer was deposited again and the silicon substrate was exposed over the nMOSFET region. After that, a PSG layer that contained 8 mol% phosphorus was deposited and SPD from the PSG layer was carried out at 1000 °C for 10 s [Fig. 4(b)]. In the next step, the PSG layer, including the gate cap of the nMOSFETs, was then stripped away [Fig. 4(c)]. The PSG etch rate in hydrofluoric acid solutions is 20 times higher than that of thermal SiO_2. Thus, the PSG layer is easily removed, which simplifies this otherwise complex CMOS process. After the SiO_2 sidewall formation, deep S/D junctions were formed by using conventional ion implantation combined with RTA at 950 °C for 10 s. Then the PSG gate cap of the pMOSFETs was stripped away. Finally, 50-nm-thick tungsten was selectively deposited on the deep S/D junctions and the gate electrodes to reduce their resistance [Fig. 4(d)]. In this experiment, the gate oxide thickness, estimated from capacitance–voltage (*C–V*) measurements, was 4.5 nm. Local pocket implantation was done to suppress the short-channel effect. For comparison, conventional devices with ion implanted S/D extensions were also fabricated. The extensions ($As^+ 3 \times 10^{14}$ cm^{-2} at 15 keV; $BF_2^+ 5 \times 10^{14}$ cm^{-2} at 10 keV) were formed through a 5 nm SiO_2 layer. After the formation of a 70 nm SiO_2 spacer, deep S/D ion implantation ($As^+ 4 \times 10^{15}$ cm^{-2} at 40 keV; $BF_2^+ 3 \times 10^{15}$ cm^{-2} at 25 keV) and RTA at 950 °C for 10 s were carried out.

III. Device Characteristics

A. DC Characteristics

Fig. 5 shows typical subthreshold characteristics for devices with an effective channel length of 0.12 μm. The current–voltage (*I–V*) characteristics for the nMOSFET show no leakage current. On the other hand, leakage current was observed for the pMOSFET. Two types of the leakage current can be considered. One is the junction leakage current due to tungsten erosion along the Si/SiO_2 interface into the channel. Excessive dopants at the surface formed by RVD were segregated and they assist metallization into the channel near the gate edge. This local tungsten encroachment was confirmed by cross-sectional scanning electron microscope (SEM). Another one is gate-induced drain leakage (GIDL) current due to heavily doped S/D extension. To confirm this, GIDL current was evaluated by using the two-dimensional process simulator ATHENA and the device simulator ATLAS [9]. Band–band field emission and tunneling [10] were modeled in the simulation. The schematic simulated device structure is shown in Fig. 6. The isotropically diffused extension was formed in the simulated structure by using a thermal diffusion corresponding to the RVD process. Fig. 7 is the calibrated *I-V* characteristics that were fitted to the measurement results by changing the parameters of GIDL effects. However, the leakage current at $V_d = -0.1$ V can not be explained by GIDL effects. Thus, it is considered that excessive leakage current at lower V_d is due to junction leakage. This excessive leakage current can be suppressed by optimizing the selective tungsten deposition. A raised S/D technique using epitaxial growth is alternative solution to avoid the leakage current due to lateral diffusion of metal or silicide.

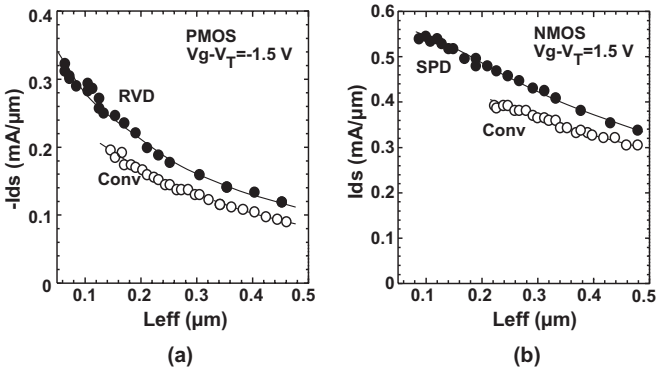

Fig. 8. Drain current (I_{ds}) as a function of effective channel length ($L_{\rm eff}$) of (a) pMOSFETs and (b) nMOSFETs.

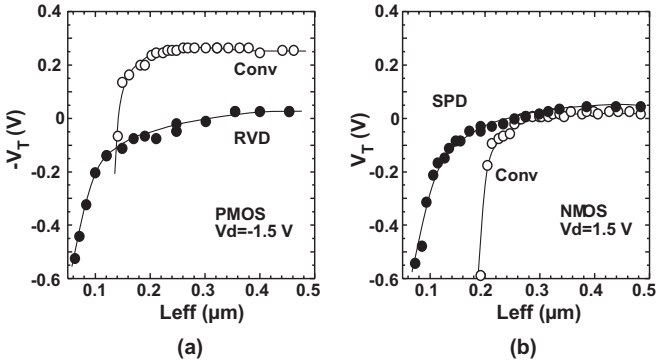

Fig. 9. Threshold voltage ($V_{\rm T}$) rolloff characteristics of (a) pMOSFETs and (b) nMOSFETs.

Fig. 8 shows the dependence of the drain current on the effective channel length. The drain current of the RVD and SPD devices was higher than that of the conventional devices. Higher current drivability was obtained through the heavily doped extensions and the lateral diffusion of the extension underneath the gate edge. For the nMOSFETs, the extension sheet resistance of the SPD devices was similar to that of conventional devices, so it can be concluded that lateral diffusion was the main cause of the improved current drivability. Fig. 9 shows the threshold voltage as a function of the effective channel length. Significantly improved threshold voltage rolloff characteristics were observed for the SPD and RVD devices. This improvement was achieved by forming shallow and abrupt S/D extensions. The lower threshold voltage for the RVD devices was due to boron penetration into the channel near the gate edge. The threshold voltage shift in the pMOSFETs was confirmed by *C-V* measurements. Fig. 10 shows the dependence of the flat-band voltage on the RVD process conditions. The flat-band voltage increased with an increasing thermal budget, and the difference in the flat-band voltages between typical RVD devices and the conventional devices was 0.15 V. In the RVD process, boron and hydrogen were supplied from the gate edge because hydrogen was used as a carrier gas. Thus, the boron penetration was enhanced near the gate edge. This boron penetration can be suppressed by forming a thin Si_3N_4 gate sidewall before the RVD process.

The device parameters are summarized in Table I. The lower S/D extension resistance of 400 Ω/sq and the shallow extension junction depth of 40 nm were achieved by using RVD for the pMOSFETs. These values were 80 and 33% lower, respectively,

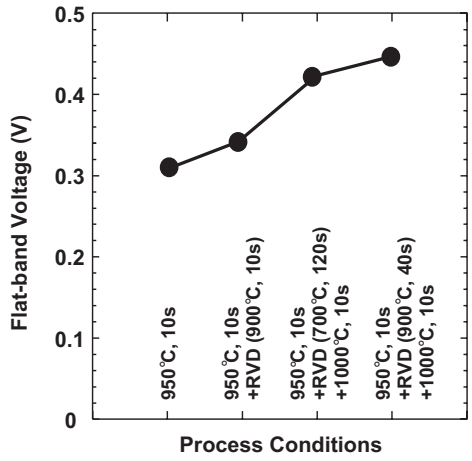

Fig. 10. Flatband voltage as a function of thermal budget in RVD-pMOSFETs.

TABLE I
DEVICE PARAMETERS OF THE FABRICATED DEVICES

Device		NMOS		PMOS	
		This Work	Conv	This Work	Conv
Extension	Rs (Ω/sq.)	510	500	400	1940
	Xj (nm)	46	52	40	60
Rex (Ω)		34	64	42	65
Drain Cap. (fF/ m^2)		1.24	1.61	1.75	1.76
Extension Cap. (fF/ m^2)		2.18	1.63	2.35	2.16
Overlap Cap. (fF/ m^2)		0.80	0.81	1.07	0.27

than those of conventional devices. The external S/D resistances were reduced by about 40% compared with those of conventional devices because of the large gate-extension overlap. However, the overlap capacitance was about four times larger than that of the conventional devices. To optimize the overall design of the transistor, it is necessary to achieve the best balance between on-current and capacitance. In the next section the optimization of the device structure will be discussed.

B. Gate-Extension Overlap Effect

A gate-extension overlap is required to get high on-current. However, excessive gate-extension overlap causes some drawbacks on the device performance. We therefore investigated how the S/D extension structure could be designed to give optimum device performance. The threshold voltage rolloff, drain current (I_{ds}), and overlap capacitance (C_{ov}) were characterized as a function of the lateral diffusion length (L_{ov}) of S/D extensions. The various L_{ov} were obtained by changing the doping condition. The dependence of the threshold voltage rolloff on the L_{ov} for the RVD pMOSFETs is shown in Fig. 11. L_{ov} was defined as the distance between the drain extension edge and the gate edge (Fig. 6) and it was determined by the channel resistance method [11]. A degradation of threshold voltage rolloff characteristics was observed in the devices with $L_{ov} = 75$ nm due to increased charge sharing. The short channel effects were improved by a shallower junction and smaller L_{ov}. The dependence of normalized drain current on L_{ov} is shown in Fig. 12.

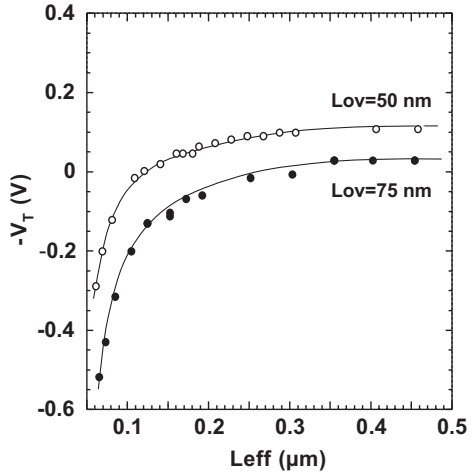

Fig. 11. Comparison of the gate-extension overlap (L_{ov}) dependence on $V_{\rm T}$ rolloff characteristics for RVD-pMOSFETs.

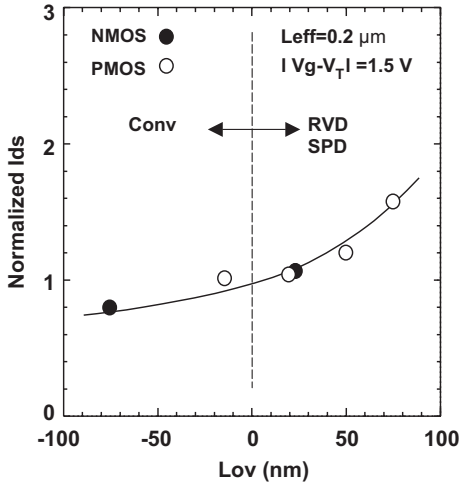

Fig. 12. I_{ds} versus L_{ov}. I_{ds} is normalized by respective $L_{ov} = 0$ values.

The ion implanted S/D extension devices showed a negative L_{ov} because of their graded channel profiles due to high counter doping [12]. On the contrary, the RVD and PSD devices had a positive L_{ov} because of the isotropically and heavily doped S/D extensions. The drain current increased with increasing L_{ov} because of the reduction of external resistance. The dependence of the overlap capacitance on L_{ov} is shown in Fig. 13. The overlap capacitance increases with increasing L_{ov}. The dependence of the overlap capacitance on L_{ov} is stronger in pMOSFETs than in nMOSFETs due to the interfacial diffusion of boron underneath the gate edge. Similar results have been reported by Young *et al.* [13] who considered that boron is easy to diffuse along the $\rm Si/SiO_2$ interface into the channel region.

C. Circuit Performance

To test the circuit performance, unloaded CMOS ring oscillators were used. A CMOS inverter gate delay of 22 ps/gate at a power supply voltage of 1.5 V was obtained. Fig. 14 shows the simulated variation of inverter gate delay with effective channel length for various values of L_{ov} for the pMOSFETs. The value of L_{ov} for the nMOSFETs was fixed at 25 nm. The gate delay was decreased with decreasing L_{ov} due to less overlap capacitance. Thus, we found that pMOSFETs with $L_{ov} = 25$ nm enabled excellent dc and high-speed circuit performance in 0.1 μm effective channel length devices. As a result, a shallower junction is required to obtain lower overlap capacitance and higher circuit performance.

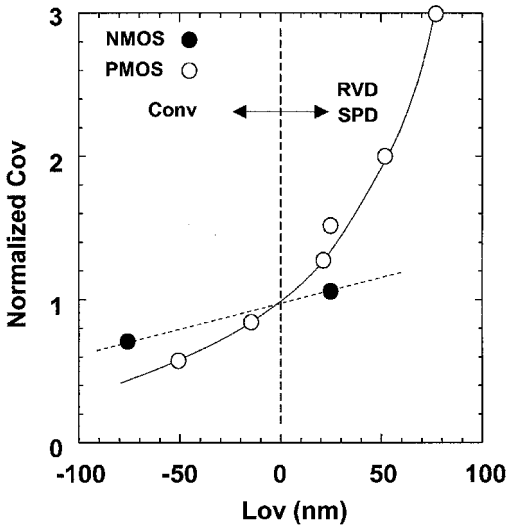

Fig. 13. Overlap capacitances (C_{ov}) versus L_{ov}. C_{ov} is normalized by respective $L_{ov} = 0$ values.

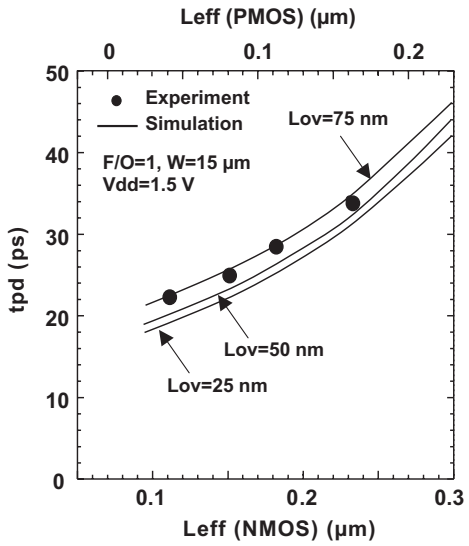

Fig. 14. Dependence of CMOS inverter gate delay time (tpd) on Leff.

IV. Summary

We have developed an advanced CMOS technology using two techniques in combination: RVD and SPD. The RVD and SPD devices we fabricated have shown excellent threshold voltage rolloff characteristics down to 0.1 μm effective channel length, a drain current 40% higher than that of conventional devices, and high-speed circuit performance. This high level of performance was due to the shallow and steep junctions formed by using RVD and SPD. We also investigated the effect of the S/D extension structure on the device performance. We found that a gate-extension overlap of 25-nm enabled excellent dc characteristics and high-speed circuit performance in 0.1-μm devices.

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