TABLE III
THE DEVICE RF AND POWER CHARACTERISTICS COMPARISONS OF THE $Al_xGa_{1-x}As/InGaAs$ DCFETs

$Al_xGa_{1-x}As$ Schottky Layer	RF Performance		Microwave Power Performance		
	f_T (GHz) V_d=3V	f_{max} (GHz) V_d=3V	P_{out} (dBm) Max.	G_p (dB) Max.	PAE(%) Max.
x = 0.3	10	22	14.5	15.7	19
x = 0.5	13	25	15.2	16.3	22
x = 0.7	9	20	14.3	15.2	10
x = 1	7	17	10.5	10.3	5.1

exhibits the same trend with their gate diode characteristics, where the higher Al content devices present the lower gate leakage current, and all leakage currents are increased by increasing the input rf powers.

IV. CONCLUSION

In summary, the $Al_xGa_{1-x}As/InGaAs$ ($x = 0.3, 0.5, 0.7, 1$) DCFETs on GaAs substrates were fabricated and characterized. Based on the experimental evaluations, we conclude that for the aluminum content of $Al_{0.5}Ga_{0.5}As$, i.e. $x = 0.5$, is the best composition to realize DCFETs in terms of device dc and RF characteristics. Although higher Al content devices ($x = 0.7, 1$) can further enhance the Schottky diode performance; however, due to the inferior material quality and higher parasitic resistance, the device characteristics degrade. The dc peak extrinsic g_m of $Al_{0.5}Ga_{0.5}As/In_{0.15}Ga_{0.85}As$ DCFETs is 272 mS/mm, together with an f_T of 13 GHz and an f_{max} of 25 GHz. As to the power performance at 2.4 GHz, it demonstrates a 15-dBm saturated output power, a 16.5—dB linear power gain and a 20% efficiency.

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Design of 50-nm Vertical MOSFET Incorporating a Dielectric Pocket

D. Donaghy, S. Hall, C. H. de Groot, V. D. Kunz, and P. Ashburn

***Abstract*—A new architecture for a vertical MOS transistor is proposed that incorporates a so-called dielectric pocket (DP) for suppression of short-channel effects and bulk punch-through. We outline the advantages that the DP brings and propose a basic fabrication process to realize the device. The design issues of a 50-nm channel device are addressed by numerical simulation. The gate delay of an associated CMOS inverter is assessed in the context of the International Technology Roadmap for Semiconductors and the vertical transistor is seen to offer considerable advantages down to the 100-nm node and beyond due to the dual channels and the ability to produce a 50-nm channel length with more relaxed lithography.**

***Index Terms*—Dielectric pocket, short-channel effects (SCEs), Si devices, vertical MOSFET.**

I. INTRODUCTION

It is recognized that vertical transistors can overcome scaling problems due to lithography resolution, whereby decananometer channels can be realized with relaxed lithography as the channel length is determined by the accuracy of ion-implantation or epitaxial growth. Vertical transistors also allow double gate or gate all-around structures thus increasing current drive albeit at the expense of increased device capacitance. The architectures are however compact and hence give a high drive with reduced footprint compared to an equivalent lateral architecture, as demonstrated in [1]. Much of the work reported previously is concerned with discrete device fabrication often using fabrication techniques that could not be easily integrated into an advanced CMOS process [2]–[5]. We report here on a novel vertical transistor architecture incorporating a so-called dielectric pocket (DP) [6], [7] for control of short-channel effects (SCEs). This concept was first demonstrated successfully within a lateral architecture [8], but implementation in a vertical architecture is considerably simpler. The structure is compatible with strategies reported previously to reduce parasitic capacitances

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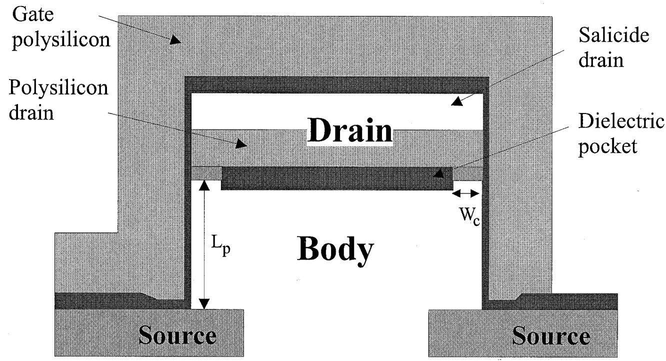


Fig. 1. Cross section showing the concept of the dielectric pocket vertical MOST.

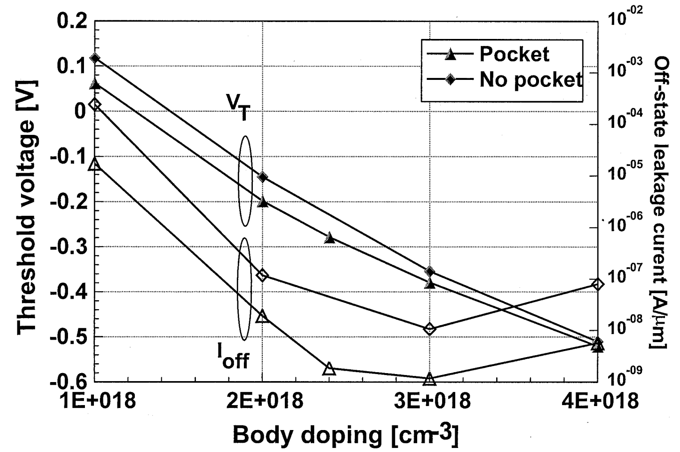


Fig. 2. Threshold voltage and offstate leakage current versus body doping for 50 nm vertical MOSTs with and without dielectric pocket. The gate oxide thickness was 2 nm.

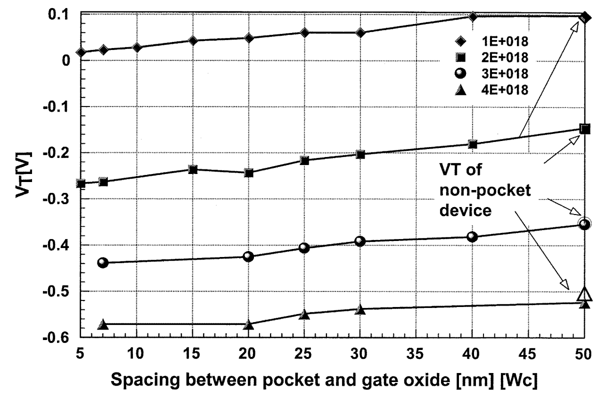
in the device [7], [9]. The objective of this communication is to demonstrate the use of a dielectric pocket to suppress short channel effects in a vertical MOSFET, rather than other strategies such as pocket implantation. Furthermore, we demonstrate how the device could be designed and made and assess its potential performance in the context of the International Technology Roadmap for Semiconductors (ITRS).

II. Device Design and Performance Appraisal

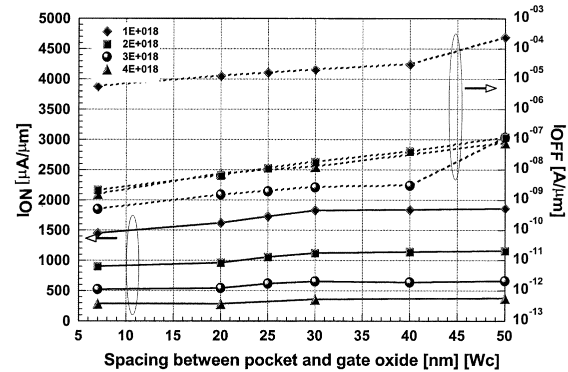
The basic structure of the vMOST device concept is shown in Fig. 1. The pocket serves a number of functions; it greatly reduces the influence of the large area parasitic bipolar transistor in the vertical structure, and also prevents encroachment of the doping from the extrinsic drain, so reducing electrical bulk punchthrough effects. Furthermore, it reduces charge sharing effects associated with the reverse biased drain and so improves threshold control.

Referring again to Fig. 1, a basic process to realize such a device could be as follows. Body regions are implanted for pMOS and nMOS followed by growth of an oxide layer to form the DP. A layer of polysilicon is then deposited to form the extrinsic drain contact. This layer is partly silicided to reduce drain resistance. The pillar is then etched with overetching of the DP layer to undercut the poly-Si drain contact. A blanket silicon epitaxial layer is then grown with continuity over the DP edge realized because the epi can seed on the Si region under the DP and also on the extrinsic drain poly-Si layer, because of the undercut profile. This process is similar to that used in SiGe HBTs [10], where a graft base is formed on the bottom face of an exposed polysilicon layer. The gate oxide is then grown followed by gate electrode formation by deposition of poly-Si followed by appropriate implant. Care is required with the thermal budget to ensure that only slight out-diffusion occurs from the extrinsic drain contact such that there is no encroachment of drain dopant below the DP into the channel region. Such encroachment would remove the electrostatic influence of the DP on the channel and so mitigate its influence on the SCE. Note that dual channel operation is achieved by the gate poly-contact running over the pillar width, which is set to the minimum feature size to reduce drain/gate overlap capacitance.

The ISE device simulator was used to obtain electrical characteristics for the DP vMOST. The Van Dort quantum correction model, hydrodynamic model, avalanche and band-to-band tunnelling were all switched on to provide selfconsistent data for short-channel, highly doped devices. The dielectric pocket thickness was set at 15 nm to minimize its parasitic capacitance [7]. The gate oxide thickness was set at a conservative value of 2 nm. The body doping was then varied to produce electrical characteristics for the pMOS with and without the DP, as summarized in Fig. 2. Note that the threshold voltage V_T was determined by linear extrapolation of transconductance $g_m(V_{GS})$ to zero [11] and the offstate leakage current was taken as the current measured at $V_{DS} = -1$ V and $V_{GS} = 0$ V. The leakage current is seen to be a minimum for a body doping of 3.0×10^{18} cm^{-3}; band-to-band tunnelling becomes increasingly dominant beyond the minimum whereas punchthrough causes the increase in leakage for lower doping levels. A body doping of 2.4×10^{18} cm^{-3} results in a threshold voltage of -0.28 V and a leakage current of 1.5 nAμm at a drain to source voltage of -1 V.



(a)



(b)

Fig. 3. (a) Effect of the contact width W_C on the threshold voltage for a p-channel vMOST, $L_P = 50$ nm, $W_P = 1$ μm, N_{body} varied from 1×10^{18} cm^{-3} to 4×10^{18} cm^{-3}, $V_{DS} = -1.0$ V. (b) Effect of the contact width W_C on I_{ON} and I_{OFF} for a p-channel vMOST, $L_P = 50$ nm, $W_P = 1$ μm, N_{body} varied from 1×10^{18} cm^{-3} to 4×10^{18} cm^{-3}, $V_{DS} = -1.0$ V.

A further set of simulations was undertaken to investigate the influence of the spacing between the pocket and the gate oxide, referred to as the contact region width W_C on the threshold voltage and results are shown in Fig. 3. The DP serves to increase the magnitude of

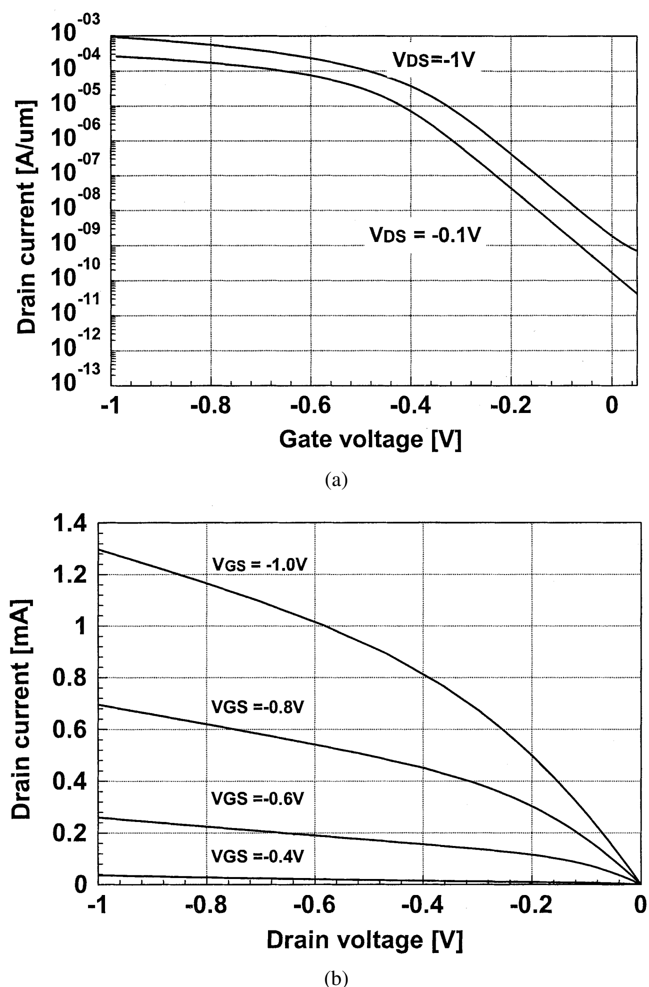


Fig. 4. Simulated vMOST dc characteristics for a p-channel $DP = \mathrm{vMOST}$, $L_P = 50$ nm, $W_P = 1$ μm, $N_{\mathrm{body}} = 2.4 \times 10^{18}$ cm^{-3}. (a) Transfer characteristics, for $V_{DS} = -0.1$ V and -1.0 V. (b) Output characteristics.

threshold voltage because it inhibits charge sharing by the drain. For $W_C = 50$ nm, the V_T equals that of the non-DP device indicating that the DP no longer exerts electrostatic influence as W_C is comparable to the depletion width under the gate. Fig. 3(b) shows that decreasing W_C results in significant reduction in I_{OFF} with little reduction in I_{ON}. For example, for a substrate doping of 2×10^{18} cm^{-3} and a pocket width of 30 nm, the reduction in I_{OFF} compared with no pocket is a factor of 10 but the reduction in I_{ON} is only 5%. Thus the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is improved by a factor of 5. The slight reduction in I_{ON} arises from the increase in V_T because of the reduced charge sharing. The much greater and beneficial reduction in I_{OFF} arises from the suppression of both drain induced barrier lowering and tunnelling as is also clearly evident on Fig. 2. Fig. 4 shows the simulated transistor characteristics and a DIBL of 80 mV is apparent for a body doping of 2.4×10^{18} cm^{-3}. Repeating the simulations with a gate oxide thickness of 1.2 nm results in a DIBL of 30 mV, $I_{\mathrm{OFF}} = 1.5$ nA/μ m, $I_{\mathrm{ON}} = 1.3$ mA/μ m.

The vMOST inverter performance with 2 nm gate oxide was compared to equivalent minimum sized lateral CMOS inverters deduced from ITRS 2001. The width of the pMOST, W_p was set to $2W_n$. Parameters extracted from ITRS were I_{dd} (saturation current), C_{gate} and $C_{\mathrm{parasitic}}$ (intrinsic gate and overlap capacitances), equivalent electrical oxide thickness, and supply voltage, V_{DD}. The delay was then calculated using $C_T V_{DD}/I_{dd}$ where $C_T = C_{\mathrm{gate}} + C_{\mathrm{parasitic}}$. For the vMOST, the gate oxide was scaled, as was C_T and V_T using the models of [7], [12], respectively. The simulation results of the 50-nm channel device allowed for some calibration and selfconsistency.

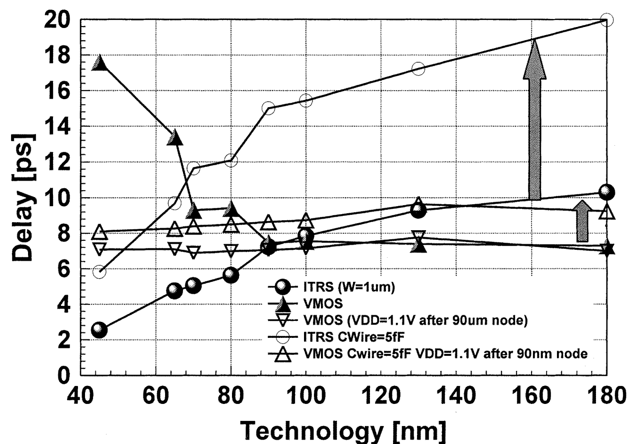


Fig. 5. Delay for DP vMOST versus technology node, compared to ITRS roadmap values. Channel width for all $\mathrm{devices} = 1$ μm. vMOS channel $\mathrm{length} = 50$ nm. Circles are for ITRS and triangles show vMOS performance. The arrows show the effect of adding a 5-fF load capacitor.

It's worth noting that the source and drain resistances of the vMOST (extracted from ISE simulation) are three to four times smaller than the ITRS values and this represents a further significant advantage of the vMOST architecture. This advantage arises because the dielectric pocket precludes the need for pockets or extensions. These resistances do not significantly increase when the device is scaled. Fig. 5 serves to make the comparison with the roadmap using the delay metric $C_T V_{DD}/I_{\mathrm{ON}}$. The vMOS shows a clear advantage down to the 90-nm node (note that the channel length of the vMOS is not scaled). Thereafter the performance deteriorates largely because of the reduced V_{DD}. The effect of maintaining V_{DD} for the vMOST is shown also. It should be noted that although C_T is higher for the vMOST, the ability to realize a 50-nm channel at coarser technology nodes produces a significant advantage over conventional lateral architectures. Beyond the 100-nm node, we can say that load capacitance due to interconnections will have a very dominant role and so the additional drive capability of the vMOS should continue to offer considerable advantage. We demonstrate this by including a fixed load capacitance of 5 fF in the calculation of delay. In this context, the smaller relative degradation in performance of the vMOST compared with the ITRS roadmap demonstrates the potential of the latter device. Finally, it is worth noting that we envisage no serious problem in scaling the device to 20-nm channel length.

III. Conclusion

We have proposed and presented design details of a novel vertical transistor architecture that offers good short channel control and drive capability together with low off current. The off current can be reduced without seriously compromising on current. The device can easily be scaled without incurring high series parasitic resistances. Fabrication would still be realized with existing tools. The use of a DP within a vertical architecture therefore opens up a new design space for these vertical transistors and allows greater flexibility than is afforded by simple scaling of lateral MOSFETs.

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