Compressively-strained, buried-channel $Si_{0.7}Ge_{0.3}$ p-MOSFETs fabricated on SiGe virtual substrates using a 0.25 μm CMOS process

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***Abstract*— Enhanced performance is demonstrated from a buried, compressively strained-$Si_{0.7}Ge_{0.3}$ p-MOSFET fabricated on a relaxed $Si_{0.85}Ge_{0.15}$ using a high thermal budget 0.25 μm CMOS process. The devices are designed to be fully compatible with a strained-Si CMOS process but offers a number of potential benefits over a surface channel p-MOSFET for certain circuit applications. Transconductance, on-current, hole velocity and mobility enhancements are observed over surface strained-Si channel devices on both $Si_{0.85}Ge_{0.15}$ and $Si_{0.8}Ge_{0.2}$ virtual substrates and the bulk Si control devices for constant effective channel length. The buried channel devices exhibit enhancements over the Si control devices of 93% in on-current and 62% in hole velocity for 0.25 μm effective channel length devices without compromising the subthreshold characteristics. The extracted effective mobility for the buried channel device is over 40% greater than the universal mobility curve for bulk Si p-MOS devices at 0.55 MV/cm vertical effective electric fields.**

***Index Terms*— CMOS, p-MOSFET, strained-Si, SiGe, quantum well, thermal budget, drain current enhancements, transconductance enhancements, virtual substrate.**

I. Introduction

SiGe in the form of the heterojunction bipolar transistor became a main stream technology in 1999 with the sales of the first circuits using the technology [1][2]. While the share of SiGe devices has been increasing even during the microelectronics market downturn in the last few years, it is complementary metal oxide semiconductor (CMOS) technology which has the largest share of the microelectronics market [3]. CMOS devices are now being aggressively scaled to gate-lengths below 100 nm and predictions suggest that the scaling is likely to continue for at least another decade [3]. A number of problems, however, are being found as the MOSFET gate-lengths are reduced. In particular the gate oxide thickness in state-of-the-art production devices is now below 2 nm and thinner oxides increase the off-state current through the increase in quantum mechanical tunnelling of charge through the gate insulator [4]. A secondary effect of the reduction of the gate insulator thickness is the reduction of electron and hole mobilities in the inversion layers of CMOS transistors [4][5]. Therefore a number of technology solutions are being pursued to find methods of circumventing these problems.

One of the leading contenders for improving the mobilities of the inversion layer carriers is the use of strained-Si technology [6][7][8]. A number of different schemes are being researched to produce appropriate strain in the n- and p-channel devices but most include SiGe technology. Many of the main microelectronic companies are involved in SiGe technology research at some level.

Ge has a 4.2% larger lattice constant than Si. Therefore the growth of a $Si_{1-x}Ge_x$ heterolayer on top of a silicon or a relaxed $Si_{1-y}Ge_y$ buffer layer or virtual substrate results in a compressively strained SiGe channel for $x > y$ [8][9][10]. By growing a strain relaxation buffer of $Si_{1-y}Ge_y$ followed by a tensile strained-Si layer results in a structure which from a processing point of view, looks very similar to a silicon wafer and can be processed in a fashion much closer to a standard CMOS process [8][9][10]. This is the basis of strained-Si CMOS. The tensile strain splits the conduction band valleys with the Δ_2 valleys being lowered in energy and the Δ_4 valleys being increased in energy to such an extent that only the lower Δ_2 valleys have any significant population of carriers [9][10]. A quantum well is formed with a conduction band discontinuity of $\sim 0.6y$ eV for a strained-Si grown on top of a relaxed $Si_{1-y}Ge_y$ buffer and this combined with the high effective mass in the vertical direction confines the electrons in the tensile strained-Si surface layer. The reduction of intervalley scattering has demonstrated significant increases in the n-MOSFET mobility both at room [11]-[15] and low temperatures [8]. Strained-Si on insulator has also been used to increase the mobility enhancements [16][17].

For holes the situation is very different. For both compressive or tensile strain, the light-hole and heavy-hole bands are split but only by a small amount so both have significant populations of carriers especially with the high electric fields produced in short-channel CMOS devices [9][10]. The major change is the reduction in the density of states heavy-hole effective mass for both compressive and tensile strain [10]. For the light-hole mass, tensile strain reduces the mass value but compressive strain increases the mass. The reduction in the heavy hole mass, however, is significantly higher for

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compressive strain. A second issue is that a tensile strained-Si layer grown on a relaxed $Si_{1-y}Ge_y$ buffer is higher in energy to holes than the relaxed substrate [9][10]. This combined with the lower effective mass in the vertical direction results in a larger spread of the wavefunction into the substrate compared to electrons. It can result in a parasitic channel of holes in the relaxed $Si_{1-y}Ge_y$ buffer especially if high Ge contents in the substrate are used to improve the mobility since then only a thin strained-Si channel can be grown under the critical thickness. Therefore the use of a buried, compressively strained-$Si_{1-x}Ge_x$ quantum well may have advantages in improving the hole mobility in such devices by the use of the lower effective mass and by confining the holes away from the Si/SiO_2 interface [7][18]. The mobility enhancement in the strained-Si surface p-MOSFET has been limited to less than 30% for standard virtual substrates with Ge contents of 20% and below [13][15] with silicon-on-insulator devices required for any significant mobility improvement [17][19].

A number of papers have demonstrated the higher mobility possible in compressively strained SiGe quantum wells either in p-MOSFETs or modulation-doped FETs but all have used low thermal budget processing [20][21][22]. In particular deposited gate insulators rather than a thermal gate oxide have frequently been used [20]. We have previously demonstrated the performance of strained-Si n-MOS transistors fabricated on top of a buried $Si_{0.7}Ge_{0.3}$ layer with a $Si_{0.85}Ge_{0.15}$ virtual substrate and processed using a high thermal budget 0.25 μm CMOS process [14]. Significant performance enhancements were demonstrated over bulk Si devices. Very little performance degradation was demonstrated with the addition of the buried $Si_{0.7}Ge_{0.3}$ layer to the strained-Si n-MOS devices. We have also demonstrated improved strained-Si p-MOS enhancements with high thermal budget processing using low energy plasma enhanced chemical vapor deposition virtual substrates [23]. In this paper we demonstrate p-MOS transistors with a compressively strained buried $Si_{0.7}Ge_{0.3}$ channel, grown on a $Si_{0.85}Ge_{0.15}$ virtual substrate and processed using the same high thermal-budget CMOS process as the n-MOS devices [14]. Enhanced performance over control Si devices of I_{on}, transconductance, hole velocity and mobility are observed for a large range of effective channel length devices. The extracted effective mobility for the buried channel device is over 40% greater than the universal mobility curve for bulk Si p-MOS devices at 0.55 MV/cm vertical effective electric fields.

II. Device Design and Fabrication

The wafers were grown by low pressure chemical vapor deposition on 100 mm n-type (18-33 Ω-cm) (100) silicon substrates [24]. The process gases of Si_2H_6 and GeH_4 were used with AsH_3 as the n-type dopant. Virtual substrates were grown at 800 ^{o}C with the active regions grown at 550 ^{o}C to reduce Ge diffusion. Typical growth parameters can be found in [24]. The virtual substrates consisted of 1.5 μm graded SiGe followed by 1 μm of constant composition $Si_{1-y}Ge_y$ doped with As to 10^{17} cm^{-3} with Ge contents of y=0.15 and 0.20. The temperature was then reduced to 550 ^{o}C before a constant Ge composition undoped spacer of 50 nm was

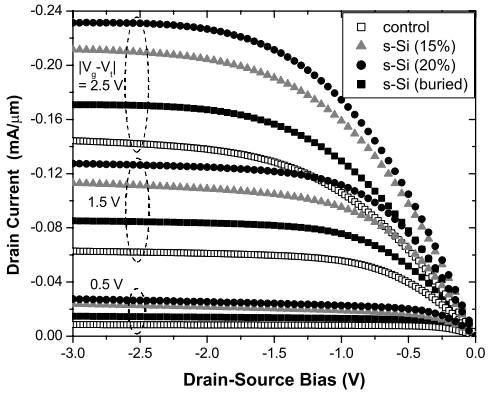

Fig. 1. The drain-current as a function of source-drain voltage for gate overdrive voltages of 0.5, 1.5 and 2.5 V. All devices have a lithographic gate length of 0.3 μm and 5 μm width and all measurements are dc.

then grown followed by the channel layers. The thickness of this spacer layer was chosen after modelling the As diffusion during the high thermal budget fabrication process to produce a retrograde doping profile for the n-type wells. N-type dopant diffusion of As and P in SiGe is known to be larger than that in bulk Si [25] but there is little accurate data in the literature for the diffusivity of n-type dopants in SiGe. Therefore the setback of the dopant was modeled using diffusion data for Si [26]. All process steps with thermal anneals above 400 ^{o}C were included in the diffusion modeling. Simulations indicate that a 50 nm spacer will result in a channel doping of less than 10^{16} cm^{-3} whilst providing good subthreshold characteristics.

On the $Si_{0.85}Ge_{0.15}$ virtual substrate a 20 nm i-Si layer was grown and a 17 nm i-Si on the $Si_{0.8}Ge_{0.2}$ virtual substrate. Both these tensile strained-Si layers are below the Matthews and Blakeslee critical thickness [27] and should therefore be stable to high temperature processing [28][29]. The buried channel device was grown on top of a $Si_{0.85}Ge_{0.15}$ virtual substrate and consisted of a 50 nm undoped $Si_{0.85}Ge_{0.15}$ spacer, a 10 nm undoped compressively-strained $Si_{0.7}Ge_{0.3}$ channel and a 10 nm undoped tensile-strained Si cap. This cap thickness was chosen after a number of simulations to calculate the consumption of the cap through cleans, thermal oxide growth and also Ge diffusion [30] from the $Si_{0.7}Ge_{0.3}$ channel. At least 2 nm of Si cap should remain after the devices have been processed. This is especially important as any Ge incorporated into the oxide would create defect states or result in Ge pileup at the SiO_2 interface increasing the interface trapped charge density and reducing the transistor performance [31][32].

Device fabrication followed the process flow of a high-thermal budget 0.25 μm CMOS process [14][23]. Si control wafers were also processed after the n-well was implanted using a three stage phosphorus implant of 4×10^{12} cm^{-2} dose at 400 keV, 2×10^{13} cm^{-2} dose at 280 keV and 2×10^{12} cm^{-2} dose at 70 keV. Modelling was used to design the well implant to be nominally identical to the well doping in the as-grown heteroepitaxial material. It should be noted that Si wafers with epitaxially grown doping profiles demonstrated near identical performance to the present Si control implanted well wafers [33]. No chemical mechanical polishing (CMP) of the starting

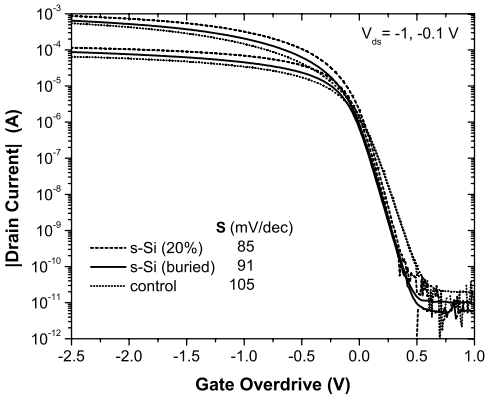

Fig. 2. The subthreshold plots for the Si control, strained-Si on $Si_{0.8}Ge_{0.2}$ and buried channel devices. All devices have a lithographic gate length of 0.3 μm and 5 μm width.

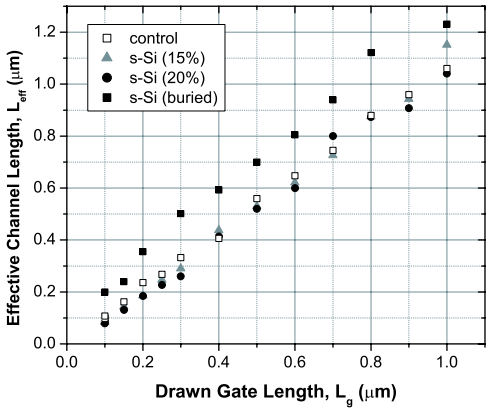

Fig. 3. The effective channel length as extracted by the shift and ratio technique versus the drawn or lithographic gate length for the 4 different wafers.

substrates at any stage was undertaken as previous results have demonstrated significantly higher mobilities [14][23] than CMP polished substrates[13][20]. As CMP is likely to produce off-cut surfaces when the growth and relaxation processes are considered [34], non CMP substrates should be expected to produce higher mobilities [35]. A thermal gate oxide was grown at 800 ^{o}C followed by an anneal in a N_2 atmosphere. Source and drain implants using high doped drain (HDD) and low doped drain (LDD) structures with Si_3N_4 spacers were activated with a 1020 ^{o}C rapid thermal anneal and a full titanium salicide process was used. Oxide thicknesses of 4.5 nm were extracted from C-V characteristics of 300×300 μm MOS capacitors.

III. Electrical Results

Fig. 1 shows the measured drain current, I_{ds} as a function of source-drain bias V_{ds} for as-drawn 0.3 by 5 μm (L_g by W) devices at three values of gate overdrive $|V_g - V_t|$ where V_g is the gate voltage and V_t is the threshold voltage. On-current enhancements are observed for each of the strained-Si devices including the buried channel over the bulk Si controls. At $|V_g - V_t| = -V_{ds} = 2.5$ V, I_{ds} for the strained-Si surface channel device on $Si_{0.85}Ge_{0.15}$ exceeds that of the control by 50%, whereas for the strained-Si device on $Si_{0.8}Ge_{0.2}$ the enhancement is 60%. The enhancements are higher at lower gate overdrive ($|V_g - V_t| = 1.5$ V) due to the result of reduced self-heating in the strained-Si devices [36] since only dc measurements of devices are presented in this paper. It is apparent from Fig. 1, however, that the current drive performance is considerably lower for the buried channel device than for the surface channel strained-Si devices. I_{ds} enhancements of the buried channel device over the Si control of 38% at -1.5 V and 21% at -2.5 V are observed.

The subthreshold I_{ds} versus $|V_g - V_t|$ characteristics for the same strained-Si (20%), buried channel and control devices are plotted in Fig. 2. All the devices exhibit on-current/off-current ratios of at least seven orders of magnitude, suggesting, together with the extracted values of subthreshold slope, S that electrostatic integrity is not seriously compromised in the strained-Si devices. The strained-Si and buried channel devices actually have better subthreshold slopes that the Si control devices.

IV. Effective Channel Length

The plotting of performance parameters as functions of lithographic gate length, L_g, however, can be misleading especially for submicron LDD MOSFETs. In such cases, the effective channel length L_{eff} is normally taken as the independent variable rather than L_g in comparing channel-length dependent performance parameters [37]. Particularly in LDD structures, the lateral straggle in the source and drain doping can actually cause L_{eff} to increase significantly with respect to L_g, as can a retrograde, setback or modulation doping profile [37]. Furthermore, L_{eff} may exhibit a strong dependence on gate bias at low gate overdrives $|V_g - V_t|$ because of the virtual channel which forms in the LDD regions under or close to the gate contact [38]. The diffusivities of dopants in strained-Si and SiGe are expected to be higher than in bulk Si especially for the p-type implant boron used for the Ohmic contacts [39], possibly leading to different LDD and HDD source and drain profiles and hence different metallurgical as well as effective channel lengths. L_{eff} is effectively a measure of the length over which a gate bias can invert charge in the substrate to form a channel, and is also found to be sensitive to the doping profile perpendicular to the channel; it is found to be significantly longer than the metallurgical gate length in the case of retrograde doping [37] and for buried channel Si pMOSFETs [40]. In fig. 3 L_g is plotted against L_{eff} for the Si controls and the surface- and buried-channel strained-Si devices. The shift and ratio method for L_{eff} extraction was used and is described in detail elsewhere [23][37]. For the shortest channel length devices, L_g is longer than L_{eff} for the strained-Si surface channel devices, as expected from enhanced source and drain diffusion, compared with the controls. For the buried channel devices, L_{eff} is indeed significantly higher by approximately 0.2 μm, as anticipated.

Replotting Fig. 1 for a constant L_{eff} of 0.25 μm is shown in Fig. 4. For L_{eff} of 0.25 μm, the buried channel device now has higher performance than the surface strained-Si p-

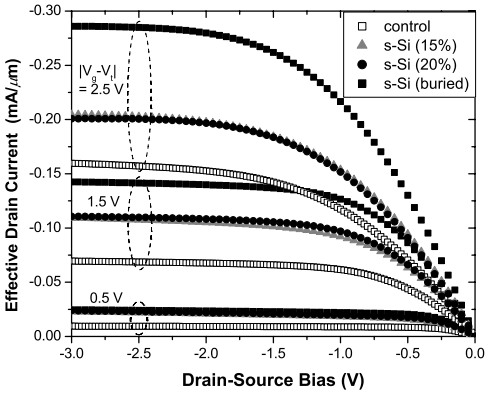

Fig. 4. The drain-current as a function of source-drain voltage for gate overdrive voltages of 0.5, 1.5 and 2.5 V. All the devices have an effective channel length of 0.25 μm and width of 5 μm.

MOSFETs and the Si control. For $|V_g - V_t| = -V_{ds} = 1.5$ V, I_{ds} for the strained-Si surface channel device on a $Si_{0.85}Ge_{0.15}$ virtual substrate exceeds that of the control by 45%, for the strained-Si device on the $Si_{0.8}Ge_{0.2}$ virtual substrate the enhancement is 57% and the buried channel has a 92% enhancement. These values are reduced for an applied bias of 2.5 V to 24%, 22% and 71% respectively again demonstrating the self-heating in the devices [36]. It must be stated that enhanced performance from the buried channel transistor is a device with a lithographically or as-drawn gate length around 0.2 μm smaller than some of the other devices in the same plot and demonstrates one of the disadvantages of the buried channel design in that the gate has less control of the channel since it is further from the gate. The results also demonstrate that the band-offset of the heterostructure also plays a significant rôle in changing the effective channel length of a device. As the cost of lithographically typically increases exponentially with the exponential decrease in minimum feature size [3][8], this is a significant disadvantage for the buried channel device.

The maximum transconductance, g_m^{max} per unit width divided by the oxide capacitance, C_{ox} versus lithographic and effective channel lengths are plotted in Fig. 5(a) and 5(b) respectively. The g_m^{max}/C_{ox} is a measure of the hole velocity and therefore is a good measure of material performance which should be relatively device independent. It is also independent of oxide thickness allowing the values to be easily compared to other devices with substantially different oxide thicknesses. Again the performance of the buried channel device is above that of the control Si sample for the lithographic gate lengths but below the strained-Si surface channel devices. When the effective channel length is plotted, the buried channel device is superior to all the other devices for all gate lengths (Fig. 5(b)). Enhancements over the Si control of 23% for the strained-Si on $Si_{0.85}Ge_{0.15}$ virtual substrates, 45% for the strained-Si on $Si_{0.8}Ge_{0.2}$ virtual substrates and 62% for the buried channel devices were measured for an effective channel length of 0.25 μm for a low source-drain bias of -0.1 V.

Fig. 6 shows the drain induced barrier lowering (DIBL) as a function of lithographic gate length. No significant increase in the roll-off is observed for the strained-Si devices, indicating that electrostatic integrity is conserved notwithstanding the

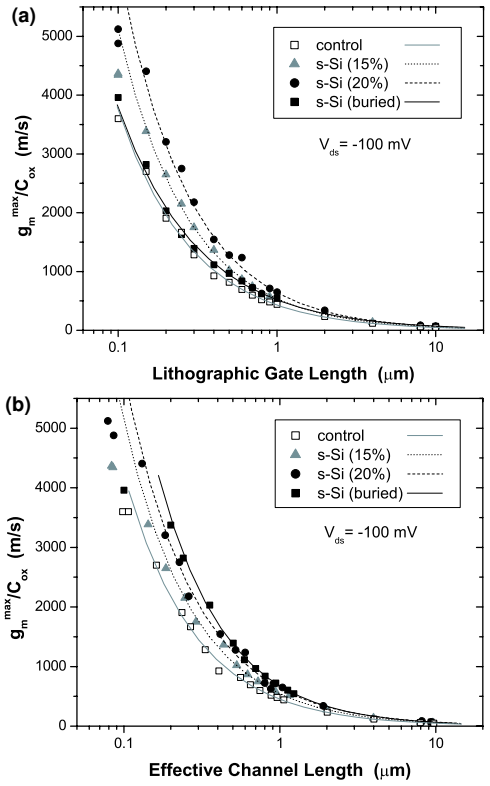

Fig. 5. (a) The velocity of the holes (that is g_m^{max}/C_{ox}) versus the drawn or lithographic gate length for the four wafers for device widths of 5 μm. (b) The velocity of the holes (that is g_m^{max}/C_{ox}) versus the effective channel length.

strain, in spite of the high thermal budgets employed in the fabrication of the devices. The buried channel devices have almost comparable performance to the control Si device down to 0.2 μm drawn gate length.

A. Effective Mobility

Effective mobilities μ_{eff} as functions of vertical effective electric fields E_{Eff} were calculated for long channel devices (L= 100 μm) according to the expressions

$$\mu_{eff} = \frac{L}{W} g_d\left(V_g\right) Q_{inv} \tag{1}$$

and

$$E_{eff} = \frac{1}{\epsilon_{Si}}\left(Q_b + \eta Q_{inv}\right) \tag{2}$$

where $\eta = 1/3$ for holes and Q_{inv} and Q_b are the inversion layer (i.e. channel) and the bulk (depletion) charge densities, respectively. The drain conductance $g_d\left(V_g\right)$ was obtained from $-I_d(V_g)/V_{ds}$ measured at low drain bias ($V_{ds} = 10$ mV). The charge densities are computed from split C-V measurements [41][42]:

$$Q_{inv} = \int_{V_g}^{\infty} C_{gc} dV_g \tag{3}$$

and

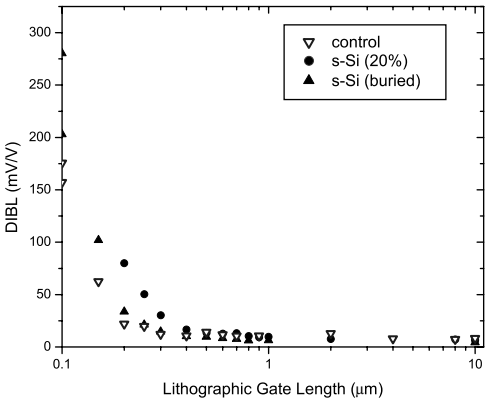

Fig. 6. The drain induced barrier lowering (DIBL) as a function of effective channel length for 5 μm wide devices.

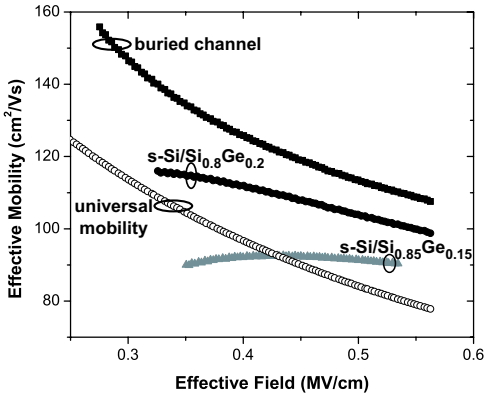

Fig. 7. The effective mobility as a function of the vertical electric field for the strained-Si and buried channel devices with the universal mobility of bulk Si control devices plotted for comparison.

$$Q_b = \int_{V_g}^{V_{fb}} C_{gb} dV_g \tag{4}$$

where C_{gc} is the gate-to-channel and C_{gb} the gate-to-body capacitance (per unit area). The flat-band voltage V_{fb} which limits the integration in (4) is determined from the high-frequency MOS-C capacitance measurements [43], and the overlap capacitance was subtracted from C_{gc} before performing the integration in (3). The $\mu_{eff} - E_{eff}$ characteristics for the buried and strained-Si devices are plotted in Fig. 7 along with the universal mobility curve for a bulk Si p-MOS device. The control sample had effective mobility below the universal curve and has been omitted for clarity. The results for the strained-Si devices on both the $Si_{0.85}Ge_{0.15}$ and the $Si_{0.8}Ge_{0.2}$ virtual substrates show modest enhancements compared to the universal curve and are comparable to many results in the literature [13][15]. Both of these mobilities are significantly below the values calculated by the theory of Oberhuber et al. [44] for strained-Si p-MOS devices at these Ge contents. The buried channel device does demonstrate significantly higher mobility of a 40% enhancement over the universal curve at an effective electric field of 0.55 MV/cm. While the theory of Oberhuber et al. [44] is only for strained-Si surface channel devices, the value of 40% enhancement for the buried channel is much closer to the value predicted by the theory for surface channel devices.

V. Conclusion

Enhanced performance over bulk Si and strained-Si p-MOS devices fabricated on $Si_{0.85}Ge_{0.15}$ and $Si_{0.8}Ge_{0.2}$ virtual substrates has been demonstrated from a compressively strained, buried quantum well $Si_{0.7}Ge_{0.3}$ channel p-MOSFET. For $|V_g - V_t| = -V_{ds} = 1.5$ V, I_{ds} the strained-Si surface channel device on a $Si_{0.85}Ge_{0.15}$ virtual substrate exceeds that of the control by 45%, for the strained-Si device on the $Si_{0.8}Ge_{0.2}$ virtual substrate the enhancement is 57% and the buried channel has a 92% enhancement. The extracted effective mobility from long-channel transistors for the buried channel device is over 40% greater than the universal mobility curve for bulk Si p-MOS devices at 0.55 MV/cm vertical effective electric fields. Enhancement in the hole velocity were also demonstrated over the Si control of 23% for the strained-Si on $Si_{0.85}Ge_{0.15}$ virtual substrates, 45% for the strained-Si on $Si_{0.8}Ge_{0.2}$ virtual substrates and 62% for the buried channel devices were measured for an effective channel length of 0.25 μm for a low source-drain bias of -0.1 V. The enhancement over the strained-Si p-MOS devices is only evident when devices with the same effective channel length are compared and this is reversed when constant lithographic or as-drawn gate lengths are compared. The effective channel length was around 0.2 μm longer than the as-drawn or lithographic gate length for all gate lengths below 1 μm which may preclude the use of such buried technology devices as significantly shorter gate-length devices are required to be fabricated to obtain performance enhancements over strained-Si technology.

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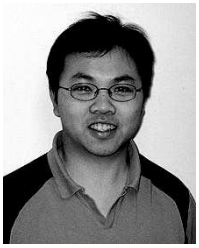

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