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Microfabrication of gold wires for atom guides

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Abstract

Miniaturised atom optics is a new field allowing the control of cold atoms in microscopic magnetic traps and waveguides. Using microstructures (hereafter referred to as atom chips), the control of cold atoms on the micrometer scale becomes possible. Applications range from integrated atom interferometers to the realisation of quantum gates. The implementation of such structures requires high magnetic field gradients.

The motivation of this work was to develop a suitable fabrication process for micromachined high-density current-carrying wires for atom guides. However, the developed process may be used for a variety of applications such as on-chip inductors and microtransformers. In order to realise the micromachined wires for atom guides different designs and fabrication processes were investigated. We discuss the feasibility and the suitability of the fabrication process based on gold sputtering technique to realise such devices. As an alternative we have considered a lower cost technique based on gold electroplating. For the electroplating we used commercial full bright cyanide free gold plating solution (gold sulphite, mild alkaline solution with pH = 9 Gold ECF 60, brightener E3) containing 10 g/dm^3 gold from Metalor.

Some analytical and measurement results of magnetic atom traps are also presented in this paper.

Keywords: Atom guide; Gold wires; High density currents; Sputtering; Electroplating; SPR 220-7; Thick photoresist

1. Introduction

In the last few years considerable interest in the design of microscopic atom traps for manipulating neutral atoms has developed. Miniature atom traps have potential applications in many fields including quantum computing and integrated atom optics. Microfabricated current-carrying wires can produce magnetic fields suitable for trapping atoms that are laser cooled to μK temperatures; this is depicted schematically in Fig. 1. Recently, Bose–Einstein condensed atom clouds have been produced using micrometer-sized atom traps fabricated on chips [1,2]. This paves the way to a field where microelectromechanical systems (MEMS) and atom optics overlap. Microfabrication can bring a significant contribution to this field due to the advanced techniques used to fabricate micron scale structures. The overlap between the two fields is expected to lead to a range of interesting devices for sensing applications and quantum computing.

The purpose of this work is the microfabrication of wires capable of carrying high density currents necessary to create high magnetic field gradients used for atom trapping. The development of a suitable fabrication process for gold wires for atom chips is a challenging task. There are mainly three different techniques that could be considered: gold evaporation, sputtering or electroplating; all having their advantages and disadvantages. The trade-off is cost of fabrication versus ease of fabrication. In this work we discuss the feasibility of gold sputtering technique and electroplating as an alternative.

2. Atom trapping

Neutral atoms with an unpaired electron have a magnetic dipole moment, and interact with magnetic fields. The sign of the interaction depends on the orientation of the dipole with respect to the magnetic field. If the atoms have a

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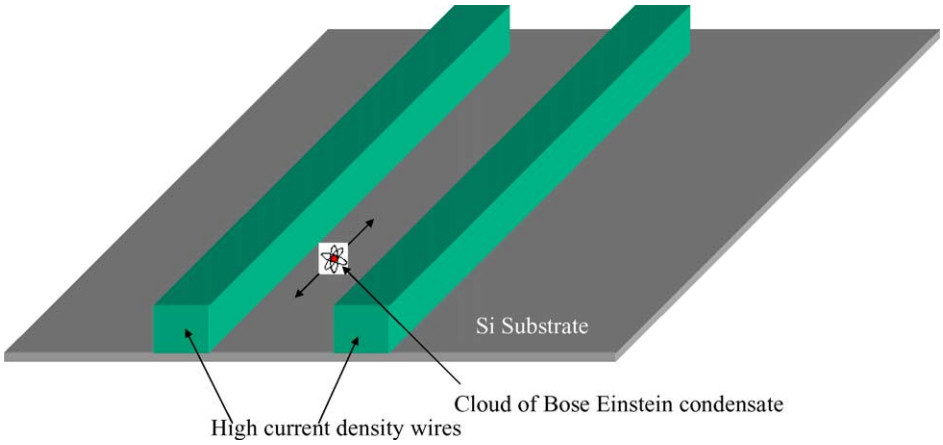

Fig. 1. Schematic representation of an atom cloud in the vicinity of high current density carrying wires.

lower energy in regions of a low magnetic field, they can be trapped and guided using magnetic field minima. Creating these magnetic fields using microfabricated wires on a chip allows the atoms to be trapped and guided close to the surface, and the flexible geometry of the wires allows a wide variety of trapping potentials to be produced. Fig. 2 shows contour plots of the magnetic field produced by two wires showing the minimas of the magnetic field where atoms can be trapped. These simulations were made for three different values of the current. For example, the combination with an external magnetic bias field, two parallel wires carrying a current of a few Amperes allow the creation of a waveguide that can be split and recombined simply by varying the bias field. One target application of this work is an atom interferometer.

The magnetic dipole interaction is quite weak, and hence the atoms must be pre-cooled to <100 mK before they can be trapped. This is achieved using laser cooling techniques. The gold surface in parts of the fabricated atom chips forms a good mirror, which is used to reflect some of the light, used to cool the atoms. Once the chip is loaded, the atoms can be cooled further using radiofrequency evaporative cooling. This allows the atoms to be cooled to 300 nK. At temperatures this low, bosonic atoms such as ^{87}Rb will undergo Bose–Einstein condensation. The resulting atom cloud is a giant "coherent matter wave". Using a simple atom chip based on a single macroscopic wire, we have successfully produced Bose–Einstein condensates of ^{87}Rb containing 5×10^4 atoms. Fig. 3 shows absorption images of atom clouds; the sharp peaks are the signature of Bose–Einstein condensation on a chip. Combining this condensate with the wide variety of magnetic potentials that can be produced by microfabrication techniques will open up many possibilities for coherent control of matter waves; one example is atom interferometry.

Cold atoms trapped on atom chips have already been used as a highly sensitive probe of the magnetic field fluctuations above a conducting wire [3].

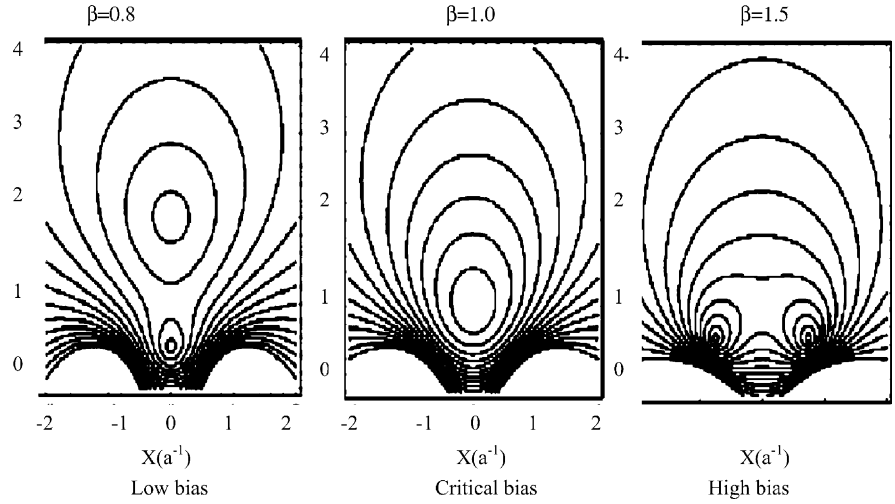

Fig. 2. Contour plot of the magnetic field produced by two wires showing the minimas of the magnetic field where atoms are trapped. These simulations were made for three different values of the current.

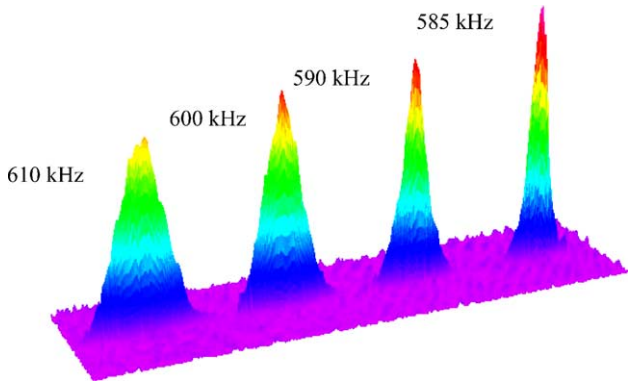

Fig. 3. Absorption images of atom clouds; the sharp peaks are the typical signature of Bose–Einstein condensation on a chip.

3. Fabrication process techniques

3.1. Sputtering technique

The challenge of the fabrication technique is to produce thick, high density current-carrying gold wires. From simulations of the magnetic field a thickness of the gold wires between 5 and 10 μm was found to be suitable. Additionally, the surface of gold wires has to be very smooth since roughness of the surface may cause a non-homogeneous current distribution.

The first fabrication process that was developed in this work is based upon sputtering and wet etching of a thick gold layer. The full fabrication process flow is described in the following:

(1 0 0) silicon wafers (p-type, 17–33 Ω cm resistivity, 100 mm in diameter) were cleaned in fuming nitric acid (FNA) for 10 min, followed by rinsing in de-ionised water and spin-dryed in a nitrogen environment. Next, a thin electrical insulating film of silicon dioxide SiO_2 (600 nm) was deposited by wet oxidation. Then, few hundreds of Angstroms of Cr were sputtered on four different wafers as an adhesion layer. Next, layers of Au with thickness of 3, 5, 10 and 25 μm were deposited on the top.

This was followed by a spin-coating step to deposit standard photoresist (S1818) using a hand spinner. Then, the gold layers were photolithographically patterned with a mask to form the areas for the contacts pads, the gold wires, and the gold mirrors. The mask design is shown in Fig. 4. The four central wires, above which atom clouds can be trapped, were 50 and 100 μm wide, 7 mm long and separated by a gap of 30 μm. The transverse wires were 45 and 90 μm wide and 11 mm long. The exposure was done with a contact mask using a hybrid technology group (HTG) aligner using UV lights source (350–450 nm spectrum, mercury lamp) at 1.6–1.9 mW/cm^2 intensity. The next step was wet chemical etching of Au with aqueous KI_3 solution (4 g KI, 1g I_2 in 40 ml H_2O) and then Cr in a mixture of a ceric ammonium nitrate ($H_8CeN_8O_{18}$) with nitric acid (5 g $H_8CeN_8O_{18}$, 4 ml HNO_3 (70%) in 5 ml H_2O) [4]. The

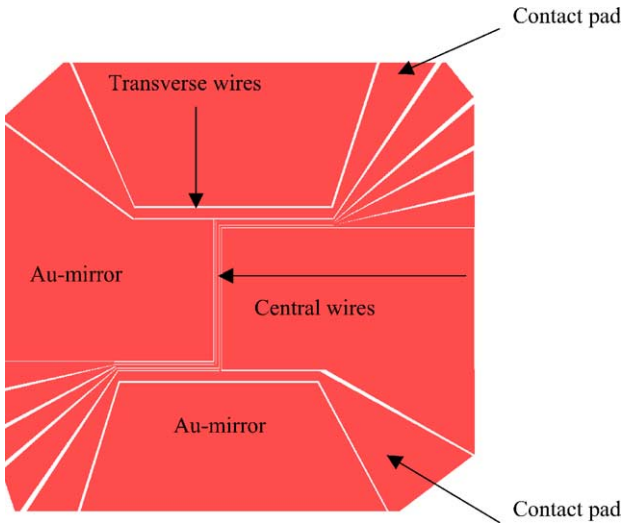

Fig. 4. Mask design used for wire fabrication.

process flow is diagrammatically illustrated in Fig. 5. A first prototype device was fabricated using this technique.

3.2. Electroplating technique

Despite of the fact that a fabrication technique based on sputtering was found to be suitable for our applications, it is a time-consuming and a costly process. Thus, we decided to develop an alternative fabrication technique. Electroplating is a promising technique for the fabrication of MEMS in general. It has a number of significant advantages. First, electrochemical deposition produces a high density of the deposited material in the holes of the template (mould) and leads to volume templating of the structure as opposed to templating of material. As a result there is no shrinkage of the material when the template is removed and no need for further processing steps or the use of elevated temperatures. In consequence, the resulting metal film is a true cast of the template structure and the size is directly determined by the

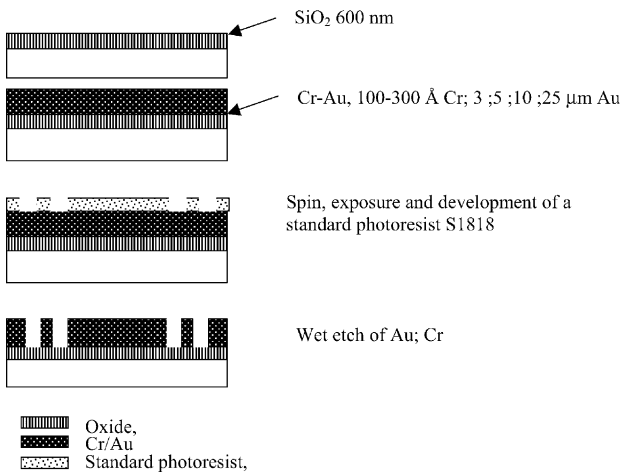

Fig. 5. Fabrication process flow using sputtering technique.

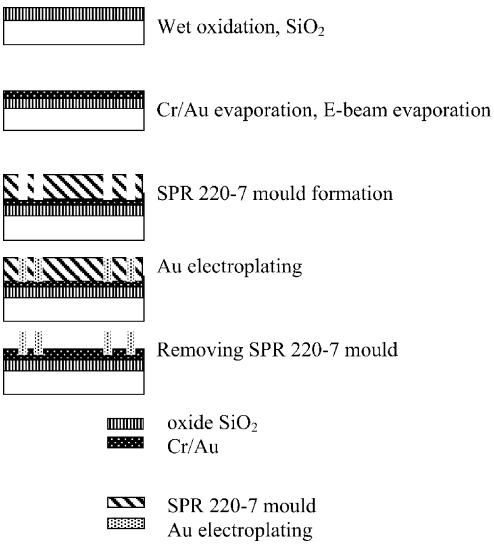

Fig. 6. Fabrication process flow for the gold electroplating test batch.

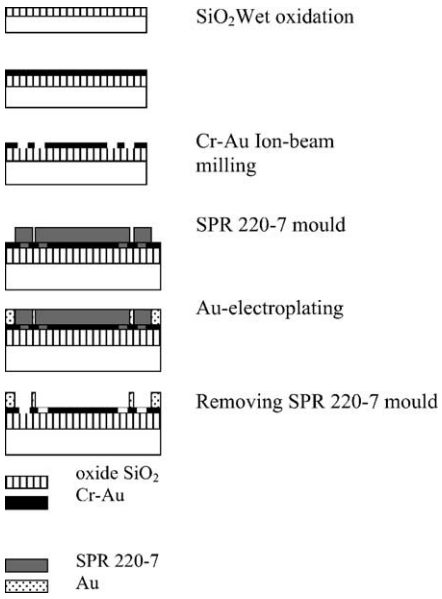

Fig. 7. Fabrication process flow for the gold electroplating and evaporation techniques.

size of the template used. Secondly, electrodeposition can be used to prepare a wide range of materials from both aqueous and non-aqueous solutions under conditions, which are compatible with the template. Thirdly, electrochemical deposition allows fine control over the thickness of the resulting film by controlling of the total charge passed to deposit the film. This is a unique feature of the approach. Various material properties, such as the grain size and surface roughness, can be controlled by the electroplating conditions [5,6].

Fourthly, electrochemical deposition is ideal for the production of thin supported layers for applications such as photonic mirrors since the surface of the electrochemically deposited film can be very uniform [7].

A batch to check the suitability of thick gold electroplated films for atom guides was developed. An important aspect is to find a compatible photoresist with the gold sulphite alkaline plating solution. The process steps are summarised as follow: the same silicon wafers as for the first process were used. After a standard cleaning process a thin layer of Cr/Au (40, 300 nm) was evaporated. The Au layer served as a seed layer for electroplating. In order to make the surface as clean as possible a preliminary cleaning was necessary, which was done by immersing the wafer into IPA solution for 10 min. This was followed by spin-coating of thick positive photoresist SPR 220-7 (up to 14 μm) which later was used as a mould for the gold electroplating [8,9]. This thickness was achieved with a single layer coating to get good contact between the mask and the wafer we had to remove the photoresist edge bead which was formed during the low-speed coating. This was achieved by exposing

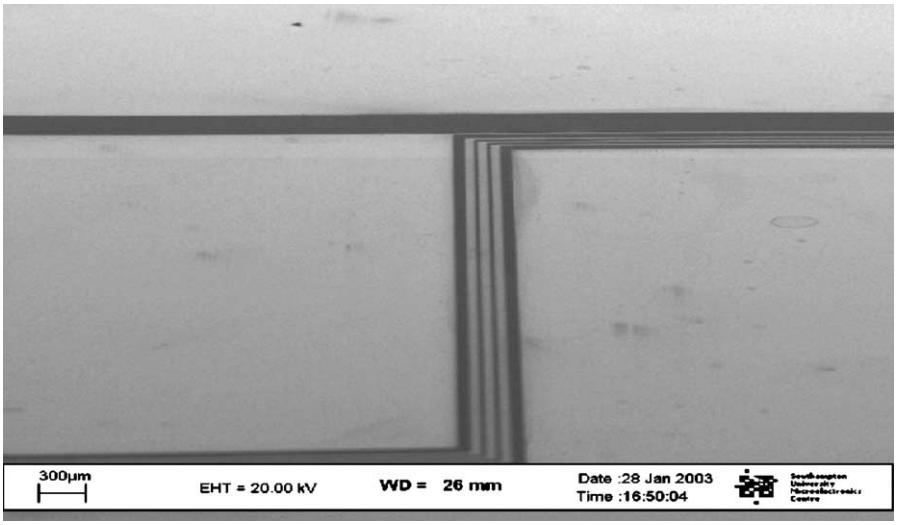

Fig. 8. SEM picture showing the central region the wires structure.

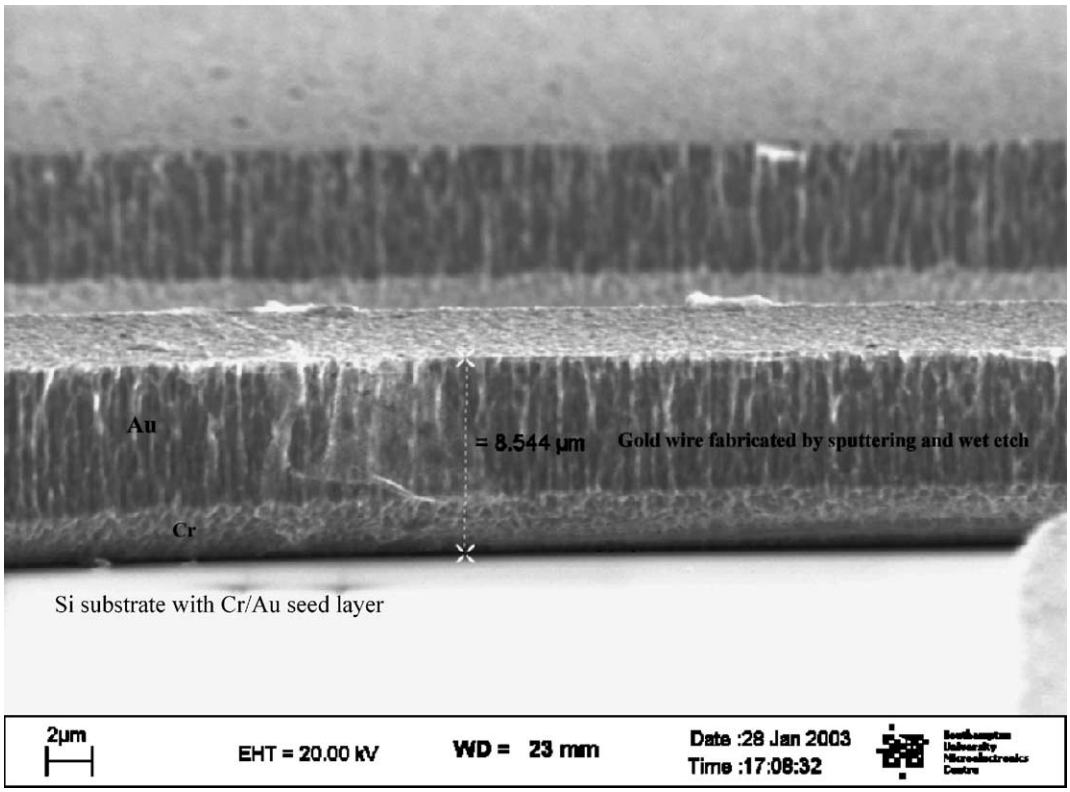

Fig. 9. SEM side view of gold wires fabricated by sputtering.

the edges of the wafer for 700 s and developing for 2 min. The resist was photolithographically patterned with the mask shown in Fig. 4 to define the areas for electroplating. Once the photoresist moulds were fabricated, electroplating of Au was performed without a hardbaking the photoresist since this can cause SPR 220-7 to reflow.

Electrochemical deposition was performed in a thermostatically controlled cell at 25 °C using a conventional

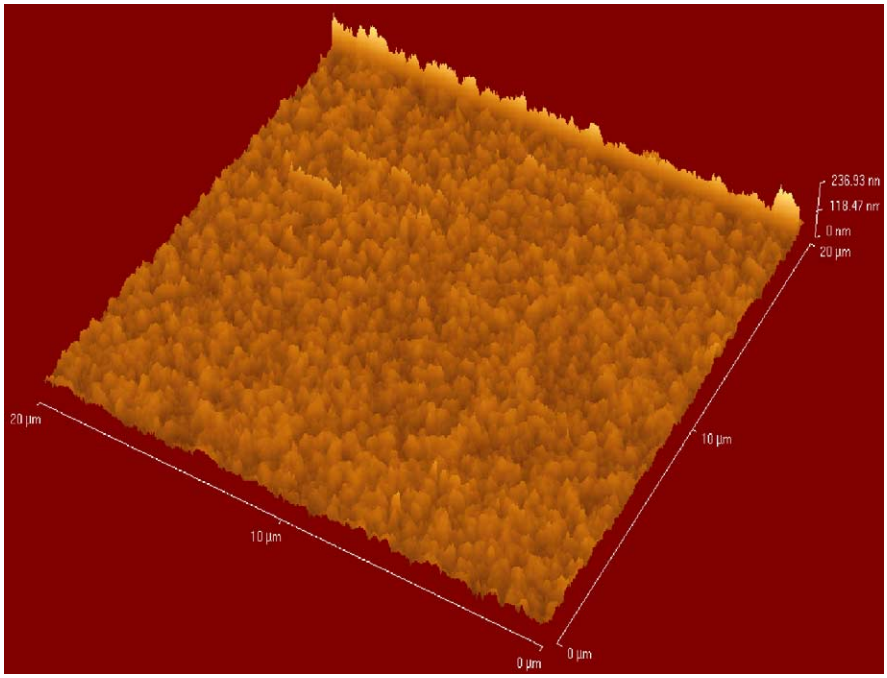

Fig. 10. AFM roughness measurement for gold wires fabricated by sputtering. The r.m.s. roughness is about 16 nm.

three-electrode configuration controlled by an Autolab PGSTAT30 [10]. The gold substrate with the template was the working electrode with a large area platinum gauze counter electrode and a custom-made saturated calomel reference electrode (SCE). We used commercial full bright cyanide free gold plating solution (Gold ECF 60, brightener E3) containing 10 g/dm^3 gold from Metalor. This is mild alkaline solution with pH = 9. Gold films were deposited under potentiostatic conditions at −0.7 V versus saturated calomel reference electrode (SCE). The deposition rate was 7 μm/h with a current density of 1.2 A/dm^2. The SPR 220-7 mould was removed after electroplating. The full process flow is shown in Fig. 6. The gold electroplating bath was compatible with the SPR 220-7 photoresist, which adhered very well to the substrate, so underplating did not occur.

One problem with the described electroplating is that the achievable smoothness is not sufficient for the gold mirrors without further optimisation of the electroplating solution using special additives such as brighteners. For our applications a very smooth mirror surface, which is crucial for realising the optics for the laser cooling of the atom clouds [11]. Consequently, we are developing a two-mask process, which is a combination between the described electroplating technique for the thick gold wires (where the roughness and brightness of surface are not critical on submicron scale) and a "conventional" and easy to realise vacuum evaporation technique for the gold mirrors.

In this process, samples are fabricated using silicon substrates with silicon dioxide as an isolation layer. Then, a thin Au–Cr layer (40, 300 nm) is evaporated and photolithographically patterned using a standard thin photoresist (SPRT 518) in order to define electroplating areas for gold wires, to provide electrical isolation between gold mirrors, gold wires, and contact pads. The same gold layer is used as a seed layer for the gold electroplated wires. This is followed by spin-coating of thick positive photoresist SPR 220-7. Patterning is performed using standard contact photolithography in order to define electroplating areas. Once photoresist moulds are fabricated, electroplating of Au is performed. Removing of the SPR 220-7 mould concludes the process. The process flow is diagrammatically illustrated in Fig. 7.

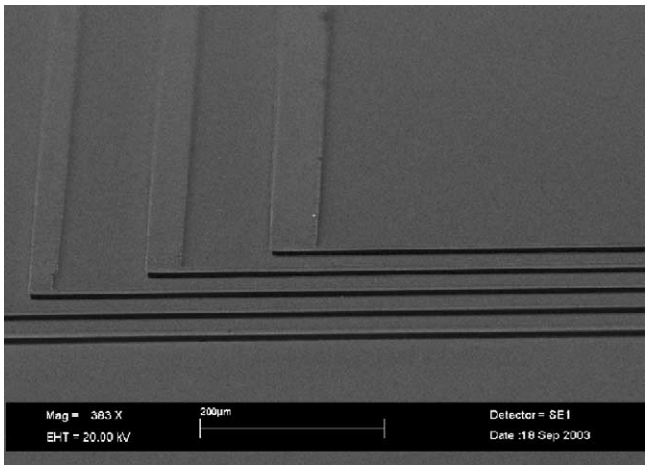

Fig. 11. SEM side view of electroplated 6 μm high gold wires.

4. Fabrication results

The SEM picture in Fig. 8 shows a top view of the atom guide prototype fabricated by the sputtering technique. The dark areas are thick gold wires and the lighter ones are gold mirrors. A SEM side view of the same wires is shown

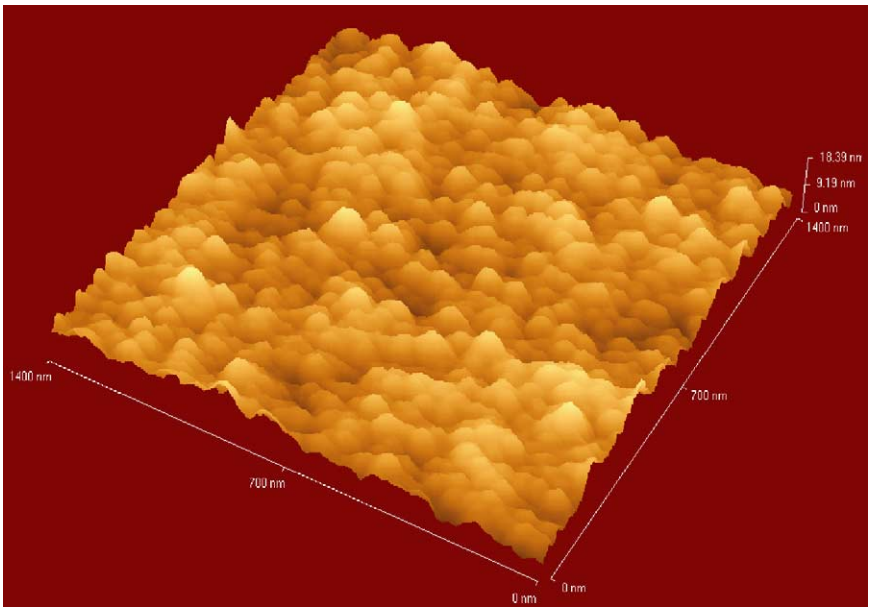

Fig. 12. AFM roughness measurement for gold wires fabricated by electroplating. The r.m.s. roughness is about 2.3 nm.

in Fig. 9; it is obvious that the thickness is uniform along the wires. This is important for uniform current distribution which is required to obtain a high current density in the wire necessary for an atom guide. Another requirement is to have a low surface roughness and a uniform grain size in the wire. These microstructural aspects were investigated using an atomic force microscope. Fig. 10 shows a 20 μm × 20 μm AFM picture of the wire surface. The r.m.s. surface roughness of gold wires is about 16 nm, which is expected to be low enough to make it suitable for atom trapping applications. The grain size was estimated to be approximately 800 nm and its distribution is clearly uniform across the scanned area.

Fig. 11 shows a SEM picture of gold 6.1 μm thick electroplated wires after removal of the photoresist. From the picture it can be seen that the wires fabricated in this low-cost alternative technique were well-defined and uniform in thickness.

AFM scans were performed at different locations across the wire surface. Fig. 12 shows a 1.4 μm × 1.4 μm area. The r.m.s. surface roughness is about 2.3 nm which was even better compared to the sample fabricated by the sputtering technique. The scan also shows that the sample has a finer grain structure of approximately 90 nm.

5. Conclusion

We fabricated gold wires for atom chips using a sputtering and an electroplating technique. We have compared the microstructural properties of the wires fabricated by both techniques. The grain size of the electroplated wires was approximately 10 times smaller than in the sputtered wires. Also, the surface roughness was smaller using the electroplating techniques. From these findings and considering the low-cost and simplicity of the electroplating technique, we decided to develop this process further to fabricate more complex atom guides for an atom interferometer. Currently, the fabricated wires are being tested by loading a Bose–Einstein condensate atom cloud and moving it in the magnetic confinement field along the wire. This will allow us to develop a sensor based on an atom interferometer.

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Biographies

E. Koukharenko received her Diploma in chemical engineering and technology from Chemical Technological University of Minsk (Republic of Belarus) in 1995. She had her Master Diploma in physical chemistry of condensed matter from University of Montpellier II in 1996. Between 1997 and 2000 she jointly attended the Belarusian State University of Minsk and University of Montpellier II (France) for her PhD working on materials for thermoelectric applications. She then has been employed as a research fellow at the Microfabrication Centre at the School of Electronics and Computer Science, Southampton University since 2001. Her research interest include research and development work on different kind of thick photoresists, microfabrication of 3D metallic and non metallic-structures and process development focused on fabrication of MEMS for different sensors applications. She is interested in surface and microstructure characterisation of different materials.

Z. Moktadir received his MSc (1991) in materials science from the University of Montpellier France and his PhD in microsystems technology from Toulouse University (France). He was a JSPS fellow at Nagoya University Japan for the period 1999 and 2001. He then joined MESA+ research institute at the University of Twente (The Netherlands) before joining the Department of Electronics and Computer Science at the University of Southampton, UK where he is a research fellow. His research interests are in the area of micro/nanofabrication, Thin film growth/etching mechanisms and nanostructures and surface morphology characterization.

M. Kraft was born in Nürnberg, Germany, in 1966 and received his Dipl.-Ing. (Univ.) in electrical and electronics engineering from the Friedrich Alexander Universität Erlangen-Nürnberg in 1993. In the same year he joined the Nonlinear System Design Group at Coventry University, UK where he worked on the design of a digital micromachined accelerometer and received his PhD in 1997. He then spent 2 years at the Berkeley Sensors and Actuator Centre, University of California at Berkeley, USA, working on the design of integrated micromachined gyroscopes. He is currently employed as a lecturer at the Microelectronics Centre, School of Electronics and Computer Science at Southampton University, UK. His principle interests include micromachined inertial sensors, MEMS sensors and actuators, intelligent control systems for MEMS devices and electronic circuit design.

M.E. Abdelsalam received his MSc in electroanalytical chemistry, Tanta University, Egypt (1995). Then he moved to the electrochemistry group, Southampton, UK, where he received his PhD in microelectrodes and

their fabrications, characterisations and applications (2000). He spent 1 year as a postdoctoral research fellow, School of Chemistry, University of Southampton, working on sonoelectrochemical destruction of organic pollutants (2001–2002). Then moved to Prof. P. Bartlett group, Southampton, where he is working in the field of electro-material science. His research interests are in the field of microelectrodes and electrochemical fabrication of macroporous materials that have striking optical and magnetic properties.

D.M. Bagnall was born in 1966 in Stoke-on-Trent, England. He studied for his BEng (in Electronics) and his PhD at Salford University between 1985 and 1993. He joined the Department of Physics and Applied Physics at Strathclyde University, Glasgow in 1993, the Institute of Materials Research, Tohoku University, Japan in 1995 and RIKEN, Sendai, Japan in 1997. Since 1999 he has been a joint lecturer between electronics and computer science, and physics at Southampton University. His research interests are based around the exploration of the limits of lithographic and deposition techniques in the development of new silicon based optoelectronic devices.

C. Vale received his BSc (Hons) in physics and computing in 1995 and his PhD from Victoria University, Melbourne, Australia in 2000. He then was a postdoctoral research fellow at the University of Sussex from 1999 to 2002. He is currently employed as a postdoctoral research fellow at the University of Queensland, Brisbane, Australia. His main research interests are Bose–Einstein condensates and coherent atom optics in magnetic microtraps.

M.P.A. Jones received his MSc in physics from the University of Bristol in 1999 and his DPhil in physics from the University of Sussex in 2003. He is currently employed as a postdoctoral research at Imperial College, London. His research interests are the physics of ultracold atoms and quantum information.

E.A. Hinds was born in 8 September 1949; Cardiff, United Kingdom and received BA (physics) in Jesus College, Oxford University, England in 1971. He had his PhD (physics) from Oxford University in 1974. He then worked at Columbia University as a research associate in the Astrophysics Laboratory in 1975–1976. He then was employed as a research associate and lecturer at Yale University (1976–1977) and inaugurated as assistant professor of physics in 1977. He then was promoted to associate professor of physics (1981–1983). He was director of undergraduate studies, 1984–1985; 1986–1990; 1994–1995. He became a professor of physics in 1988 at Yale University. In 1995 he was employed as professor of experimental physics by the University of Sussex where he was a founder and director of SCOAP 1995–2002 and chair of the research strategy group 1999–2002. Since October 2002 he has been professor of physics at Imperial College, London.