INSTITUTE OF PHYSICS PUBLISHING JOURNAL OF MICROMECHANICS AND MICROENGINEERING

J. Micromech. Microeng. **14** (2004) S114–S122 PII: S0960-1317(04)77980-2

Modelling and analysis of a MEMS approach to dc voltage step-up conversion

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Received 18 March 2004, in final form 5 August 2004
Published 20 August 2004
Online at stacks.iop.org/JMM/14/S114
doi:10.1088/0960-1317/14/9/020

Abstract

This paper studies the principle of a novel voltage step-up converter based on a micromachined variable parallel-plate capacitor in combination with an electrostatic actuator. Electrical equivalent circuit and system-level SIMULINK models have been developed. Based on these models, an analysis of design parameters and expected device performance has been performed to serve as a starting point for a prototype implementation. Possible areas of application are self-powered, stand-alone sensing systems, aerospace applications and any kind of electrostatic or piezoelectric MEMS devices in general.

1. Introduction

A number of micro-devices could benefit from a fully integrated MEMS voltage converter that steps up their usually low dc input voltage to higher levels. For example, the efficiency of micro-resonators can be increased by using a high dc bias voltage [1] and electrical noise levels in capacitive accelerometers can be reduced in a similar fashion [2]. High dc voltages are also required in space applications such as scientific instruments [3] and micro-propulsion units [4] aboard satellites. The relatively low output voltage of solar panels and the trend towards microsatellites create a strong need for miniaturized voltage converters.

The stepping up of dc voltages is usually performed by either boost converters or charge pumps. Boost converters rely on an electrical inductance and are therefore difficult to integrate. Charge pumps [5] consist of a number of capacitors interconnected by MOS diodes and are widely used in integrated circuits. However, the amount of required capacitors increases linearly with the desired voltage multiplication factor, thus requiring much wafer surface area.

To explore new methods of direct dc-to-dc voltage conversion, this paper proposes a micro-electro-mechanical voltage converter. The method exploits the interdependence of voltage and capacitance in a micromachined parallel-plate capacitor of variable capacitance. The voltage of a charged and electrically isolated capacitor can be increased by reducing the capacitance while preserving its charge. This capacitance variation can be achieved mechanically by moving one of the electrodes with an electrostatic micro-actuator. By periodically switching between two defined capacitance values, a bistable MEMS voltage converter can be realized.

Since the absolute capacitance of the micromachined variable capacitor is expected to be very low, such a conversion device will have a high output impedance and will thus be mainly suitable for high voltage generation at very low output power, i.e. for driving purely capacitive loads.

The voltage conversion approach described here is novel and very little previous work exists about MEMS voltage converters. Approaches to replace the inductor in boost converters by a micromachined variable capacitor have been described [6, 7]. In contrast, the device presented in this paper resembles the charge pump circuit but reduces the number of capacitor stages to one.

2. Operating principle

The proposed MEMS voltage converter consists of a variable capacitor which is mechanically coupled to a micro-actuator. The operating principle is illustrated in figure 1: (*a*) shows the charging and conversion states of the capacitor and (*b*) gives a timing diagram for the switch control signals S_1 and S_2 as well

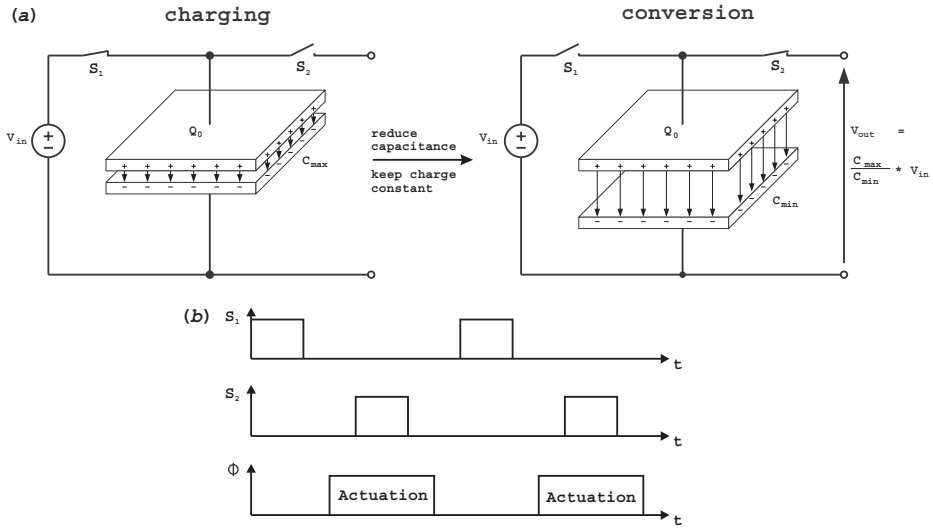

Figure 1. Operating principle of the MEMS dc converter. (*a*) Charging and conversion states (intermediate isolated states not shown). (*b*) Control signals for active reduction (non-overlapping clocks S_1 and S_2, actuator clock Φ).

as the actuator control signal Φ. The capacitor is first brought into its position of maximum capacitance $C_{\max}$ and charged to the input voltage. To keep this charge Q_0 constant, the input switch S_1 is opened. Then, the capacitor plates are moved by the actuator in order to decrease the capacitance from $C_{\max}$ to $C_{\min}$. The voltage over the capacitor electrodes increases by the voltage multiplication factor $M = C_{\max}/C_{\min}$ and the high voltage can be accessed at the output via the second switch S_2. This set-up bears a resemblance to switched capacitor circuits and can be analysed in a similar fashion. However, in the present case the switched capacitor is not used to emulate a resistor but varied in capacitance in order to shift its stored charge from low to high potential.

The capacitance variation can either be based on a variable electrode gap (transverse structure, as seen in figure 1) or be achieved by a change in effective electrode area (comb structure). Both approaches are suitable to serve both as capacitor and actuator. This leads to four possible capacitor–actuator combinations and two different modes of operation have been identified for each combination. (i) In 'active reduction' mode, the capacitor is charged which causes it to move into $C_{\max}$ position automatically. The micro-actuator then reduces the main capacitance thus performing the conversion. (ii) In the 'active increase' mode, the electrostatic actuator is used first to increase the main capacitance and at the same time to load the compliant mechanical suspension of the structure. The capacitor is charged and subsequent deactivation of the actuator prompts the mechanical suspension to reduce the main capacitance and thus increase the voltage. In this case, the actuator has to be controlled by a signal $\overline{\Phi}$ inverse to the one used in active reduction mode.

Crucial to the proper operation of the device is the condition of constant charge on the capacitor when its capacitance is reduced. This is ensured by a switching element between input voltage and capacitor and another switch towards the output. Micromechanical switches are well known in the literature [8], mainly for microwave applications. An adapted switch design, integrated with the voltage converter, would have the advantage of very low forward voltage drop and good electrical isolation.

As an alternative, diodes could be used instead of the switches S_1 and S_2: diodes with the cathode pointing towards the output would ensure that charge only flows in the desired direction towards the output. When the capacitor voltage increases above the input voltage, the input diode is reverse biased thus isolating the capacitor and ensuring constant charge. As an advantage, diodes do not require active control thus reducing the number of clock signals to only the one for the actuator. However, diodes have a forward voltage drop that would adversely affect the achievable multiplication factor and thus, this method will not be further considered.

3. Equivalent circuit model

The schematic in figure 2(*a*) contains the components of a complete voltage converter. The clock signals run at a frequency of f_{clk} and are activated in a pattern as given in figure 1(*b*). Any constant capacitances parallel to the main capacitor have been modelled as a lumped element C_p. In a practical application, the actuator voltage V_{act} will be supplied from the same input voltage V_{in}. Also, the circuit will drive an output load of capacitor C_L and resistor R_L.

3.1. Behaviour of the output voltage

The electronic behaviour of the MEMS voltage converter is similar to the classic charge pump [5]. The system pumps charge into the load capacitor C_L in which the amplified output voltage gradually builds up. In each clock cycle, the output voltage is highest in the instant when S_2 is switched on and charge is shared between $C(x)$, C_p and C_L. The voltage then linearly decreases as C_L is discharged over R_L. The value $V_L(n)$ of this peak voltage in the nth clock cycle after start up has been found to be

$$V_L(n) = \left(M + \frac{C_p}{C_{\min}}\right) V_{\text{in}} \times \left[B_1^n \left(\frac{C_{\min}}{C_{\min} + C_L} - B_2\right) + B_2\right] \tag{1}$$

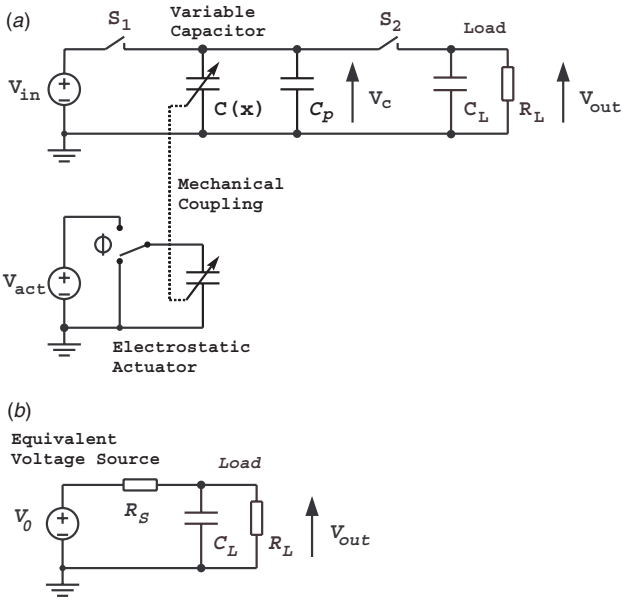

Figure 2. (*a*) Electrical equivalent circuit. (*b*) Voltage source representation.

with the abbreviations

$$B_1 = \frac{R_L C_L f_{\text{clk}} - 1}{R_L (C_{\min} + C_L + C_p) f_{\text{clk}}}$$

$$B_2 = \frac{R_L C_{\min} f_{\text{clk}}}{R_L (C_{\min} + C_p) f_{\text{clk}} + 1}.$$

For increasing n and because of $B_1 < 1$, the output voltage reaches a stationary value

$$V_{\text{out}} = V_L(n \to \infty) = \left(M + \frac{C_p}{C_{\min}}\right) \frac{R_L C_{\min} f_{\text{clk}}}{R_L (C_{\min} + C_p) f_{\text{clk}} + 1} V_{\text{in}}. \quad (2)$$

The system needs a certain amount of time to reach this stationary output. This rise time T_r, defined as the time required to get V_L to within a fraction p of V_{out}, is given by

$$T_r = \frac{\log(-pB_2[C_{\min}/(C_{\min} + C_L) - B_2]^{-1})}{\log(B_1) \cdot f_{\text{clk}}}. \quad (3)$$

After the rise time, when the system is in its steady state, there remains a ripple voltage V_R:

$$V_R = \frac{V_{\text{out}}}{R_L C_L f_{\text{clk}}}. \quad (4)$$

At the rising edge of S_2 the output voltage peaks at V_{out} and then decreases to $V_{\text{out}} - V_R$ over one clock period until S_2 is activated again. The amplitude of this ripple is frequency dependent and is reduced for increasing time constants $R_L \times C_L$ of the load.

To understand the frequency behaviour of these characteristics, figure 3 shows the evolution of the effective multiplication factor $M_e = V_{\text{out}}/V_{\text{in}}$ for different values of $C_{\min}$ and C_p.

For the same frequency range, figure 4 gives the rise time T_r and the output ripple V_R for various parameter sets.

3.2. Equivalent voltage source

The circuit can be represented as an equivalent voltage source as seen in figure 2(*b*). Fitting equation (2) to this voltage source yields expressions for open-circuit voltage V_0 and internal resistance R_S:

$$V_0 = \frac{MC_{\min} + C_p}{C_{\min} + C_p} \times V_{\text{in}} \quad (5)$$

$$R_S = \frac{1}{(C_{\min} + C_p) f_{\text{clk}}}. \quad (6)$$

It is expected that $C_{\min}$ will be of the order of 1 pF. The maximum clock frequency is limited by the mechanical system

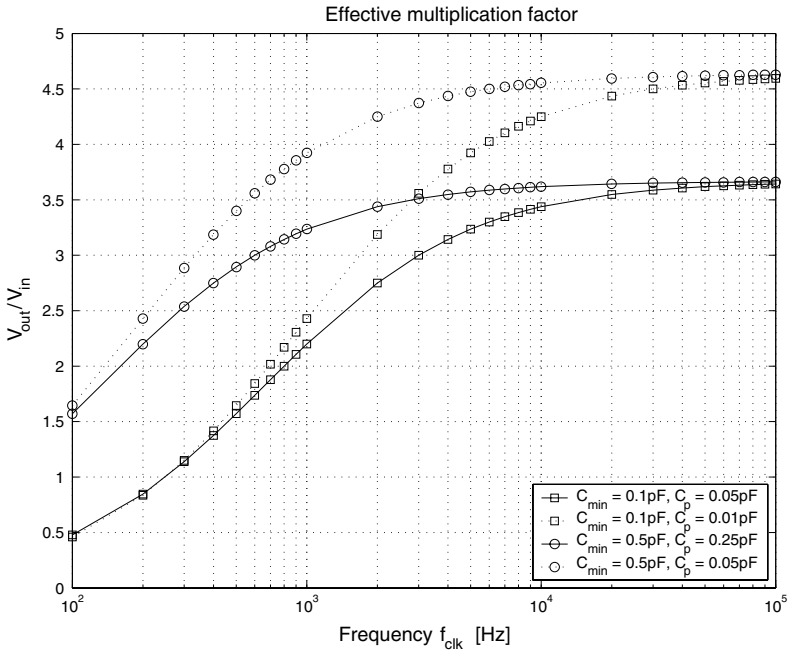

Figure 3. Effective multiplication factor for $M = 5$ and $R_L = 10\ \text{G}\Omega$.

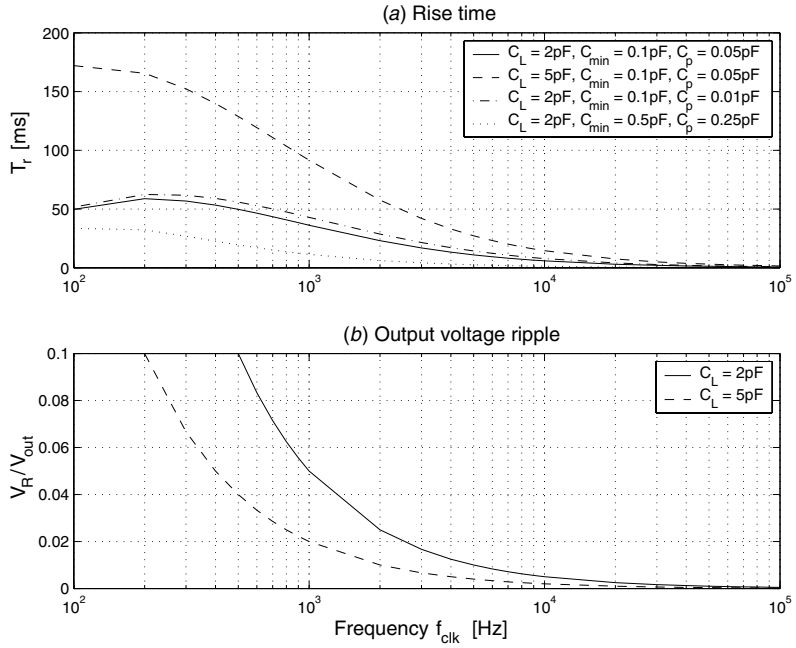

Figure 4. (*a*) Rise time and (*b*) relative ripple voltage for $M = 5$ and $R_L = 10\,\mathrm{G}\Omega$.

and will be of the order of $1 \ldots 10$ kHz while C_p is expected to be of the same order of magnitude as $C_{\min}$. This results in resistance values around $1\,\mathrm{G}\Omega$ for R_S. Because of this very high output impedance, the load resistance R_L has to be even higher for an effective voltage multiplication, which renders the system suitable for purely capacitive loads only.

3.3. Power output and efficiency

The power output to the load is given by

$$P_{\text{out}} = \frac{R_L}{(R_L + R_S)^2} \times V_0^2 = \frac{V_0^2}{R_L} \times \left(\frac{R_L(C_{\min} + C_p) f_{\text{clk}}}{R_L(C_{\min} + C_p) f_{\text{clk}} + 1} \right)^2 . \tag{7}$$

The maximum power

$$P_{\max} = \frac{(C_{\min} + C_p) f_{\text{clk}}}{4} \times V_0^2 \tag{8}$$

is obtained if $R_L(C_{\min}+C_p) f_{\text{clk}} = 1$ and in this case the output voltage is $V_{\text{out}} = \frac{1}{2} V_0$.

The input power consists of two parts. Firstly, the power P_c used to charge the variable capacitor:

$$P_c = \frac{V_0^2}{R_L} \times \frac{R_L(C_{\min} + C_p) f_{\text{clk}}}{R_L(C_{\min} + C_p) f_{\text{clk}} + 1}. \tag{9}$$

Secondly, the power P_a consumed by the electrostatic actuator:

$$P_a = \tfrac{1}{2} C_a V_{\text{act}}^2 \, f_{\text{clk}} \tag{10}$$

where C_a is the maximum capacitance of the actuator when it is fully switched on. This parameter depends on the system topology and dimensions; example values will be given in section 5. The actuator voltage is considered to be provided by the system input voltage such that $V_{\text{act}} = V_{\text{in}}$.

The power efficiency of the device can thus be computed as

$$\eta = \frac{P_{\text{out}}}{P_c + P_a} = \left(\frac{R_L(C_{\min} + C_p) f_{\text{clk}}}{R_L(C_{\min} + C_p) f_{\text{clk}} + 1} \right)^2 \times \left[\frac{R_L(C_{\min} + C_p) f_{\text{clk}}}{R_L(C_{\min} + C_p) f_{\text{clk}} + 1} + \frac{R_L C_a f_{\text{clk}}}{2} \left(\frac{C_{\min} + C_p}{M C_{\min} + C_p} \right)^2 \right]^{-1} . \tag{11}$$

To visualize these equations for power output and efficiency, figure 5 shows the frequency behaviour for two different multiplication factors and two different values of $C_{\min}$. The values for C_a have been taken from the examples given in section 5.

4. SIMULINK modelling

A system-level SIMULINK library has been created to model the converter subsystems and to simulate complete system behaviour. The models are similar to those described in [9] but have been created in a modular fashion to facilitate the simulation of different system set-ups.

The capacitors have been modelled as transducers that transform an electrical input current and a mechanical coordinate into an electrostatic force. Figure 6 shows the model for the transverse capacitor which has the parameters of electrode area A_a and parasitic capacitance C_p. The input current I is accumulated in the model's internal state variable Q_t which represents the total charge stored on the two capacitors $C(x)$ and C_p. The electrode gap g_c is the other input of the system and determines the current capacitance $C(x)$. The fraction of Q_t which is stored on the main capacitance, i.e. the effective charge, is computed and used to find the resulting electrostatic force F_e and voltage V_c which are the main outputs of the model. The comb capacitor model is shown

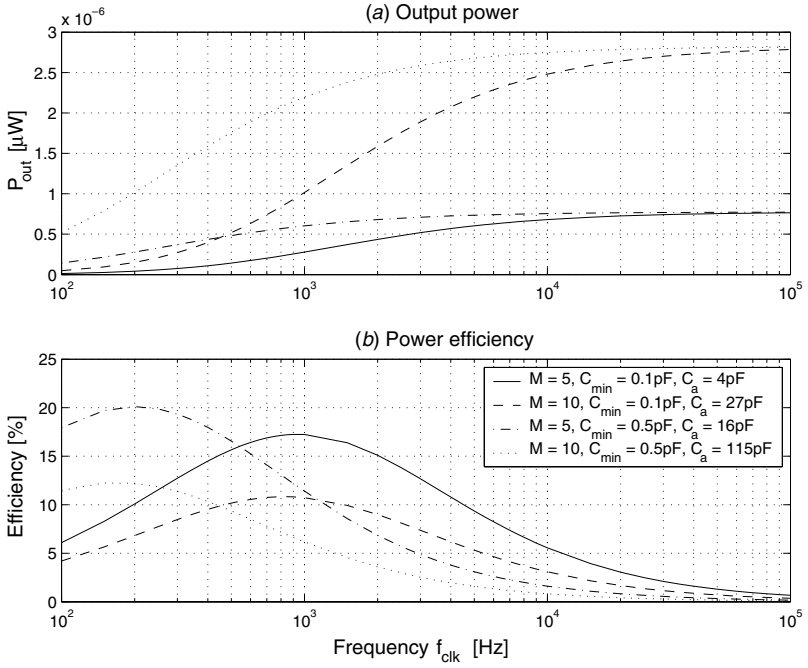

Figure 5. (*a*) Output power and (*b*) power efficiency for $R_L = 10\,\mathrm{G\Omega}$ and $V_{\mathrm{in}} = 24\,\mathrm{V}$.

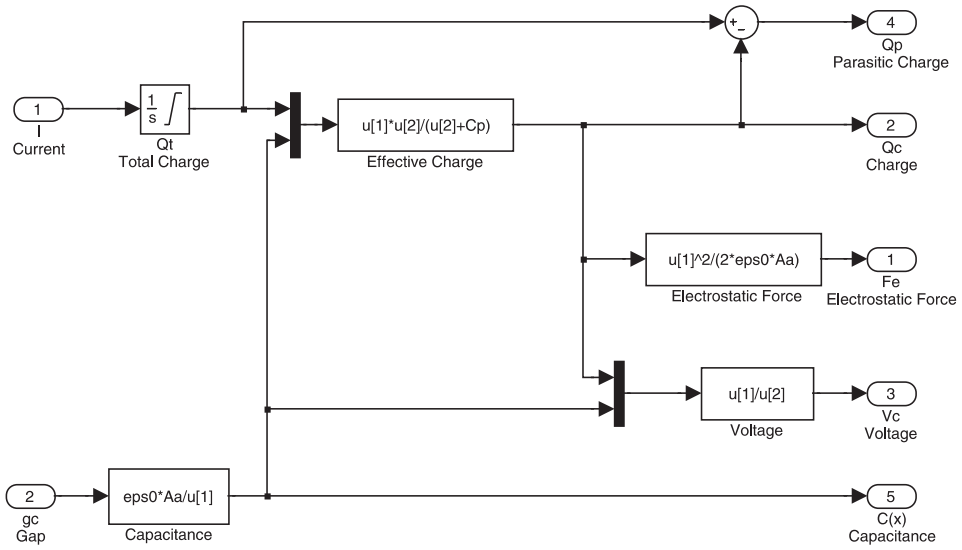

Figure 6. SIMULINK model of the transverse capacitor.

in figure 7 and has the electrode overlap w_c as its geometrical input. The model parameters are the number of electrode fingers N, electrode thickness t, the constant gap g_c and the parasitic capacitance C_p. The structure of this model is very similar to the transverse case. For the electrostatic actuators, the stored charge does not have to be explicitly known and thus, a simplified voltage-controlled model was used.

The electromechanical coupling and compliant suspension of the system is implemented as a mass–spring–dashpot model as shown in figure 8. In addition to the parameters for mass m, spring constant k and damping coefficient b, the model also has geometrical parameters for minimum displacement $x_{\min}$, maximum displacement $x_{\max}$ and at-rest displacement x_0. The displacement limitation is implemented in the displacement limit controller block which contains comparators and some logic to model inelastic collision with a bumper structure in analogy to the description in [9]. For the particular set-up of a bistable system in active reduction mode, these displacement limits are necessary to define the two capacitance values between which the system operates. For active increase mode, only the lower limit is used.

Using the switch blocks in SIMULINK, the models could be put together in the desired topology to form the MEMS voltage converter. An output block representing load capacitance and resistance has been added to obtain a complete model of the circuit from figure 2(*a*).

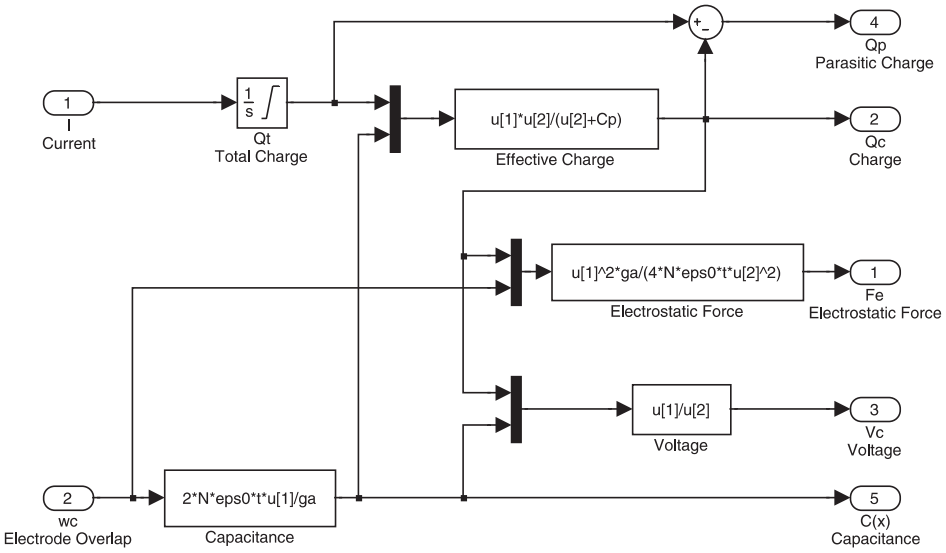

Figure 7. SIMULINK model of the comb capacitor.

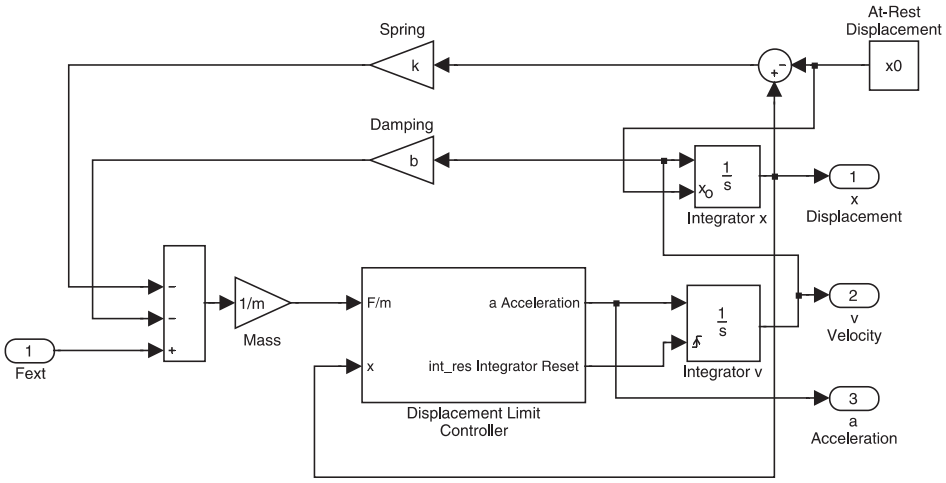

Figure 8. SIMULINK model of the mass–spring–dashpot system.

5. Design analysis

5.1. Case study of system dimensions

In order to compare the different element combinations and modes of operation, case studies have been undertaken by analytical estimates and simulations using the models described before. The calculations were based on the micromachining process described in section 6 with a silicon structure thickness of $t = 60\,\mu$m, a minimum trench width of $g_c = 3.5\,\mu$m and a lithography resolution of $g_{\min} = 1\,\mu$m. Capacitance values for $C_{\min}$ of 0.1 pF and 0.5 pF have been used together with the assumption that the parasitic capacitance $C_p = 0.5C_{\min}$. The input voltage was $V_{\text{in}} = 24$ V as this represents a typical value for satellite solar panels.

For the active reduction mode, the at-rest position of the mechanical system has to be between the two displacement limits. Its exact location has an influence on system speed and actuator size: placed close to the $C_{\max}$ position, the system is charged very rapidly but requires a strong actuator, and vice versa.

In the case of active increase, the system enters harmonic oscillations when it is released from its maximum capacitance position. The at-rest displacement has to be determined in such a way as to let the oscillation amplitude exactly reach the minimum capacitance position. This was done by computing the stored energy which must be the same at both limit positions of the oscillations.

In both modes, the required size of the actuator was found from an analysis of the electrostatic and mechanical forces in the system. Transverse actuators are characterized by their electrode area A_a and minimum gap $g_{\min} = 1\,\mu$m while comb drives are defined by finger number N_a, finger gap $g_c = 3.5\,\mu$m and the minimum finger overlap $w_{\min}$, which was chosen to be $5\,\mu$m.

Table 1 shows the design parameters for a number of cases. For a set of parameters M, $C_{\min}$ and the resulting actuator size, the maximum clock frequency and effective multiplication factor $M_e = V_{\text{out}}/V_{\text{in}}$ have been determined via simulations using the models described before. Systems with a comb capacitor have been studied as well but all of them turned out

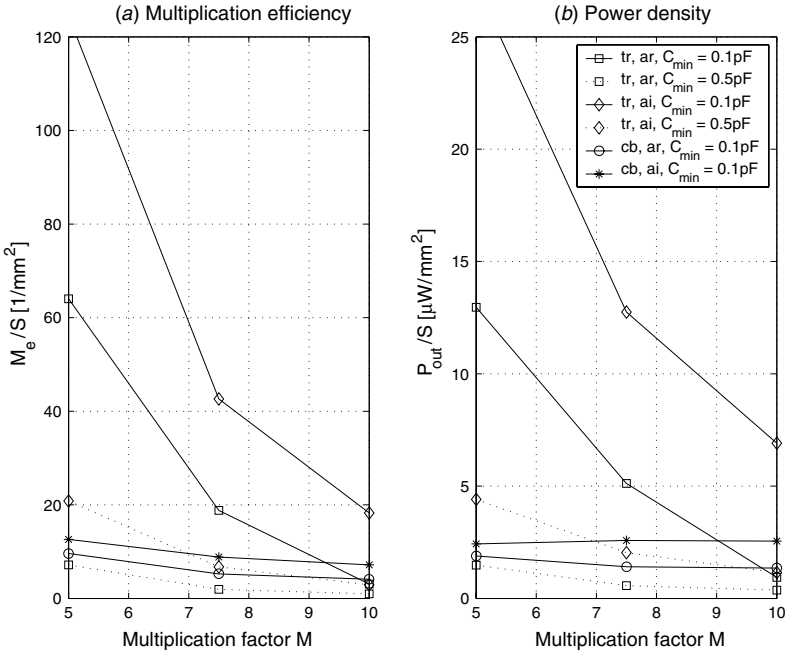

Figure 9. Performance measures for the systems from table 1 (tr = transverse actuator, cb = comb-drive, ar = active reduction, ai = active increase).

Table 1. Design parameters for transverse capacitor systems.

System	M	$C_{\min}$ (pF)	f_{clk} (kHz)	M_e	A_a (mm)^2	C_a (pF)	Surface S (mm)^2
Transverse actuator	5.0	0.1	12.0	3.5	0.65	6	0.05
'active reduction'	5.0	0.5	6.0	3.6	6.20	55	0.50
	7.5	0.1	5.0	4.7	2.00	17	1.25
	7.5	0.5	2.5	5.1	20.50	181	2.60
	10.0	0.1	2.0	5.3	9.90	88	1.70
	10.0	0.5	1.5	6.4	39.20	347	6.50
Transverse actuator	5.0	0.1	20.0	3.3	0.45	4	0.03
'active increase'	7.5	0.1	20.0	5.1	1.38	12	0.12
	10.0	0.1	7.0	6.2	3.10	27	0.34
					N_a		
Comb-drive actuator	5.0	0.1	8.0	3.4	1762	5	0.35
'active reduction'	7.5	0.1	5.0	4.7	3616	13	0.90
	10.0	0.1	3.0	5.7	4440	19	1.40
Comb-drive actuator	5.0	0.1	18.0	3.5	2611	11	0.28
'active increase'	7.5	0.1	12.0	5.0	4375	22	0.57
	10.0	0.1	8.0	6.7	6208	36	0.94

to be inferior to the transverse capacitor systems and therefore have been left out.

The last column of table 1 gives an estimate of the wafer surface area S for each system based on the fabrication process from section 6. As a measure of performance, two ratios have been visualized in figure 9. Part (a) shows a 'multiplication efficiency' M_e/S as a measure of how much wafer surface is needed to achieve a certain multiplication factor. Part (b) shows the power density P_{out}/S for each device. The lower multiplication factors are clearly dominated by transverse actuator systems with the active increase mode being superior to active reduction. However, their performance rapidly decreases with increasing M while the comb-drive systems show less dependence on M. The data also show that an increase in minimum capacitance $C_{\min}$ reduces the maximum operating frequency and renders the resulting device less area efficient.

The minimum gap $g_{\min}$ of the capacitor can be seen as a measure for the miniaturization of the system. Four different values of $g_{\min}$ are shown in table 2 from which it can be seen that the system becomes faster and more efficient if it is miniaturized.

5.2. Simulation results

Figure 10 shows a simulation of the system listed in the topmost row of table 1. The first five clock cycles after startup are shown. Because of the parasitic capacitance, there is a reduction of stored charge when the actuator is switched on. The charge is then shared between $C(x)$, C_p and C_L when S_2 is activated and the output voltage V_L builds up step by step.

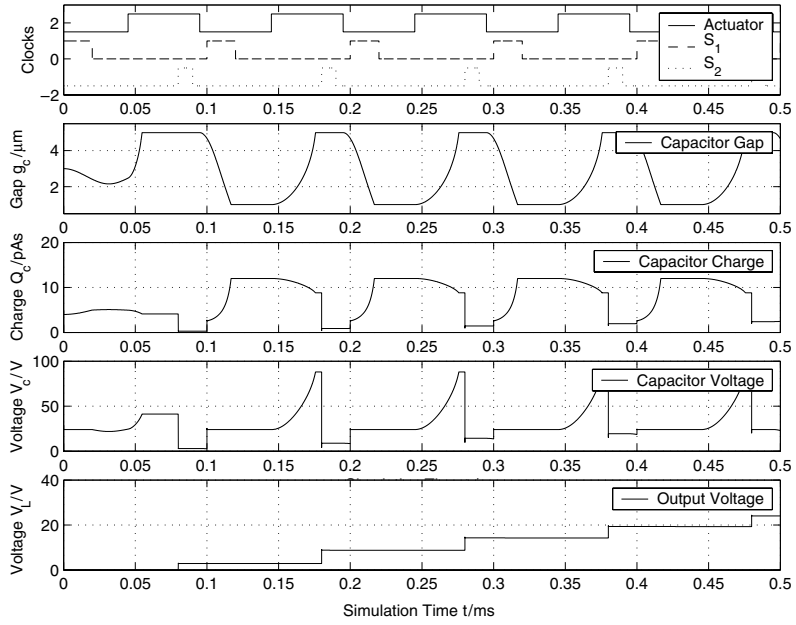

Figure 10. Simulation of the system with transverse capacitor, transverse actuator, active reduction. Startup and first five clock cycles for $M = 5$, $C_{\min} = 0.1$ pF, $f_{\text{clk}} = 10$ kHz, $V_{\text{in}} = 24$ V.

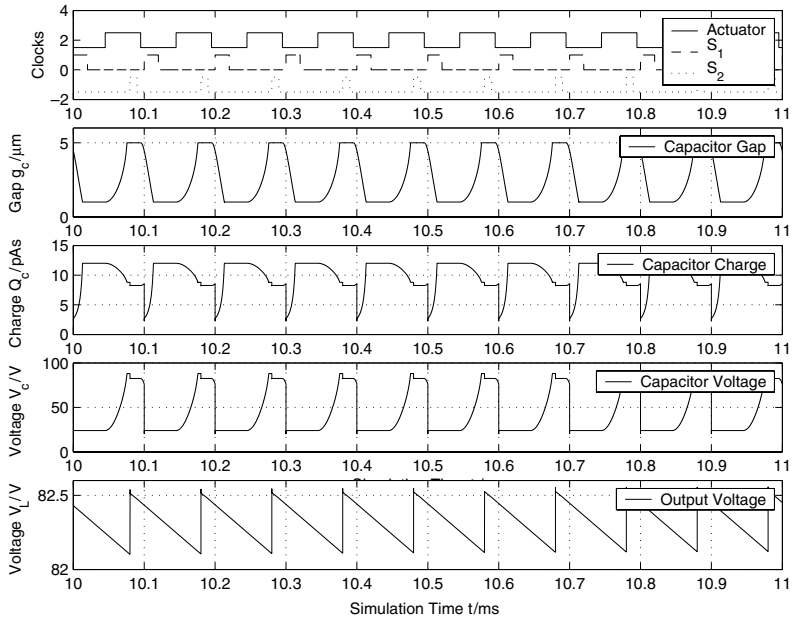

Figure 11. Simulation of the system with transverse capacitor, transverse actuator, active reduction. Stationary output after 10 ms for $M = 5$, $C_{\min} = 0.1$ pF, $f_{\text{clk}} = 10$ kHz, $V_{\text{in}} = 24$ V.

Table 2. Influence of $g_{\min}$ in transverse capacitor systems with transverse actuator and active increase, for $M = 5$ and $C_{\min} = 0.1$ pF.

$g_{\min}$ (μm)	f_{clk} (kHz)	M_e	A_a (mm^2)	C_a (pF)	Surface S (mm)^2	M_e/S (1/mm^2)	P_{out}/S (μW/mm^2)
0.5	50.0	3.6	0.17	3	0.01	509.4	105.63
1.0	20.0	3.3	0.45	4	0.03	124.5	27.34
2.0	10.0	3.3	2.74	12	0.29	11.5	2.34
5.0	1.4	2.4	39.80	70	10.00	0.2	0.04

In figure 11 the system has reached its stationary output and the remaining ripple caused by the resistive load R_L can be clearly seen. The simulation results are in good agreement with equations (2), (3) and (4) from section 3.

6. Prototype design

A suitable fabrication process exists in the clean room at Southampton University and is used as a basis for prototype

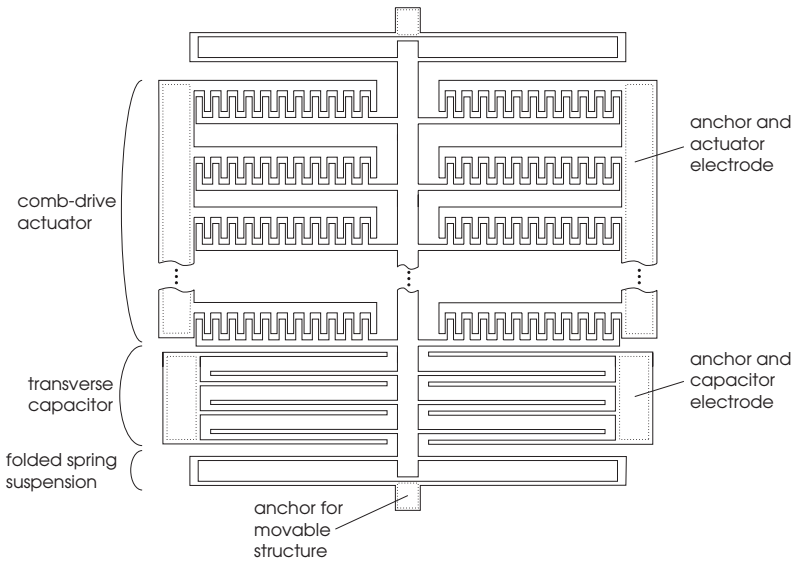

Figure 12. Suggestion for a prototype layout. Dotted lines represent the anchors of full wafer thickness.

design. The process uses DRIE from the back of a 380 μm silicon wafer to define anchor structures and leave a 60 μm thick structural layer. The bottom of the wafer is anodically bonded to a support glass wafer before the MEMS structures are etched in DRIE from the top. This process should allow for low parasitic capacitances since the dielectric path length through the glass wafer will be long.

Since the structures discussed in this paper require quite large electrode areas and finger numbers, the electrodes have to be split up into a number of parallel segments. A layout for the transverse capacitor and comb-drive system with active reduction is shown in figure 12. A central beam is suspended by folded flexure springs and connected to the electrical ground through the anchors of the springs. In the lower section it carries eight capacitor electrode segments. The upper section is the comb-drive actuator, which is only partially shown for clarity. The dotted areas represent the anchors underneath the top layer. This layout can be reused for all the system topologies discussed in this paper.

It should be noted that the cascaded arrangement of electrodes introduces unwanted electrostatic fields on the backsides of the electrodes, which leads to a reduction in effective multiplication factor. Larger spacing between the segments reduces this influence at the expense of greater system size. Also, the transverse electrodes will bend towards each other depending on their beam width. This effect leads to an increase in maximum capacitance and thus conversion factor but it imposes a maximum length for the electrode segments.

7. Conclusion

The principle of a micro-electro-mechanical voltage step-up converter has been introduced in this paper. This type of voltage converter holds potential benefit for applications that hinge on process integration and miniaturization.

The electrical properties of MEMS voltage converters have been analysed in analogy with the classical charge pump and a SIMULINK model library has been implemented. A number of design cases have been studied and their theoretical performance has been verified by system simulations. Prototype layouts have been suggested and further work should mainly concentrate on the fabrication and characterization of actual devices and the development of micromechanical switches to be integrated with the conversion system.

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