A CDMA2000 Zero-IF Receiver With Low-Leakage Integrated Front-End

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***Abstract*—This paper describes a highly integrated CDMA 2000 US-CEL band (880-MHz) receiver. The single-chip zero-IF design incorporates all receiver signal-path functions including the low-noise amplifier (LNA) on a single die. The complete receiver design exceeds the stringent linearity and local oscillator (LO) leakage requirements for this standard arising from the coexistence with narrow-band FM signals. The integrated LNA achieves 1.0-dB noise figure with +9-dBm IIP3 at high gain, and by maintaining LO leakage to the antenna port well below −80 dBm at all gain settings, no external LNA is required. The receiver is fabricated in a 0.25-μm 40-GHz f_t BICMOS technology, and occupies 3 mm^2.**

***Index Terms*—CDMA, *I/Q*, integrated channel filter, RF front-end, receiver, zero IF.**

I. System Requirements

INCREASED levels of radio integration with low external component count are essential for cellular handset manufacturers to achieve low product cost. These demands have led to the popularity of low and zero intermediate frequency (IF) architectures which eliminate IF surface acoustic wave (SAW) filters and their associated terminated interfaces in the radio. While practical implementations have been demonstrated for GSM and UMTS systems [2]–[4], the much more stringent performance requirements of the U.S. CDMA-2000 [1] cellular system have made it more difficult to avoid conventional superhet architectures.

As a full duplex system, one of the key challenges that CDMA2000 presents is dealing with signal leakage from transmit to receive paths; at the present state of the art, separate transmit and receive chips are the rule to avoid substrate- and package-related signal coupling. For the receiver alone, there is also the requirement to tolerate and indeed to work with legacy narrow-band FM analog systems (AMPS) in the same 880-MHz frequency spectrum [1] (Fig. 1), leading to several severe performance restrictions, in terms of input linearity, local oscillator (LO) leakage, and LO phase noise. In this design, we tackle the first two requirements, and meet the limits with a fully integrated signal path. Other designs employing zero IF (ZIF) for U.S. CDMA have opted to use a separate low-noise amplifier (LNA) to achieve this isolation [5].

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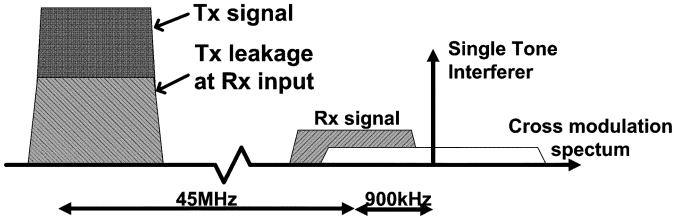

Fig. 1. CDMA input frequency spectrum with FM (AMPS) interferer and cross-modulation spectrum.

A companion transmitter IC [6] also uses a direct conversion scheme to keep total system costs to a minimum.

II. ZIF Receiver Architecture

The overall system architecture is shown in Fig. 2, and the key performance requirements are given in Tables I and II. The worst case interference scenario is presented in Fig. 1, where transmit leakage cross-modulates with a strong adjacent FM carrier. This situation tends to dictate the linearity performance specifications. In practical designs, the attenuation afforded at the input by commercial duplexer blocks is typically around 55 dB, which is insufficient to keep the power in the transmit spectrum present at the receiver input low enough to eliminate this cross-modulation problems associated with FM carriers. To minimize the impact of cross-modulation without employing a sharper, more lossy (and costly) filter at this point, the LNA must have very high linearity (IIP3 of +9 dBm). Note that even with this demanding performance, it is necessary to employ an additional bandpass SAW filter in the receive path between the LNA and the mixer to provide additional attenuation of transmit band leakage (typically 40 dB) and thus ease the mixer linearity requirements.

An external oscillator module running at double the required frequency provides the drive to the LO quadrature generator. The signal path is split into in-phase (I) and quadrature (Q) paths in the mixer switching core and passed to low-pass channel-selection filters.

III. LNA Design

Three gain settings are used to achieve the best overall gain and linearity; only high (+15-dB) and low (−5-dB) gain settings are shown for clarity. The target here is to achieve 20-dB reverse isolation in all gain modes. To meet the overall leakage requirements, the majority of the required −80-dBm isolation is then achieved in the mixer core and its associated interfaces, and maintained with careful layout and pad assignments.

To meet the need for very high reverse isolation a cascode design would normally be used. However, the requirement in high gain mode to combine extremely low noise figure with

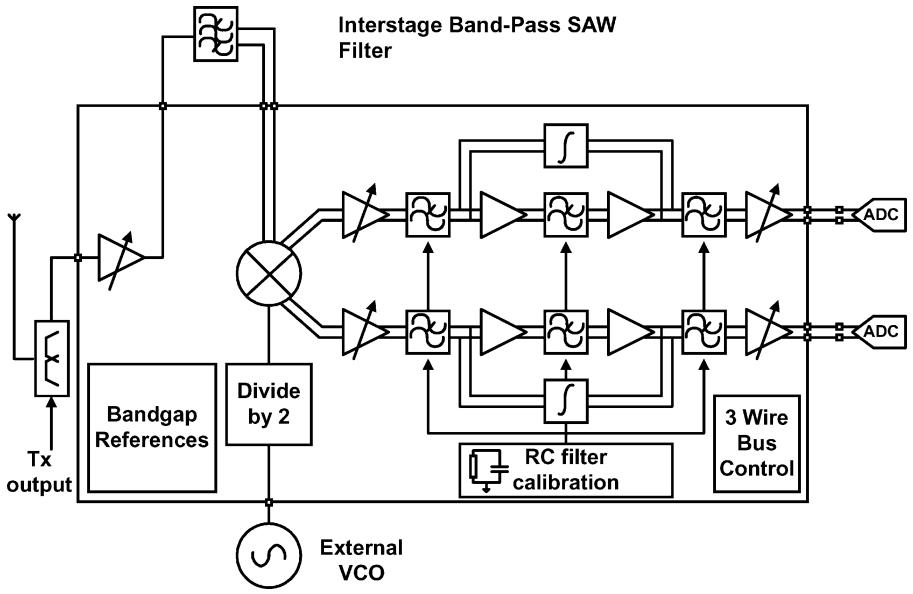

Fig. 2. Zero-IF receiver architecture.

TABLE I
LNA TYPICAL MEASUREMENT RESULTS

Performance Parameter	High Gain Specification	High Gain Meas.	Mid Gain Meas.	Low Gain Meas.
Gain (dB)	16	15.5	4.8	-7
Noise Figure (dB)	1.2	1.0	3.8	9
IIP3 (dBm)	9	9	8	20
Reverse Isolation (dB)	20	20	20	20
LO level at LNA input (dBm)	-82	<-100	<-100	<-100
Icc (mA)	7.5	7.7	3.5	3.2

TABLE II
MIXER AND BASEBAND TYPICAL MEASUREMENT RESULTS

Performance Parameter	Specification	Measured
Gain, high gain mode (dB)	55	55
Gain, mid-gain1 mode (dB)	39	39
Gain, mid-gain2 mode (dB)	23	23
Gain, low gain mode (dB)	7	8.8
DSB Noise Figure (dB)	10	9
IIP2 (dBm)	58	65
IIP3 (dBm)	3	3
Sideband Suppression (dB)	20	40
LO Phase noise at mx input (dBc/Hz)	-148 @ 900kHz	-148 @ 900kHz
LO level at mixer input (dBm)	-60	<-95
Icc (mA)	40	40

high IIP3 figures tends to rule out this configuration, and the design is based around a single transistor common emitter (CE) amplifier [Fig. 3(a)]. To achieve the best compromise between gain, linearity, and input matching, emitter degeneration is provided by means of a bondwire inductance, saving some area at the expense of requiring very thorough package modeling. An external *LC* trap circuit is also used at the input for further linearity improvement [7] (simulations typically indicate around 3-dB benefit with $C = 100$ nF, and $L = 9.5$ nH). The LNA is current biased from a mirror structure supplied from a bandgap reference. An external load is used with a simple matching network to allow reasonable power gain while providing a good match to the interstage SAW filter's 50-Ω input.

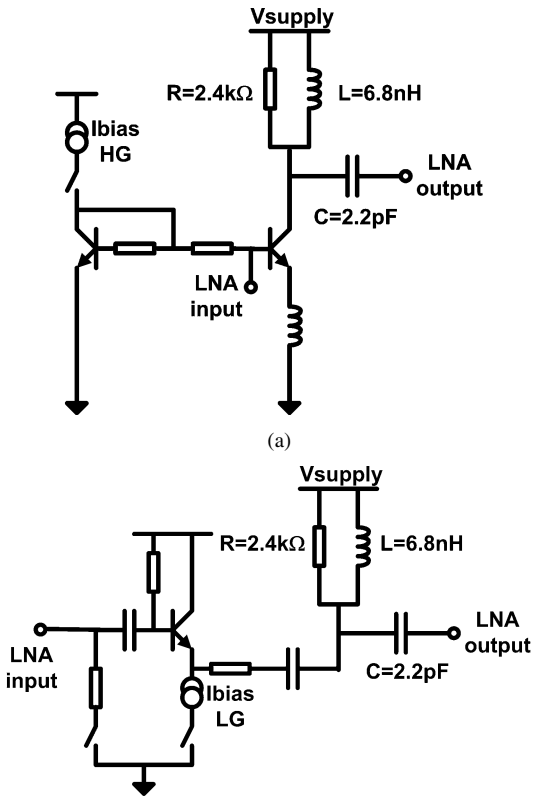

Fig. 3. (a) LNA showing high gain mode. (b) LNA showing low gain mode.

In the low gain mode, the LNA CE stage would typically be replaced with a passive attenuator configuration to save power, but this type of circuit offers very poor reverse isolation. To be consistent with the zero-IF architecture's requirements, an emitter follower is used, keeping the reverse isolation at around 20 dB while maintaining excellent linearity [Fig. 3(b)].

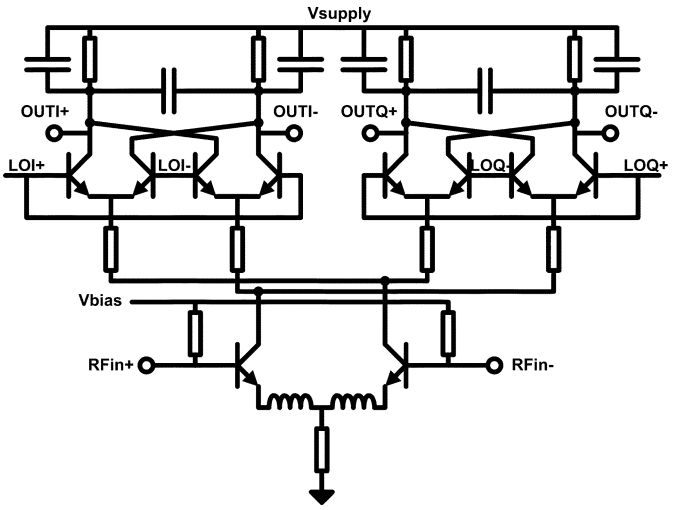

Fig. 4. Downconversion mixer.

In the mid gain setting, the LNA is again set in CE configuration to maintain isolation, this time with an internal degeneration inductance.

IV. Mixer

The linearity, noise figure, matching, and LO leakage requirements are also quite severe for the mixer. The input port now presents a 200-Ω differential impedance to match the SAW filter (the latter performs the impedance and differential-to-single-ended transformations). Fig. 4 shows the basic scheme.

The design is based on a complex version of the ubiquitous current-steering bipolar form. Inductive degeneration is used in the transconductor to achieve the linearity (IIP3 $= +5$ dBm), noise (DSB NF $= 7$ dB) and impedance matching specifications with a current of approximately 10 mA. In this case, an on-chip differential inductor is laid out in the thick top metal layer provided by the technology.

Splitting the signal into the *I* and *Q* paths occurs inside the mixer at the transconductor output, and separate *I* and *Q* LO signals are applied to create quadrature baseband paths. The switching mixer is actually implemented as the "Bixer" variant [4]. The resistors performing the current splitting between *I* and *Q* paths serve the added purpose of steering almost all of the transconductor current to the *Q* branch at the instant that the *I* branch core is in its transitional state, and *vice versa*. Hence, since each switching pair has almost no current during the time it is approximately balanced, the noise generated in the switching core transitions is periodically reduced, giving a small improvement in conversion gain and noise figure without any current penalty. With resistive loads of around 200 Ω, a voltage gain of $+7$ dB is achieved. Note the use of capacitors in the collector loads, setting a pole at approximately 15 MHz to remove part of the strong out-of-band energy from the input to the baseband filters.

To achieve the overall leakage and IIP2 requirements of the receiver, the sources of various imperfections were analyzed in some detail. As would be expected, many matching issues were highlighted in this study (load resistors, switching core, etc.) as giving rise to unbalanced terms, and hence, permitting second-order terms to propagate; these issues were addressed by optimizing both the design and layout. The requirement for having resistive loads while maintaining internal linearity without compression (i.e., clipping) inside the mixer posed some challenge to get the best compromise.

V. First IF Amplifier

The noise level at the output of the mixer imposes a restriction on the impedance level at this point, and consequently on the size of the capacitors in the channel selection filter. Hence, an amplifier with 0/+16-dB gain is used at the input of the filter, allowing the impedance of the filter to be raised with some area saving. Clearly, care is taken with the linearity behavior of this amplifier. A bipolar input operational amplifier (op-amp) with a high gain bandwidth is used to provide sufficient linearity for high-level interferer signals and to keep the $1/f$ noise low, but this means that the input common-mode range must fall within a certain window. DC coupling is used between the mixer and the amplifier, since the inclusion of any ac coupling would clearly be impractical due to the impedance level necessary. The common-mode input level of the first IF amplifier affects the dc flowing through the mixer loads as well as the bias thought the mixer transconductor. The output common-mode level as used by the channel filter is approximately mid-supply to maximize the dynamic range in the IF path. The input resistors to the amplifier cannot be made large because of the noise figure implications, and hence, the current flow is not negligible. No feedback capacitance is used in this version, as the initial filtering of out-of-band products is performed in the mixer load circuit.

VI. Local Oscillator Path

Meeting the very stringent phase noise requirements imposed by the AMPS system with an integrated oscillator is very difficult, and in this design an external oscillator is used. To minimize the LO leakage at the PCB level, the oscillator is run at twice the signal frequency followed by a conventional emitter-coupled logic (ECL) digital divide-by-two quadrature circuit. Only a single pin is available for the LO input signal, whereas a high-quality differential LO signal is needed on chip to ensure that the digital quadrature generator is accurate, and that mixer IIP2 performance is not compromised. The input buffer is a differential pair with an internally grounded port on one side, laid out with great care to equalise parasitics. The supply current is approximately 7 mA.

VII. Channel Selectivity Filters

The specifications of the channel filters are set to complement the performance of the ADC (and subsequent digital signal processing in the baseband IC); clearly, with higher resolution and faster sample rate the filter requirements could be relaxed further. In this design, the selectivity needed is achieved with a fifth-order elliptic type response; the response is optimized to this application by placing the imaginary axis zeros carefully so as to minimize the impact of the adjacent channel blocking signals at 900 and 1250 kHz, respectively [1]. The overall response

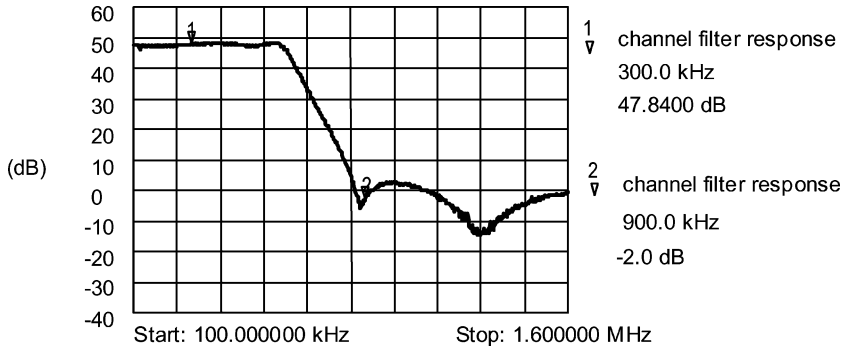

Fig. 5. Measured channel filter response.

is shown in Fig. 5. The selectivity and gain are distributed between three sections, with two biquadratic blocks and a single real pole; the overall gain can be varied from 0 to 48 dB, and the attenuation achieved at 900 kHz is greater than 45 dB.

As with any modern receiver with complex outputs, the matching of the gain and phase through the filters is critical to the overall performance. A minimum sideband suppression of 20 dB is required due to all causes, and so the filter alone must achieve significantly better than this. Together with the strict linearity requirements, this leads one to an op-amp-*RC* architecture, with the cutoff frequency and positioning of the zeros tuned by means of switchable capacitor arrays [8]. A digital calibration circuit is used to set the tuning to 5-bit accuracy with respect to the fabricated *RC* time constant and a reference oscillator, leading to maximum error in the cutoff frequency of approximately 3%.

Op-amp specifications have to be set such that there is still enough gain to handle out-of-band signals without incurring linearity problems. Fully differential amplifiers with bipolar input stages are used to achieve the unity gain bandwidth while keeping $1/f$ noise low. Signal path gain is set using switchable resistors in the gain blocks distributed through the filter chain. The impedance levels in the three filter stages are progressively scaled to optimize for noise and die size; at the input from the mixer, the noise budget must be carefully balanced and so low resistance values must be used at the cost of capacitor area. In the succeeding stages, there is some further gain available to reduce the impact of noise and so higher impedance levels can be used.

DC offset cancellation is essential in a ZIF receiver, and this must be able to handle gain-dependent errors as well as static components. A feedback integrator scheme is used with its on-chip time constant optimized at around 1 kHz against the constraints of settling time and the impact on overall error rate. The positions of the sense and feedback of the dc loop are carefully selected to optimize the management of dc offsets within the IF path.

VIII. Silicon Implementation

The circuit is implemented in a 40-GHz f_t 0.25-μm BICMOS process [9]. In addition to the high-frequency and low-noise performance of the bipolar transistors, this technology has excellent passive components available; the high-density high-linearity MIM capacitors (5 fF/μm^2) make the layout of the dual channel-selection filter banks particularly efficient. Deep trench isolation is used extensively in the layout to achieve maximum signal isolation within the die, so as to minimize the risk of unforeseen LO leakage paths arising. The die photograph is shown in Fig. 6.

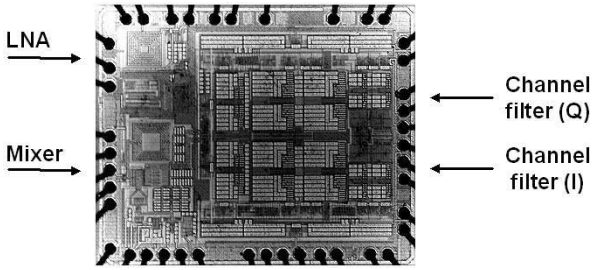

Fig. 6. Die microphotograph.

IX. Measurements and Results

The front-end performance of this design was clearly critical to the success of the receiver. Because of the requirements for external filters at the RF ports, the LNA is easily available for measurement as a separate block. The key performance results are given in Tables I and II. Performance values given are typical from the initial characterization of 20 packaged devices. The LNA noise figure of 1.0 dB is excellent for a design in a silicon (i.e., not SiGe) process. IIP3 is also excellent for the LNA. The mixer and IF path typically achieve an IIP2 of +65 dBm without calibration, IIP3 of greater than +3 dBm, and sideband suppression of −40 dB. Very low levels of LO leakage (i.e., less than −95 dBm) were measured at both the mixer and the LNA inputs. The overall figures show that the complete receiver can be made with the LNA on the same die, saving the expense of a separate SiGe or GaAs IC.

X. Conclusion

A complete CDMA2000 receiver using a zero-IF architecture has been implemented in a silicon BiCMOS technology. Measurements confirm that the receiver can meet all requirements of noise, linearity, and LO leakage with an integrated LNA on the same die. Excellent front-end RF performance has been demonstrated in a pure silicon technology.

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