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Recent developments in deca-nanometer vertical MOSFETs

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Abstract

We report simulations and experimental work relating to innovations in the area of ultra short channel vertical transistors. The use of dielectric pockets can mitigate short channel effects of charge sharing and bulk punch-through; thickened oxide regions can minimize parasitic overlap capacitance in source and drain; a narrow band gap, SiGe source can reduce considerably the gain of the parasitic bipolar transistor which is particularly severe in vertical MOSFETs. The work is put into the context of the ITRS roadmap and it is demonstrated that vertical transistors can provide high performance at relaxed lithographic constraints.
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1. Introduction

The continued scaling of MOSFETs to the deca-nanometre regime presents very major technological challenges to the industry and will require enormous investment in plant and equipment. Vertical transistors are currently of interest because they offer a route to ultra-short channel MOSFETs with relaxed (that is cheap) lithography rules. In addition, such transistors have much reduced footprint: up to a factor of 2.4 has been described [1]. Particular issues for vertical MOSFETs compared to their conventional lateral counterparts, are the higher overlap capacitance, high current drive and high gain parasitic bipolar transistor (PBT) and problems with channel engineering to control short channel effects (SCE). We describe in this paper, our recent work which addresses these short-comings of vertical transistors. Fig. 1 shows a schematic diagram that serves to summarise some of the architectural features that we propose. Notice that the transistor can be considered to operate in either source up, or down modes although not all architectural features are appropriate for bi-directional operation. Specifically we identify the use of a so-called dielectric pocket (DP) to control SCE (source down mode) [2,3], thickened oxide regions, including a novel fillet oxidation (FILOX) overlap process to minimize overlap capacitance [2,4] and the use of poly-SiGe regions to reduce the emitter efficiency of the PBT (source up mode) [5]. We now consider these concepts, and indicate the expected performance advantage in the ITRS context. Furthermore, experimental results are presented on single- and

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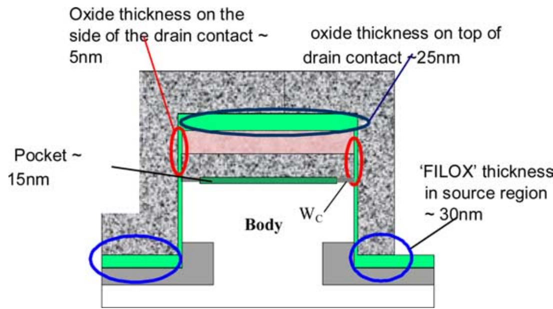


Fig. 1. Vertical MOSFET schematic.

surround-gate vertical MOSFETs [6]. Reduced overlap capacitance is demonstrated due to bird's beak formation in the FILOX process. It should be noted that our approach is to realize transistors that can be integrated into a CMOS process.

2. Short channel effects

Fig. 1 shows the incorporation of a thin oxide region (DP) on top of a pillar which defines the vertical transistor. The channel is formed by growth of a thin epitaxial layer after etching the pillar using a scheme similar to that of a graft base in heterojunction bipolar processing. We show in Fig. 2 SEM cross sections illustrating the recessed DP. This strategy permits adequate seeding of the epitaxial layer and so overgrowth to ensure connectivity over the edge of the DP region. The DP serves a number of roles: it prevents dopant out-diffusion and so mitigates bulk punch-through effects, it influences the electrostatics of the drain region so reducing charge sharing and finally, effectively suppresses the PBT associated with source/body/drain regions. Fig. 3 shows ISE simulation results which summarise the on- and off-current for different body doping and contact width for a vertical *p*-MOSFET. The influence of the DP is such that I_{OFF} can be reduced with little reduction in I_{ON}. The reduction in I_{ON} is a result of the reduced charge sharing and hence increased V_T whereas the I_{OFF} reduces due to suppressed DIBL and punch-through. For $W_C = 50$ nm, the DP no longer influences the electrostatics at the drain. A body doping of 2×10^{18} cm^{-3}, $W_C = 25$ nm, $t_{OX} = 2$ nm, gives $V_T = -0.28$ V and $I_{OFF} = 1.5$ nA/μm at $V_{DD} = 1$ V.

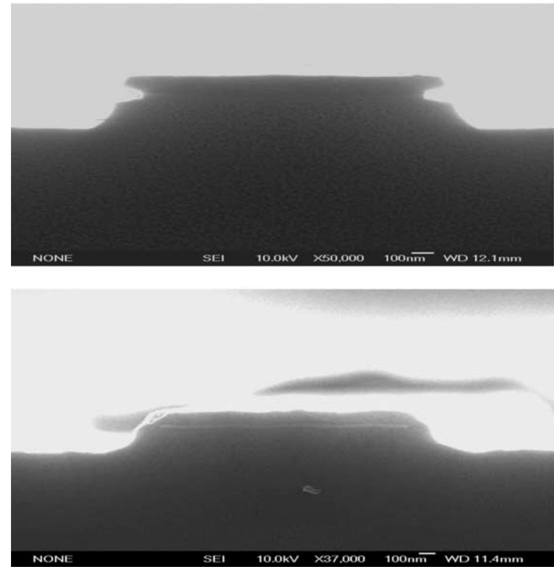


Fig. 2. SEM before and after epi-channel growth.

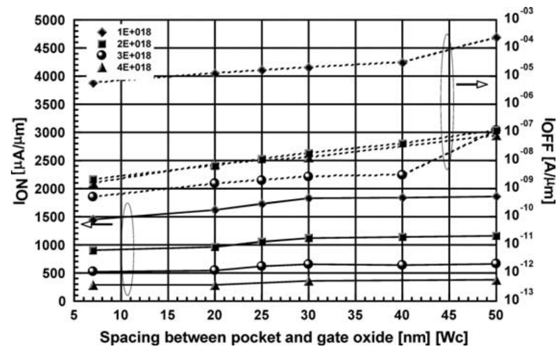


Fig. 3. I_{ON} and I_{OFF} for different contact widths, W_C.

3. Reduction of parasitic overlap capacitance

Parasitic capacitance represents probably the biggest challenge for vertical MOSFETs. The strategy here is to look for ways of thickening oxide regions, as depicted in Fig. 1. Reduction of gate-source overlap capacitance (bottom of pillar) is achieved by a LOCOS type process 'FILOX' [3]. Fig. 4 shows a field emission SEM cross-section of

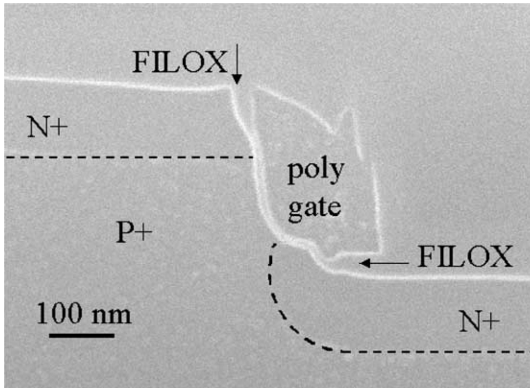


Fig. 4. FESEM of a vertical MOSFET.

a vertical *n*-MOSFET featuring this approach. Incorporation of a deposited oxide region on top of the pillar and the thicker oxide grown on the highly doped poly-Si extrinsic drain contact can reduce significantly the gate-drain capacitance. A study using MOS-capacitors has demonstrated a 5-fold reduction in parasitic overlap capacitance using FILOX and a thick top oxide [3]. To summarise the study, we show in Fig. 5, *C–V* plots for pillars with gate oxide only, with a 20 nm thermal oxide–130 nm CVD nitride and 50 nm LTO stack (ONO) and finally the ONO stack plus the FILOX process. The ONO stack reduces the capacitance by 30% and the introduction of the FILOX gives the reduction overall of a factor 5. A semi-analytical transient model has been developed to assist in the optimization of the device with regard to parasitic capacitances [2]. Essentially, we consider an inverter loaded by n other inverters. Analytical expressions can be written down for each parasitic capacitance component in terms of the device physical dimensions and parameters. These components can then be combined to form a single load capacitance C_L. The metric of output voltage fall time is used to quantify the delay of the inverter and the influence of each parasitic component can be considered in turn. Fig. 1 includes the results of such a study whereby the required relative thicknesses of the thickened oxide regions are noted. Fig. 6 shows the performance of the optimised device in the context of the ITRS roadmap. Note that the channel length of the vertical MOSFET remains fixed at 50 nm. The device shows considerably advantage over its lateral counterpart for technology nodes down to 90 nm. The degradation of performance thereafter arises because of the scaling of the supply voltage. The effect of maintaining a V_{DD} of 1 V is shown also. It should be noted that interconnect capacitance will become dominant at lower technology nodes where the additional drive offered by the vertical MOSFET dual channels will offer further advantage. This is demonstrated in the figure by the inclusion of a fixed load of 5fF and the vertical MOSFET is seen to competitive down to 50 nm. The source and drain resistances of the vertical MOSFET (extracted from ISE simulation) are 3–4

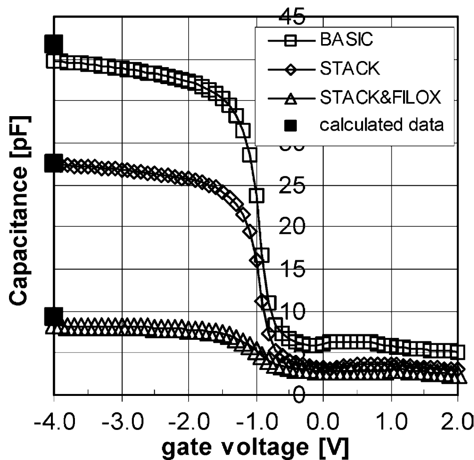


Fig. 5. *C–V* plots showing reduction of parasitics.

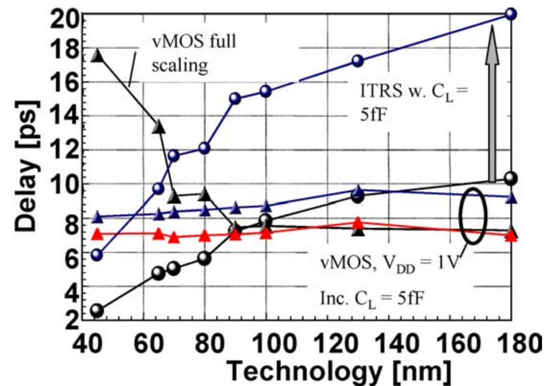


Fig. 6. Projected performance of vertical MOSFET.

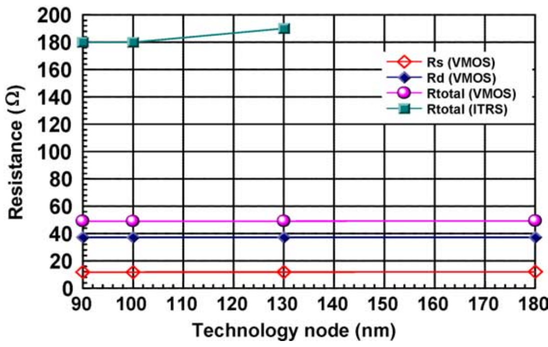


Fig. 7. Scaling of series resistance.

times smaller than the ITRS values and these resistances do not significantly increase when the device is scaled as shown in Fig. 7. This arises essentially because the dielectric pocket precludes the need for pockets or extensions.

4. Experimental transistor characteristics

Both p-channel and n-channel test transistors have been successfully fabricated to demonstrate some of the concepts outlined above. Gate oxide thickness was 3 nm. Single, double and surround gate types have been realised and Fig. 8 shows the gate over-drive I_{ON} versus drawn width W, for each type. The expected linear relationship is seen for each type confirming full control of the channel. Process differences account for the non-

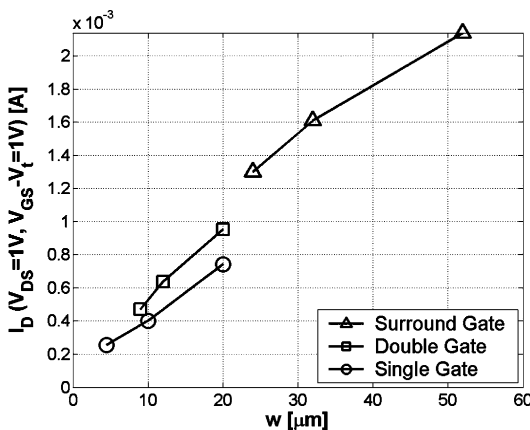


Fig. 8. I_{ON} versus W for each vertical MOSFET type.

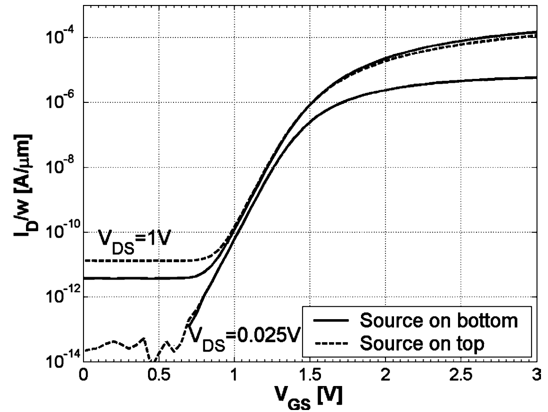
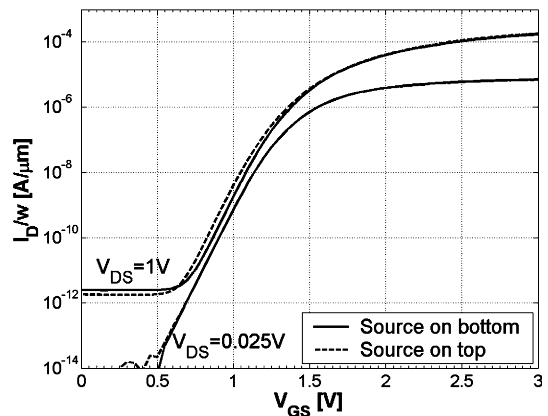


Fig. 9. I–V plots for double gate n-MOSFETs.

convergence of the data of each type. Fig. 9 shows transfer characteristics of a double gate n-MOSFET with $W = 9$ μm and $L = 125$ nm for both



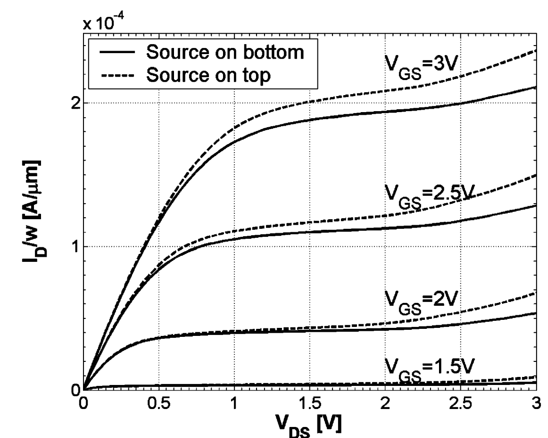


Fig. 10. I–V plots for surround gate n-MOSFETs.

modes of operation (source up and down) and $V_{DS} = 25$ mV and 1 V. The lowest sub-threshold slope and leakage current are obtained for surround gate transistors because the entire pillar is under gate control so mitigating parasitic leakage paths. Results are shown in Fig. 10 which shows transfer and output characteristics for devices with $W = 24$ μm and $L = 125$ nm. The good symmetry of operation attests to the low series resistance for both source and drain contacts. Sheet resistance of 49 Ω/□ has been extracted from experimental devices.

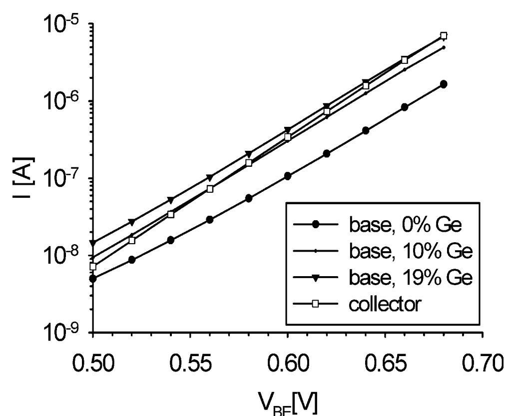


Fig. 11. Gummel plots for test bipolar transistors.

5. Suppression of parasitic bipolar transistor

The dielectric pocket concept brings the added benefit of reducing considerably the area of the effective emitter and collector formed by the source and drain of the vertical MOSFET and so reduced the magnitude of base and collector currents of the PBT. The DP device is however inherently 'drain up'. An alternative approach to minimise parasitic bipolar transistor gain for drain-down configurations (source at the top), is to include a poly-SiGe extrinsic source contact [5]. This serves to steepen the profile of minority carriers injected into the parasitic emitter so increasing the base current and reducing the gain. A theoretical model for the base current of such a polySiGe emitter has been developed, which combines the effects of the poly-SiGe grains, the grain boundaries and the interfacial layer at the polySiGe/Si interface into an expression for the effective surface recombination velocity of a polySiGe emitter [5]. The model is equally valid for the parasitic BJT in vertical MOSFETs. Silicon bipolar transistors were fabricated with 0, 10% and 19% Ge in the polySiGe emitter and the variation of base current with Ge content characterised. Fig. 11 shows Gummel plots from bipolar test transistors where a considerable reduction in BJT gain is evident. The measured base current for a polySiGe emitter is seen to increase by a factor of 3.2 for 10% Ge and 4.0 for 19% Ge compared with a control transistor containing no germanium, in good agreement with the theoretical predictions. The competing mechanisms of base current increase by Ge incorporation into the polysilicon and base current decrease due to an interfacial oxide layer were investigated. The size of the base current increase with Ge content depends on the thickness of the interfacial layer, with larger increases being obtained for thinner interfacial layers. The introduction of germanium into a polysilicon emitter therefore allows the base current, and hence the gain, to be controlled by means of the Ge content in the polySiGe parasitic emitter of a vertical MOSFET.

6. Discussion and conclusions

We have reviewed in this paper, a number of strategies to address problems with realising high performance vertical MOSFETs. Our transistor architectures and processes are all compatible with full CMOS realisation. We have demonstrated by simulation that a dielectric pocket can reduce charge sharing and other short channel effects to produce a transistor with good I_{ON} to I_{OFF} ratio. It is worth noting that the approach has a particular benefit for the *p*-MOSFET in that excessive boron penetration in the bulk of the transistor is prevented. A process to realise the DP has been developed based on that of a HBT graft base. Continuity of the epitaxial channel layer over the DP edge has been achieved. Strategies to reduce parasitic capacitances have been proven and shown to produce a factor of five improvement from capacitors. A LOCOS type, FILOX process

has been developed to place a thick oxide in the bottom contact region of the device to reduce greatly the overlap capacitance. A semi-analytical circuit based model has been developed to identify the important parasitic overlap capacitance components and to assist in the optimisation of the device. The semi-optimised device performance has been assessed in the context of the ITRS roadmap. The reduced scaling constraints for channel length and series resistance suggest great potential for these transistors. Experimental test transistors have been successfully realised. A narrow band gap concept to suppress parasitic transistor action in the vertical MOSFETs has been shown to reduce the gain by a factor of three.

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