REALIZATION AND CHARACTERIZATION OF VERTICAL MOSFETs WITH REDUCED PARASITIC CAPACITANCE

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Key words to describe this work: Vertical MOSFET, parasitic capacitance

Key Results: Vertical MOS transistors composed by an etched pillar structure with self-aligned Source and Drain and reduced parasitic capacitance have been realized and characterized.

How does the work advance the state-of-the-art?: Comparison between Surround Gate and Single/Double Gate devices will improve understanding of physical behavior and process variables.

Motivation (Problems addressed): Realization of Vertical MOSFETs with reduced parasitic capacitance and easy to integrate in standard CMOS processing.

Introduction

Vertical MOS transistors built on the sidewalls of pillars have been developed for three main reasons:

- Surround Gate or Double Gate structures allow more device width per unit of silicon area; this leads to an increase of the drive current per unit area too;
- the Gate length is controlled by non-lithographic methods; this allows a smaller channel length to be realized than with photolithography;
- the Gate length is decoupled from the packing density; as a result, long channel transistors (with lower off currents) can be produced without decreasing the number of devices per unit area.

The main disadvantage or the Vertical structure is related to the significant processing challenges involved; these are difficult to integrate in traditional CMOS production processes.

Device characteristics

One of the main challenges with a vertical geometry is the integration of both pMOS and nMOS devices in a simple process flow, in order to be able to obtain CMOS circuits. In particular, the definition of the channel length by deposition of doped silicon films (epitaxy) gives raise to a lot of complications compared to the standard CMOS process.

The device analyzed here comprises an etched pillar structure with self-aligned Source and Drain. The electrodes are obtained through ion implantation followed by anneal, without any selective epitaxy step. Thus this process is easily merged in the traditional CMOS process flow.

Fabrication and layout

The most important process steps are summarized in Fig. 1.

First, the Drain (on the top of the pillar; see Fig. 1a) is obtained by ion implantation, together with the Source (at the bottom of the pillar). The Source is self-aligned to the nitride spacers on the sides of the pillars. Their width is crucial because it defines the distance between the Source border and the side of the pillar, thus determining the channel length. The pillars are separated from the silicon pillar by a 20 nm stress relief oxide.

The second important feature underlined in Fig. 1a is a thick (40 nm) oxide layer grown on top of the Source. This layer decreases the overlay between Gate and Source (see Fig. 1c), thus reducing the parasitic capacitance of the device.

Fig. 1b shows the removal of the nitride spacers and of the stress relief oxide, followed by dry oxidation to grow the Gate oxide (3 nm).

Finally (Fig. 1c) the Gate is deposited and patterned, an anneal is performed for

implant activation and the metal contacts are defined.

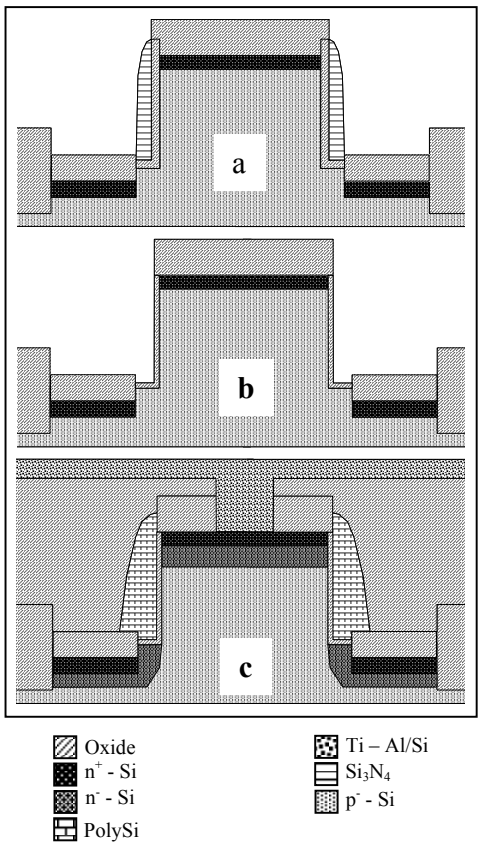

Fig. 1. Principal process steps for the production of the Vertical MOSFETs.

Results and Discussion

In Fig. 2 the layout of the devices realized is shown. Three different geometries are shown: Single Gate (Fig. 2a), Surround Gate (Fig. 2b) and Double Gate (Fig. 2c).

The devices have a channel length of about 100 nm and a Gate oxide thickness of 3 nm. In Fig. 3 is shown the measured $I_D(V_{GS})$ characteristic of the Surround Gate Transistor for various Drain voltages; in Fig. 4 the output characteristic $I_D(V_{DS})$ of the same device is presented.

The devices have a linear extrapolated threshold voltage (measured at V_{DS} = 0.025V) of 1.17/1.27V, (the range is due to the geometry and the channel width). The subthreshold swing (measured at V_{DS} = 0.025V) lies between 115 and 135mV.

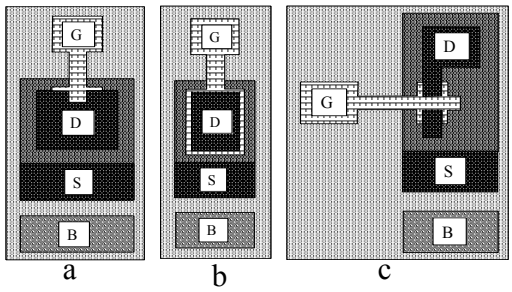

Fig. 2. Layout of realized devices.

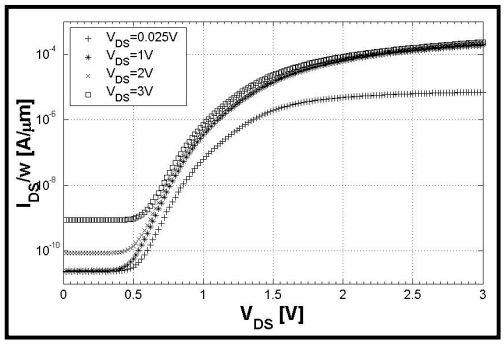

Fig. 3. Measured input characteristic of Surround Gate Transistor, channel width 24 μm.

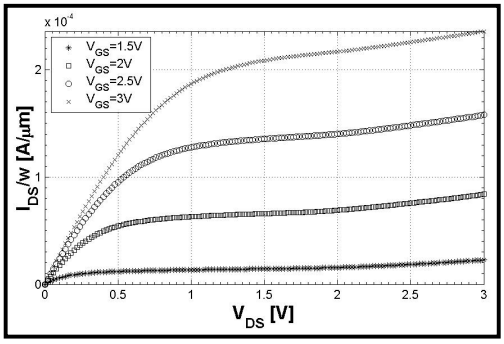

Fig. 4. Measured output characteristic of Surround Gate Transistor, channel width 24 μm.

Conclusion

Vertical MOSFET transistors with Surround Gate, Simple Gate and Double Gate geometries have been successfully realized. The production process (etched pillar structure with self-aligned Source and Drain) allows an easy integration of the devices in a standard CMOS circuit. A thick oxide layer between the bottom electrode and the Gate reduces the Gate/Source overlap and the parasitic capacitances.