Acquisition of m-Sequences Using Recursive Soft Sequential Estimation

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***Abstract*—A novel sequential estimation method is proposed for the initial synchronization of pseudonoise (PN) signals derived from m-sequences. This sequential estimation method is designed based on the principle of recursive soft-in/soft-out (SISO) decoding, and we refer to it as the recursive soft sequential estimation (RSSE) acquisition scheme. The RSSE acquisition scheme exhibits a complexity similar to that of a conventional m-sequence generator, which increases only linearly with the number of stages in the m-sequence generator. Our simulation results also show that the acquisition time of the proposed RSSE acquisition scheme is also linearly dependent on the number of stages in the m-sequence generator. Owing to the above properties, the employment of the proposed RSSE acquisition scheme is beneficial for the acquisition of long m-sequences.**

***Index Terms*—Acquisition, initial synchronization, maximum-likelihood (ML) estimation, m-sequence, pseudonoise (PN) signals, recursive decoding, sequential estimation, soft-in/soft-out (SISO) decoding, spread-spectrum signals.**

I. Introduction

PSEUDONOISE (PN) code acquisition, which is also often referred to as initial synchronization, is the necessary first step in the receiver of spread-spectrum communications schemes, since data demodulation becomes possible only after code acquisition has been obtained [1], [2]. The sequential estimation assisted PN code acquisition proposed by Ward [3] constitutes one of the simplest acquisition schemes. The principle of the sequential estimation acquisition scheme is as follows. The acquisition of an m-sequence of length $(2^S - 1)$, which is also referred to as the *maximum-length feedback shift register sequence*, is deemed successful, provided that S consecutive chips are correctly received by the acquisition device and are loaded into the local m-sequence generator, where successive shifts of the chips in the generator will generate chips that exactly match the further received chips of the transmitted m-sequence. However, in the presence of noise, one or more of the S consecutive chips might be in error, potentially resulting in erroneous loading. In this case, a new set of S chips can be processed similarly.

Clearly, the most critical requirement for attaining the successful acquisition of PN sequences based on sequential estimation [3] is that S consecutive chips of the received noise-contaminated PN sequence have to be correctly estimated. In this contribution, we invoke the iterative soft-in/soft-out (SISO) decoding principle, originally developed for turbo channel decoding [4]–[7], for improving the reliabilities associated with deciding upon the S consecutive chips. Upon exploiting the inherent properties of m-sequences, a recursive soft sequential estimation (RSSE) acquisition scheme is proposed, which estimates S consecutive chips using a recursive SISO decoder. The recursive SISO decoder receives soft information from the channel's output, and soft extrinsic information [4]–[7] from the soft channel outputs associated with the previous chips. The soft output of the recursive SISO decoder is then shifted into a so-called soft-chip register, which provides extrinsic information for the following decoding steps. An important feature of the proposed RSSE acquisition scheme is that it exploits the real-time knowledge of the reliabilities associated with the S consecutive chips. This real-time knowledge of the chip reliabilities can be exploited for determining the probability of successful acquisition of an m-sequence of length $(2^S - 1)$, once S consecutive chips have been loaded into the local m-sequence generator. The proposed RSSE acquisition scheme has an algorithmic complexity similar to that of an m-sequence generator. Our simulation results will show that the acquisition time of the RSSE acquisition scheme is a linear function of the number of stages in the m-sequence generator. Therefore, the proposed RSSE acquisition scheme constitutes a promising technique, especially for the acquisition of long m-sequences.

The remainder of this letter is organized as follows. Section II describes the principle of the sequential estimation acquisition scheme. In Section III, the proposed RSSE acquisition scheme is described and investigated. In Section IV, we provide simulation results, and finally, in Section V, we present our conclusions.

II. Principle of Sequential Estimation Acquisition

The well-established maximum-length sequences, which are also known as m-sequences, are generated using feedback shift registers, as that shown in Fig. 1. In the m-sequence generator, D represents a unity time-delay operation, while each of the coefficients, $g_1, g_2, \ldots, g_S$, represents the presence of a connection if it is a one, or the absence of a connection if it is a zero. Since spread-spectrum communication systems usually employ binary spreading sequences having chip values of $\{+1, -1\}$, in this letter, we assume that the m-sequence generator outputs duo-binary $\{+1, -1\}$ symbols, representing a logical zero with $+1$. Consequently, the conventional modulo-2 addition defined over the field of {1,0} is now replaced by the modulo-2 multiplication operation defined in the field of $\{+1, -1\}$, as shown in Fig. 1. More specifically, let the output binary sequence be $\ldots, c_{-2}, c_{-1}, c_0, c_1, c_2, \ldots$, where $c_i \in \{+1, -1\}$. Furthermore, without loss of generality, we assume that $\{s_1, s_2, \ldots, s_M = S\}$, where s_i is an integer in the range [1,S], is an index set corresponding to the set of feedback taps, implying that in Fig. 1, we have $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_M = S} = 1$, while the

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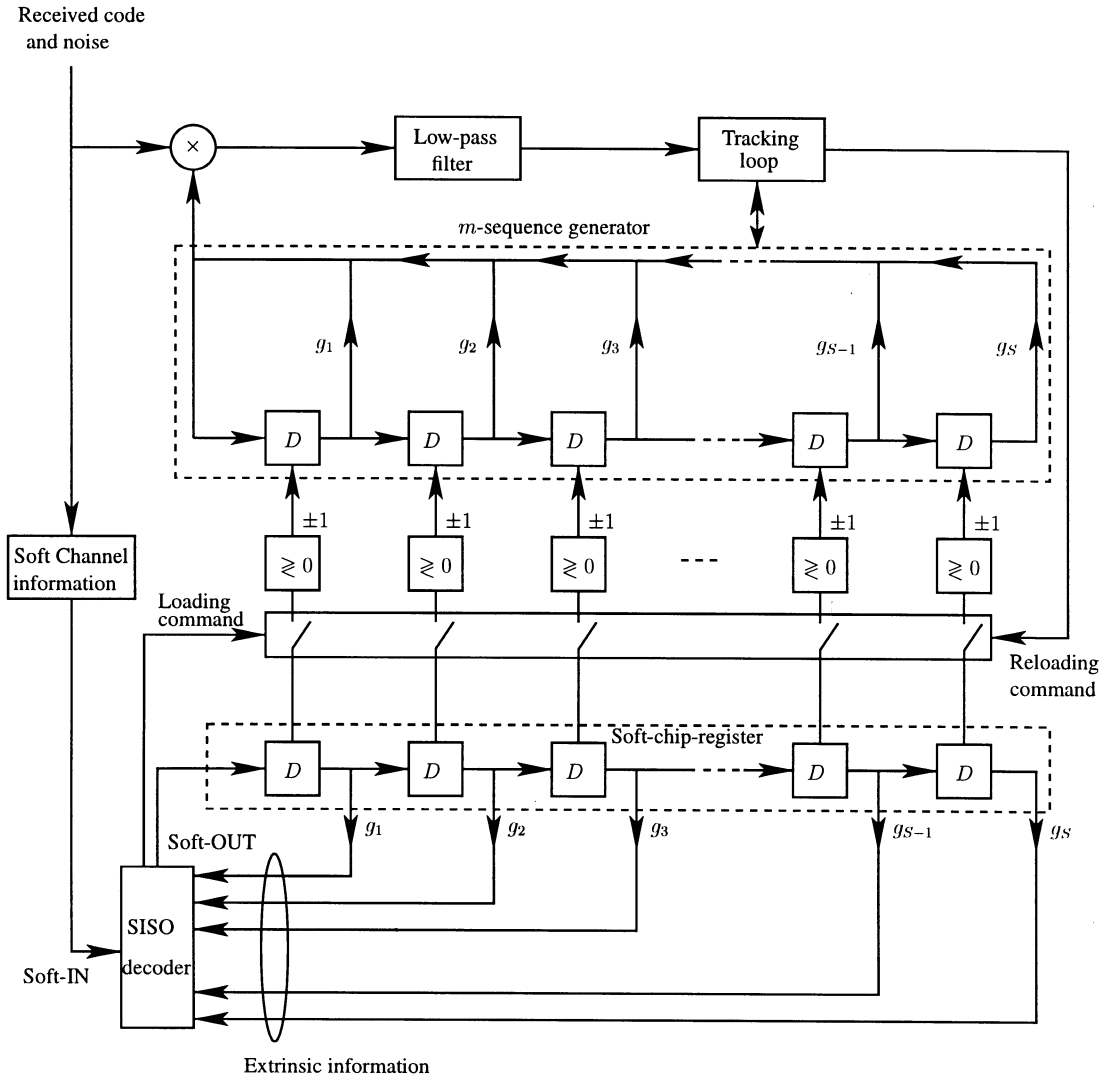

Fig. 1. Schematic diagram of the proposed soft recursive sequential estimator.

remaining coefficients are zero. The above configuration corresponds to the generator polynomial

$$g(D) = 1 + D^{s_1} + D^{s_2} + \ldots + D^{s_l} + \ldots + D^{s_M = S} \quad (1)$$

where $g(D)$ must be a primitive polynomial [8], i.e., a polynomial that cannot be factored, in order to generate an m-sequence. Based on the above assumptions, it can be shown that the output symbols of the m-sequence generator in Fig. 1 obey the recursive equation, expressed as

$$c_i = \prod_{m=1}^{M} c_{i-s_m}, \quad \text{for} \quad i = \ldots, -1, 0, 1, \ldots \quad (2)$$

where $\prod$ represents the product of the coefficients.

In spread-spectrum communications using m-sequences as spreading sequences, (2) implies that if the receiver has the knowledge of the chip values c_{i-1}, c_{i-2}, $\cdots$, c_{i-S} before the transmitter generates the ith chip c_i, and if the receiver uses the same m-sequence generator as the transmitter, then the chip values c_{i-1}, c_{i-2}, $\cdots$, c_{i-S} can be loaded into the corresponding registers of the m-sequence generator at the receiver for generating the forthcoming chips. Consequently, the corresponding replicas of the ith, as well as the following chips, namely $c_i, c_{i+1}, \ldots$, can be obtained at the receiver, which exactly match the received chips as a result of the transmitted m-sequence. Hence, the despreading of the spread transmitted signal can be successfully carried out by correlating it with the m-sequence replica generated at the receiver. What we have described above constitutes the principle behind the sequential estimation acquisition scheme proposed by Ward [3], which have been further investigated in [9] and [10]. However, so far all the known sequential estimation acquisition schemes have been based on the hard chip decisions. Below we propose and investigate a low-complexity acquisition scheme, which is based on the philosophy of the RSSE concept.

III. RSSE Acquisition

Since the invention of turbo codes [4], [5], iterative decoding techniques have attracted wide attention [7]. The employment of iterative decoding is facilitated by using multiple encoders generating either parallel or serial concatenated codes, which are decoded with the aid of SISO decoding algorithms. In iterative decoding, each code is decoded separately, but the soft

output arising from one of the decoding stages is used as the soft input of the next decoding stage. In the context of the sequential estimation-based acquisition used for short m-sequences, the generator's state can be principally estimated using iterative decoding techniques, since each m-sequence produced by an S-stage generator has a period of (2^S-1) chips, and can be considered to be a cyclic Bose–Chaudhuri–Hocquengem (BCH) codeword of length (2^S-1), having minimum distance of 2^{S-1} [9]. Consequently, after the receiver obtained two sets of $2\times(2^S-1)$ number of consecutive samples of the transmitted m-sequence, the m-sequence generator's initial state of S chips can be estimated by iteratively decoding the received m-sequence with the aid of its $2\times(2^S-1)$ number of samples. However, in practical spread-spectrum systems, typically long PN sequences are employed for ensuring secure communications and for the sake of efficiently randomizing and spreading the transmitted signals. Hence, the iterative decoding of $2\times(2^S-1)$ number of chips may be beyond the practical complexity limitations imposed. Therefore, in this section we propose a RSSE, which has a complexity that is only linearly dependent on the number of stages in the m-sequence generator used.

A. Description of the RSSE

We assume that the transmitter aids the acquisition by transmitting the phase-coded carrier signal without data modulation, and consequently, the received data obeys the recursive equation of (2), which allows us to use the proposed RSSE acquisition scheme. The schematic diagram of the proposed RSSE acquisition scheme is shown in Fig. 1, which includes four fundamental building blocks, namely, an m-sequence generator, a soft-chip register, a SISO decoder, and a code phase-tracking loop. The soft-chip register has the same number S of delay units, which we refer to as soft-chip delay units (SCDUs), as the m-sequence generator. The SCDUs store the instantaneous log-likelihood ratio (LLR) values of S consecutive chips. With the aid of these S LLR values, S consecutive chips can be determined and are loaded into the corresponding delay units of the m-sequence generator of Fig. 1. The SISO decoder estimates the corresponding LLR soft output after receiving a soft channel output sample associated with a given chip of the m-sequence. In addition to the so-called intrinsic information of this chip, which was received from the channel, we also exploit the so-called *a priori* (extrinsic) information related to the chip considered, which is provided by the previous decoded LLR values stored in the SCDUs of Fig. 1. The soft output of the SISO decoder is then shifted to the left-most position of the SCDUs in the soft-chip register, while the soft value in the right-most SCDUs is shifted out and discarded. Note that both the m-sequence generator and the soft-chip register use the same feedback branches. However, in the m-sequence generator, the feedback elements are duo-binary values, and the product of these feedback elements is used for generating a binary feedback quantity. By contrast, the feedback elements from the soft-chip register to the SISO decoder consist of the LLR values, and the specific operations must be employed in the soft-value domain to provide extrinsic information for the SISO decoding.

B. RSSE Acquisition Algorithm

As shown in Fig. 1, the SISO decoder requires both soft channel-output information and extrinsic information provided by the previous estimates of the SISO decoder in order to compute the soft output for updating the contents of the soft-chip register. Let $Z_i=\alpha_i c_i+n_i$ represent the received channel output corresponding to chip c_i, where $i=0,1,\ldots$. When communicating over a fading channel, α_i denotes the fading amplitude, whereas for an additive white Gaussian noise (AWGN) channel, we set $\alpha_i=1$. Furthermore, n_i denotes the AWGN having zero mean and a normalized variance of $N_0/2E_c$, where N_0 represents the single-sided power spectral density of the AWGN, E_c represents the transmitted chip energy, and E_c/N_0 represents the signal-to-noise ratio (SNR) per chip. The soft channel-output information, in terms of c_i, is the LLR of c_i conditioned on the channel output Z_i, which is given by [7, Eq. (15)]

$$L(c_i|Z_i)=L_c\cdot Z_i+L(c_i),\quad i=0,1,2,\ldots \tag{3}$$

where $L_c=4\alpha_i\cdot E_c/N_0$, which is referred to as the reliability value of the channel. In (3), $L(c_i)$ is the LLR of a random variable c_i, which is computed as $L(c_i)=\log(P(c_i=+1)/P(c_i=-1))$ [7], where $L(c_i)=0$ if we have no *a priori* information related to c_i, i.e., if we assume that $P(c_i=+1)=P(c_i=-1)=0.5$.

As in Section II, we assume that in Fig. 1, the generator coefficients are given by $g_{s_1}=g_{s_2}=\ldots=g_{s_l}=\ldots=g_{s_M=S}=1$, while the other coefficients are zeros, i.e., the m-sequence generator obeys a recursive equation described by (2). Consequently, the previous soft outputs of the SISO decoder of Fig. 1 obtained at the time indexes of $(i-s_1),(i-s_2),\ldots,(i-(s_M=S))$ are fed back to the SISO decoder, in order to provide extrinsic information for enhancing the correct decoding probability of chip c_i. Let the previous S number of soft outputs of the SISO decoder be $L(y_{i-1}),L(y_{i-2}),\ldots,L(y_{i-S})$. According to (2), the extrinsic information used for enhancing the correct decoding probability of c_i can be approximately expressed as [7, Eq. (12)]

$$\begin{aligned}L_e(c_i)\approx&\left[\prod_{m=1}^{M}\operatorname{sign}\left(L\left(y_{i-s_m}\right)\right)\right]\\&\cdot\min\left\{\left|L\left(y_{i-s_1}\right)\right|,\left|L\left(y_{i-s_2}\right)\right|,\ldots,\right.\\&\left.\left|L\left(y_{i-(s_M=S)}\right)\right|\right\},\quad i=0,1,2,\ldots\end{aligned} \tag{4}$$

where we assume that $L_e(c_{-\infty})=\ldots=L_e(c_{-2})=L_e(c_{-1})=0$.

Finally, with the aid of the channel output information $L_c\cdot Z_i+L(c_i)$ of (3) and the extrinsic information $L_e(c_i)$ of (4), the soft output of the SISO decoder associated with chip c_i can be expressed as

$$\begin{aligned}L(y_i)=&L(c_i|Z_i)+L_e(c_i)\\\approx&L_c\cdot Z_i+L(c_i)+\left[\prod_{m=1}^{M}\operatorname{sign}\left(L(y_{i-s_m}\right)\right]\\&\cdot\min\left\{\left|L\left(y_{i-s_1}\right)\right|,\left|L\left(y_{i-s_2}\right)\right|,\ldots,\right.\\&\left.\left|L\left(y_{i-(s_M=S)}\right)\right|\right\},\quad i=0,1,2,\ldots\end{aligned} \tag{5}$$

where again, $L_e(c_{-\infty}) = \ldots = L_e(c_{-2}) = L_e(c_{-1}) = 0$. Note that (5) represents the recursive equations that can be used for estimating the S consecutive chips required by the receiver's m-sequence generator to produce the full m-sequence. Provided that the channel output SNR per chip value of E_c/N_0 is sufficiently high, the LLR values of the S consecutive chips will increase upon increasing the depth of this recursion. In other words, the reliabilities associated with the S consecutive chips increase, while the erroneous loading probability of the generator, which is defined as the probability of the event that the m-sequence generator is loaded with one or more erroneous chips, decreases upon increasing the number of recursions. Therefore, the acquisition device is capable of observing the reliabilities of the S consecutive chips through observing the amplitudes of the LLR values stored in the SCDUs. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of update operations using (5), and they result in a sufficiently low erroneous loading probability, then, as shown in Fig. 1, a "loading command" can be activated by the SISO decoder to load the corresponding hard-decision-based binary $+1$ or -1 chip values into the delay units of the m-sequence generator, according to the signs of the corresponding LLR values stored in the SCDUs.

The operation of the RSSE acquisition scheme can be summarized in the following steps.

1) All the SCDUs are initialized to zeros.
2) Whenever the SISO decoder receives a channel output sample Z_i corresponding to the chip c_i, the SISO decoder computes the LLR of c_i conditioned on Z_i using (3), and computes the extrinsic information of $L_e(c_i)$ using (4). Finally, the soft output $L(y_i)$ of the SISO decoder related to chip c_i is computed according to (5).
3) The soft output $L(y_i)$ is then shifted into the left-most SCDU of Fig. 1 after all the other soft outputs $L(y_{i-1})$, $L(y_{i-2})$, $L(y_{i-S+1})$ have been shifted to the right by one position, while $L(y_{i-S})$ is removed from the soft-chip register. In other words, the soft-chip register always stores the most recent S number of soft outputs of the SISO decoder, which correspond to S consecutive chips of the transmitted m-sequence.
4) Following a number of recursions according to (5), when the amplitudes of the most recent S soft outputs of the SISO decoder become sufficiently high for guaranteeing a sufficiently low erroneous loading probability, a "loading command" is activated. Then, S consecutive chips are determined, using hard decisions based on the most recent S LLR values stored in the soft-chip register of Fig. 1. Then, the S consecutive binary chips are loaded into the corresponding delay units of the local m-sequence generator.
5) Once the m-sequence generator is loaded with the initial binary chip values, the received spread-spectrum signal can be despread using the locally generated m-sequence replica, provided that the initial chip values of the m-sequence generator have been correctly loaded. The despread signal is then low-pass filtered and sent to the code tracking loop. If the code tracking loop is capable of tracking the phase, the code acquisition process is completed. By contrast, if the tracking loop is incapable of tracking the phase, the code tracking loop activates a "reloading command" in order to load another group of S consecutive chips into the delay units of the m-sequence generator. The above process can be repeated until successful code tracking is accomplished.

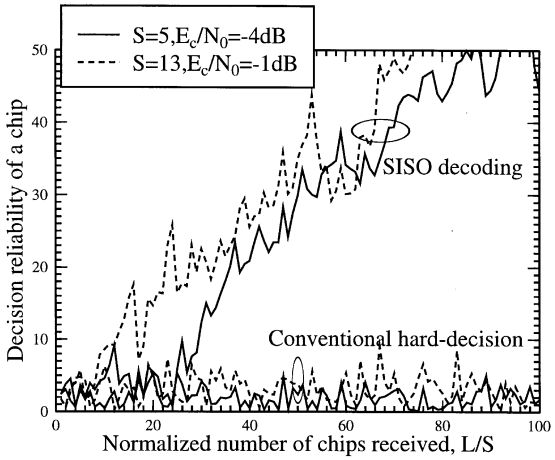

Fig. 2. Decision reliability versus the normalized number of received chips invoked in the recursive SISO decoding, when communicating over an AWGN channel and using an SNR per chip value of $E_c/N_0 = -4$ dB for $S = 5$, and $E_c/N_0 = -1$ dB for $S = 13$.

Note that since the acquisition device is capable of observing the reliabilities of the most recent S consecutive chips by observing the amplitudes of the corresponding soft outputs stored in the soft-chip register of Fig. 1, the acquisition scheme can decide when it should activate the loading command for loading the initial chips into the m-sequence generator. When the erroneous loading probability is typically deemed sufficiently low in the region of, for example, 10^{-4}, the PN sequence can be acquired with a high probability after the first loading of the initial chips. Therefore, the total acquisition time of the RSSE acquisition scheme can be approximated by the duration of time required for the RSSE to carry out the recursive SISO decoding, in order to reach a sufficiently low erroneous loading probability.

IV. Simulation Results

In this section, we provide a range of simulation results in the context of the proposed RSSE acquisition scheme. Our simulation results were mainly based on the acquisition of an m-sequence having the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$, which corresponds to having a period of $N = 2^{13} - 1 = 8191$. Note that the curves were drawn either versus the SNR per chip, namely, E_c/N_0, or versus the normalized number of chips received, which also represents the normalized number of chips that the SISO decoder processed. The normalized number of chips L/S was defined as the total number of received chips, L, divided by the number of generator stages, S, of the corresponding m-sequence generator.

Fig. 2 shows the reliability associated with correctly deciding the polarity of a specific chip of an m-sequence, when the m-sequence was transmitted over AWGN channels. The decision re-

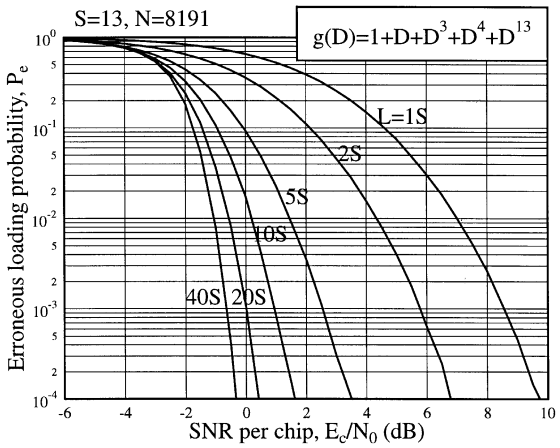

Fig. 3. Erroneous loading probability P_e versus the SNR/chip E_c/N_0 performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channels.

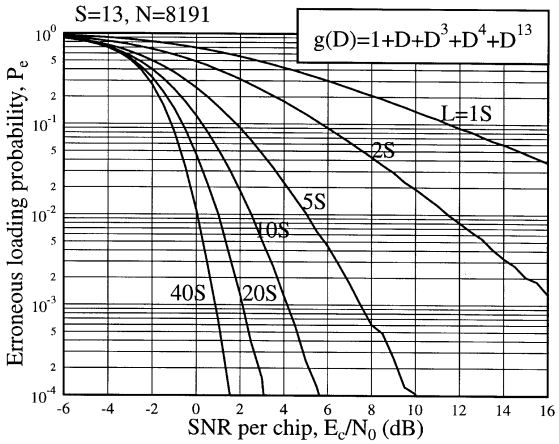

Fig. 4. Erroneous loading probability P_e versus the SNR/chip E_c/N_0 performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over Rayleigh fading channels.

liability associated with using SISO decoding was defined as the absolute value of the SISO decoder's output, evaluated according to (5) in the context of each chip received. By contrast, for conventional hard decision, the decision reliability associated with the decision concerning the polarity of a specific chip was defined as the absolute value of the channel output corresponding to that chip. From the simulation results of Fig. 2, we observe that for the conventional hard-decision-based scheme, the decision reliability associated with a chip is mainly distributed within the range of 0–10, and does not increase as more chips are received, since the polarity of each chip is decided separately. By contrast, for the proposed RSSE acquisition scheme, the correct decision reliability increases when receiving more chips from the channel. Therefore, according to Fig. 2, we expect that the RSSE acquisition scheme will outperform the conventional sequential estimation acquisition scheme [3] without exploiting the *a priori* information provided by the previous chips. Furthermore, we observe that the average correct decision reliability increases nearly linearly upon increasing the normalized number of chips received. This is because the proposed recursive SISO decoder is capable of efficiently exploiting the *a priori* information provided by the previous chips received. The following results will support this argument.

Fig. 3 shows the acquisition performance of an m-sequence having a period of $N = 8191$ chips, which was generated by a 13-stage $(S = 13)$ generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. As shown in Fig. 3, the m-sequence can be reliably acquired at an SNR per chip value of $E_c/N_0 = -0.5$ dB by invoking about $L = 40S = 40 \times 13 = 520$ chips into the recursive SISO decoder. By contrast, without using any *a priori* information, i.e., using the conventional sequential estimation acquisition scheme [3], the PN code acquisition scheme has to operate at the SNR per chip value of $E_c/N_0 = 9.5$ dB in order to achieve the erroneous loading probability of 10^{-4}. Hence, the SNR per chip gain of using the proposed RSSE acquisition scheme instead of the conventional sequential estimation acquisition scheme at the erroneous loading probability of 10^{-4} is about 10 dB, when $L = 520$ chips are invoked into the recursive SISO decoder. Let τ_D represent the integration dwell time in the context of a conventional serial search-based acquisition scheme [1], which typically assumes values from tens to hundreds of chip intervals. In [1], it is shown that the mean acquisition time of a conventional serial search-based acquisition scheme cannot be lower than $N\tau_D/2 = 4095\tau_D \gg 520$ chips for a sequence of length 8191, even if the SNR per chip value is sufficiently high, when the corresponding detection probability approaches one. Hence, the proposed RSSE acquisition scheme significantly outperforms the conventional serial search-based acquisition scheme in terms of the achievable acquisition time performance.

The results in the above figures were evaluated when communicating over AWGN channels. In Fig. 4, we investigated the acquisition performance of the RSSE acquisition scheme for transmission over Rayleigh fading channels. From the results of Fig. 4, we observe that at a given SNR per chip value of E_c/N_0, similar to the results of Fig. 3, the erroneous loading probability decreases when increasing the number of received chips invoked into the recursive SISO decoder. Furthermore, by comparing the results of Fig. 4 to those of Fig. 3, valid for communicating over AWGN channels, it can be shown that for a given number of received chips invoked into the recursive SISO decoder, the achievable SNR gain over Rayleigh fading channels is significantly higher than that over AWGN channels, when using the proposed RSSE acquisition scheme instead of the conventional sequential estimation acquisition scheme. However, for a given number of received chips used by the recursive SISO decoder and for a given SNR per chip value, the acquisition scheme communicating over AWGN channels achieves a lower erroneous loading probability than that over Rayleigh fading channels.

Finally, in Fig. 5, we show the erroneous loading probability performance versus the normalized number of received chips used by the recursive SISO decoder for an m-sequence generated by an $S = 13$-stage m-sequence generator, and hence, having a period of 8191 chips. The results were generated for transmissions over both AWGN and Rayleigh fading channels at the SNR per chip value of $E_c/N_0 = -1$ dB. According to

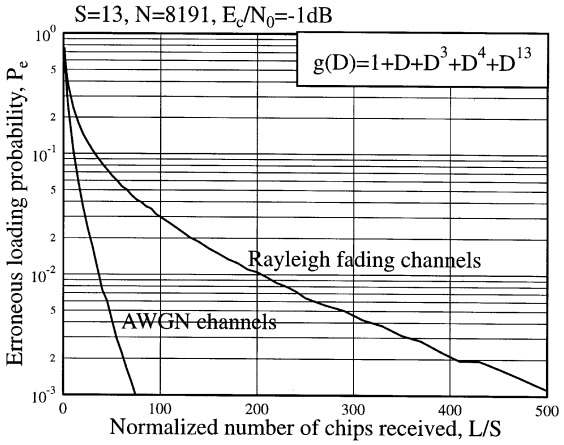

Fig. 5. Erroneous loading probability P_e versus the normalized number of received chips invoked into the proposed recursive SISO decoder for an m-sequence having a period of 8191, when communicating over AWGN or Rayleigh fading channels and using an SNR per chip value of $E_c/N_0 = -1$ dB for $S = 13$.

the results of Fig. 5, it can be shown that for AWGN channels, the RSSE acquisition scheme is capable of achieving an erroneous loading probability of 10^{-3} after receiving approximately $80 \times 13 = 1040$ chips. By contrast, when communicating over Rayleigh fading channels, the RSSE acquisition scheme is capable of achieving the erroneous loading probability of 10^{-3} after receiving approximately $500 \times 13 = 6500$ chips. These results imply that with the aid of the proposed recursive SISO decoder, the required target performance can be achieved, regardless of the specific communication environment encountered by invoking a corresponding number of chips into the SISO decoder. The results of Fig. 5 indicate that successful acquisition can be achieved by the proposed RSSE acquisition scheme, when communicating over Rayleigh fading channels at $E_c/N_0 = -1$ dB within about 6500 chips, a value which is still significantly lower than the required $4095\tau_D$ chip duration of the best mean-acquisition time associated with the conventional serial search-based acquisition scheme [1].

V. Conclusions

In summary, in this letter, the acquisition of m-sequences using the proposed RSSE scheme has been investigated. It has been shown that the RSSE acquisition scheme has both an implementational complexity and an initial synchronization time, which are linearly dependent on the number of stages in the m-sequence generator. In terms of these characteristics, the RSSE acquisition scheme outperforms both the family of conventional serial search-based acquisition schemes and the class of conventional parallel search-based [2] acquisition schemes, which either result in a mean-acquisition time or impose an implementational complexity, that are exponentially dependent on the number of stages in the m-sequence generator.

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