

## A Physically Based Relation Between Extracted Threshold Voltage and Surface Potential Flat-Band Voltage for MOSFET Compact Modeling

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**Abstract**—Compact MOS models based on surface potential are now firmly established, but for practical applications there is no reliable link between measured values of threshold voltage and the flat-band voltage on which such models are based. This brief presents an analytical relationship which may be implemented in compact models to provide a reliable and accurate threshold parameter input. Results are compared with a conventional threshold voltage model for several SOI CMOS technologies. This technique has been developed for use with body-tied SOI transistors, and hence it can also be applied to bulk devices.

**Index Terms**—Modeling, MOSFET, threshold voltage.

### I. INTRODUCTION

Many methods have been proposed to extract the threshold voltage of a MOSFET experimentally [1]–[5]. Irrespective of the extraction technique used, the measured threshold voltage  $V_{\text{Tex}}$ , is conventionally set equal to  $V_{\text{TH}}$ , the threshold voltage corresponding to the classical criterion for strong inversion [1]

$$V_{\text{TH}} = V_{\text{FB}} + \psi_{\text{si}} + \gamma\sqrt{\psi_{\text{si}} + V_{\text{SB}}} \quad (1)$$

where

$V_{\text{FB}}$	flat-band voltage;
$\gamma$	body factor;
$V_{\text{SB}}$	source-body voltage;
$\psi_{\text{si}}$	surface potential at the onset of strong inversion, usually defined as

$$\psi_{\text{si}} = 2\phi_F \quad (2)$$

where  $\phi_F$  is the Fermi potential.

It is generally recognized that  $V_{\text{Tex}}$  will not correspond exactly to  $V_{\text{TH}}$ ; the degree to which  $V_{\text{Tex}}$  and  $V_{\text{TH}}$  differ will depend partly on the extraction technique used to obtain  $V_{\text{Tex}}$ . Compact models based on device surface potential (MISNAN [6], SUSOS [7], SOISPICE [8], STAG [9], and others [10], [11]) avoid such ambiguity by using the flat-band voltage, which has a clear physical definition, to determine the level of inversion in a device. However, in practise the flat-band voltage is difficult to extract experimentally, and a common alternative is to extract a value for the threshold voltage and then obtain the flat-band voltage using (1). Using an unmodified value of  $V_{\text{Tex}}$  in this way will often result in quite large deviations from the correct flat-band voltage, which in turn leads to poor characteristic matching.

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It has been proposed [2] that a more accurate correspondance between measured and theoretical threshold voltages can be obtained by subtracting several  $\phi_t$  from  $V_{\text{Tex}}$ , where  $\phi_t$  is the thermal voltage. However, the main objection to this approach is that it lumps all the errors into a single correction factor, so that it is impossible to separate out different contributions to the threshold shift between  $V_{\text{Tex}}$  and  $V_{\text{TH}}$ .

In this brief, we describe how the flat-band voltage can be closely related to the measured threshold voltage by means of a simple physically based expression, thereby eliminating a source of uncertainty and error in the practical application of surface potential-based models. When evaluating our new threshold relation, we will be using the linear extrapolation technique as a reference method, since it is a well-known and widely-used technique [1]–[3].

### II. QUALITATIVE FEATURES OF NEW THRESHOLD MODEL

In order to derive a more satisfactory relationship, several adjustments must be made to the standard treatment. These can be summarized in the following three statements.

- 1) Since experimental threshold voltage extractions are made using a nonzero drain voltage, the new treatment must account for the influence of a finite drain voltage on the measured threshold voltage. We will use  $V_{\text{Dex}}$  to designate the drain voltage at which  $V_{\text{Tex}}$  is extracted.
- 2) The new treatment must also account for the fact that the value of the extracted threshold voltage usually corresponds to a surface potential which has a value greater than  $2\phi_F$ . For this purpose, we will use an empirical parameter  $\delta_0$ , which expresses the additional surface potential as an fraction of  $\phi_F$ . The optimal value of  $\delta_0$  will vary between different extraction techniques and process technologies; as a result, analytic derivation of  $\delta_0$  is not possible. We shall show in this study how it is possible to minimize the range of values which  $\delta_0$  can take, by using the new model to account for the different contributions to the threshold shift. In this way, empirical optimization can be kept to an absolute minimum.
- 3) Finally, when deriving the standard relation given in (1), it is assumed that the inversion charge is negligible compared with the body charge. This is valid when the surface potential is equal to  $2\phi_F$ , but beyond this point, the inversion charge will rapidly become comparable to the body charge. It is therefore not valid to discount the influence of this charge component, especially for larger values of  $\delta_0$ .

### III. DERIVATION OF NEW MODEL

We will derive the new relation for the case of a body-tied NMOS SOI MOSFET, so that  $V_{\text{SB}} = 0$ . A small measurement drain voltage  $V_{\text{Dex}}$  is applied to the device. Applying Gauss' law across the front gate provides us with the standard relation

$$V_{\text{GFS}} = V_{\text{FB}}^f + \psi_s(y) - \frac{q_{\text{tot}}(y)}{C_{\text{of}}} \quad (3)$$

where

$V_{\text{GFS}}$	front gate voltage referred to the source/body;
$V_{\text{FB}}^f$	SOI front-gate flat-band voltage;
$\psi_s$	surface potential;
$q_{\text{tot}}$	total body charge density.

These last two quantities are functions of channel position, as a result of the applied drain voltage.

Let us now consider the new form of  $\psi_{si}$ , the strong inversion surface potential corresponding to  $V_{Tex}$ . Statements 1 and 2 in Section II outline the two primary mechanisms by which  $\psi_{si}(V_{Tex})$  and  $\psi_{si}(V_{TH})$  differ. Since the presence of a drain bias makes the surface potential dependent on channel position, we simplify the treatment by averaging  $V_{Dex}$  over the entire channel. To account for the shift in surface potential due to  $V_{Dex}$ , we recall that in strong inversion, the drain voltage can be added to the gate induced surface potential [2]. This yields the following form for  $\psi_{si}$ :

$$\psi_{si} = (2 + \delta_0)\phi_F + 0.5V_{Dex}. \quad (4)$$

The surface potential corresponding to  $V_{Tex}$  is a constant value, which is necessary since  $V_{Tex}$  is itself independent of channel position. The next step is to derive an expression for  $q_{tot}$  which is also position independent. Because we cannot neglect the inversion charge (Statement 3 in Section II), it is insufficient to simply approximate  $q_{tot}$  using the expression for the body charge density, as is done in the standard treatment. Instead, we solve the 1-D form of Poisson's equation in the vertical direction [2], and by again averaging the drain voltage over the channel, we obtain the following result:

$$q_{tot} = -\gamma C_{of} \sqrt{\psi_{si} + \phi_t \exp\left(\frac{\psi_{si} - 2\phi_F - 0.5V_{Dex}}{\phi_t}\right)}. \quad (5)$$

Under the new strong inversion condition (3) can be written as

$$V_{Tex} = V_{FB}^f + \psi_{si} - \frac{q_{tot}}{C_{of}}. \quad (6)$$

Substituting (4) and (5) into (6) and rearranging gives us the final result

$$V_{FB}^f = V_{Tex} - \psi_{si} - \gamma \sqrt{\psi_{si} + \phi_t \exp\left(\frac{\delta_0\phi_F}{\phi_t}\right)} \quad (7)$$

where  $\psi_{si}$  is defined in (4). For a particular measured device, with a set value of  $V_{FB}^f$ , we would therefore expect  $V_{Tex}$  to increase as  $V_{Dex}$  is increased.

#### IV. EXPERIMENTAL EVALUATION OF MODEL

Whilst  $V_{Tex}$  and  $V_{Dex}$  can readily be obtained from measurement data and substituted directly into in (7), finding an appropriate value to use for  $\delta_0$  is less straightforward. This parameter can be expected to vary between different process technologies and extraction techniques; however, we can attempt to set ranges on  $\delta_0$  for a given extraction procedure. This was done for the linear extrapolation technique, by testing against a number of different process technologies, and the range of  $\delta_0$  was found to be between 0.05 and 0.1. The main cause of this variation in  $\delta_0$  was differences in the vertical field mobility degradation, to which the linear extrapolation method is susceptible [5]. The range was found to be valid for both NMOS and PMOS devices, although for any given technology, NMOS and PMOS usually had different optimal values of  $\delta_0$ . From this range, we can set a minimum default value of 0.05 for  $\delta_0$ , which we then use as an initial estimate whenever  $V_{Tex}$  is obtained using the linear extrapolation method.

With  $\delta_0$  set, we can now evaluate the accuracy of the new threshold relation. Measured threshold voltages, extracted for a number of different process technologies, were used directly in a surface potential-based compact SOI model, STAG [9], to reproduce measured  $I_{ds}$ - $V_{gs}$  curves. Figs. 1 and Fig. 2 compare the new and standard treatments against experimental data, for two technologies. In each case, the new treatment shows a clear improvement over the standard model. Empirical selection of a standard default value for  $\delta_0$ , combined with the new drain voltage model, allows us to close much of the gap between

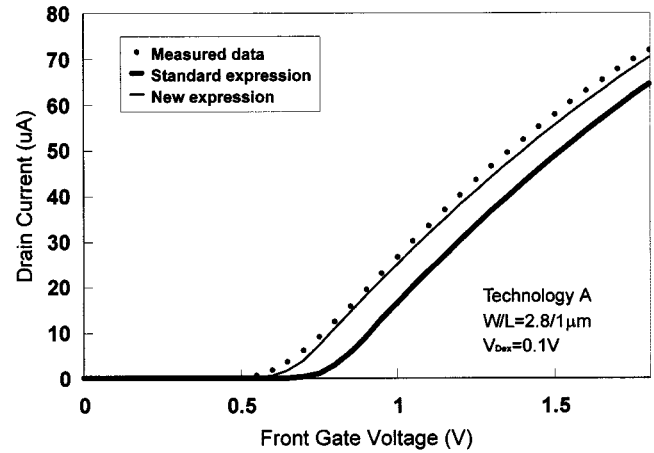


Fig. 1. Comparison of measured data with simulation results using new and standard threshold relations (Technology A).

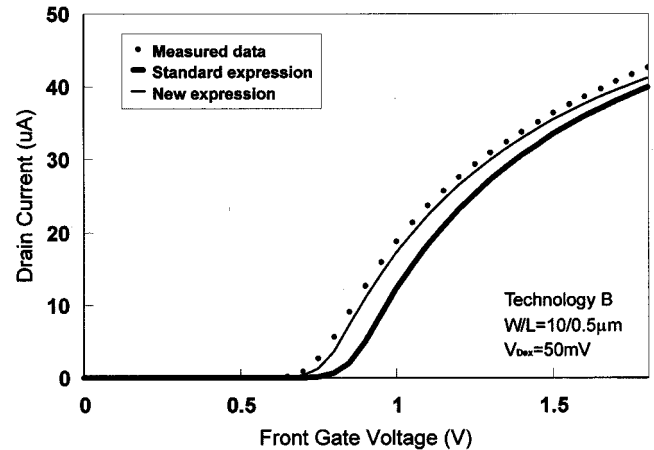


Fig. 2. Comparison of measured data with simulation results using new and standard threshold relations (Technology B).

$V_{TH}$  and  $V_{Tex}$  without resorting to optimization. Any adjustment of  $\delta_0$  to further improve the fit can therefore be made within a much tighter range of values than would otherwise be the case. Of course, there are other extraction methods for which the range of  $\delta_0$  will differ from that of our chosen technique. However, once a range is established for a given technique, and a minimum default value deduced, a similar level of accuracy can be achieved, with optimization of  $\delta_0$  only being required for final fine tuning.

In order that  $\delta_0$  can be confined to a small range of values, it is important that other effects which can also act to shift the threshold voltage are accounted for separately, otherwise these contributions will be lumped into  $\delta_0$ . Such effects include charge sharing [1], and polysilicon gate depletion [12]. For the work described in this brief, these additional effects have been accounted for where appropriate.

That the model does succeed in accounting for the effect of the measurement drain voltage can be demonstrated using Fig. 3. Each of the experimental curves plotted on the figure was obtained by applying a different drain voltage  $V_{Dex}$  when performing the measurement, and from each curve we can extract a corresponding value for  $V_{Tex}$ . Not only do the results agree qualitatively with the new theory, insofar as  $V_{Tex}$  does indeed go up with increasing  $V_{Dex}$ , but there is excellent quantitative agreement as well. Starting with an optimized value of  $\delta_0 = 0.08$ , it is possible to reproduce all of the measured curves very precisely, using any one of the five pairs of  $V_{Tex}/V_{Dex}$  values. In

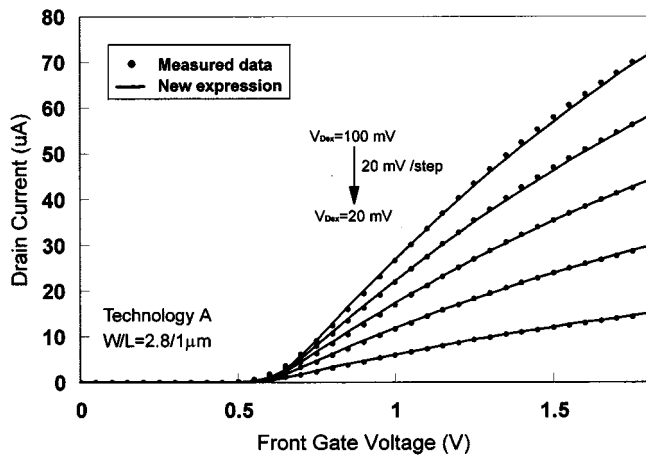


Fig. 3. Comparison of measured data with simulation results using the new threshold relation, showing accurate relation between extracted threshold voltage and applied drain voltage.

other words, we can use (7) to model very accurately the variation of  $V_{\text{Tex}}$  with  $V_{\text{Dex}}$ , and be confident that any remaining discrepancy between actual and calculated flat-band voltages can be compensated for by finding the optimal value of  $\delta_0$  for that process.

One restriction which applies to both the standard and new threshold relations is that only small drain voltages should be used when performing threshold extraction measurements, with an upper limit of  $\sim 0.1$  V applying in both cases. In the standard treatment, this is necessary in order to justify neglecting the effect of drain bias on the surface potential. In the new treatment,  $V_{\text{Dex}}$  must be kept small because extracted threshold voltages typically correspond to a surface potential only slightly greater than  $2\phi_F$ . A larger drain voltage will cause the drain end of the channel to move from strong to weak inversion. We have assumed strong inversion throughout the channel in order to obtain (4), because adding the averaged channel voltage to the gate induced surface potential becomes progressively less accurate as more of the device enters weak inversion. At even higher drain biases, the drain-induced barrier lowering (DIBL) effect will become dominant [13], and the threshold voltage will then decrease with increasing drain voltage.

## V. CONCLUSIONS

A new relationship between extracted threshold voltage and the flat-band voltage for use in surface potential-based compact MOS models has been presented, and a procedure for its implementation in

an extraction-modeling design flow outlined. One empirical parameter is used, which can often be taken as a fixed default value without major error. The results show that much better agreement is obtained, and the influence of drain-source voltage in particular is handled well. Predictions have been compared with measurement using body-tied devices from several foundries, implying that the method is also usable for bulk CMOS technology.

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