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Raised source/drains for 50 nm MOSFETs using a silane/dichlorosilane mixture for selective epitaxy

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Abstract

A selective epitaxy process for raised sources and drains is investigated, with growth performed at a pressure in the 1 Torr regime, rather than the more common CVD (10's of Torr) or UHV–CVD (1–40 mTorr) regimes. It is shown that selective growth can be achieved using a mixture of silane and dichlorosilane without any requirement for Cl_2 or HCl in the gas stream. The selectivity of the process can be controlled by varying the silane:dichlorosilane ratio in the gas mixture, with a ratio between 1:1 and 3:1 giving selective growth. Facet-free selective epitaxy is achieved, the process is selective to silicon nitride and a growth activation energy of 2.4 eV is obtained. Raised source/drain MOSFET devices with channel lengths down to 50 nm have been fabricated and the thickness of the selective epitaxial silicon layer has been varied to investigate the effect of this parameter on device performance. Excellent sub-threshold characteristics are obtained and the sub-threshold slope, S, improves from 102 to 81.9 mV/dec as the raised source/drain thickness is increased from 50 nm to 100 nm. The raised source/drain also improves threshold voltage roll-off and drain induced barrier lowering. A decrease in both I_{on} and I_{off} is seen with increasing RSD thickness, but the overall I_{off}/I_{on} trade-off is unchanged.

Keywords: Raised source/drain; Selective epitaxy; Silicon epitaxy; MOSFETs

1. Introduction

As MOSFET devices are scaled to decananometer dimensions, good control of short channel effects requires the formation of increasingly shallow junctions [1]. This scaling of the source/drain junction depth leads to undesirable increases in the parasitic series resistance of the source and drain. While increases in source/drain series resistance can be moderated by decreasing the thickness of the sidewall spacer, this has the disadvantage of degrading short channel performance because the highly doped source/drain diffuses beneath the spacer and over-dopes the extension. Raised sources and drains offer an increasingly attractive solution to these problems because the elevation of the source and drain suppresses the sub-diffusion of the source/drain dopant beneath the sidewall spacer [2–4], allowing the spacer to be thinner while maintaining short channel performance.

Selective silicon epitaxy is key to the realisation of raised sources and drains, and this can be achieved in a number of different ways. Several groups [2,5–7] have exploited the 'incubation period' to achieve selective

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epitaxial growth using SiH_4 as the source gas. While such processes are chlorine-free, they require a high temperature to achieve selective growth. For raised sources and drains, a low growth temperature is needed to avoid diffusion of the LDD and pocket implants during epitaxy. Furthermore, the achievement of selective epitaxy with a sidewall nitride spacer is difficult to achieve with SiH_4. Selective growth to silicon nitride has been reported by several groups [8–10] using a variety of gas chemistries such as $Si_2H_6/H_2/Cl_2$, Si_2H_6/Cl_2 and $SiH_2Cl_2/HCl/H_2$. However, these processes utilise the addition of Cl_2 or HCl to adjust the selectivity. In this approach, Cl_2 or HCl is used in the growth process and the selectivity is controlled by varying the amount of Cl_2/HCl in the gas stream. The minimisation of the Cl_2/HCl content is desirable because degradation of the surface quality is obtained for high Cl_2/HCl contents and because processes with Cl_2 or HCl are susceptible to loading effects [11,12].

The majority of growth processes reported in the literature operate in one of two pressure regimes. UHV–CVD and UHV–RTCVD growth processes use very low growth pressures in the 1–40 mTorr range [10] to take advantage of the ultra-clean environment in a UHV system. Alternatively, CVD growth systems used in many production epitaxy processes tend to operate in the tens of Torr pressure regime [11]. In this paper, a selective growth process for raised sources and drains is investigated in which the growth is performed in the 1 Torr pressure regime. It is shown that selective growth can be achieved using a mixture of silane and dichlorosilane, without using Cl_2 or HCl directly and that the selectivity of the growth can be tuned by varying the proportion of silane and dichlorosilane in the gas mixture. The process is shown to be facet-free and selective to silicon nitride gate spacers. This selective epitaxy process is used to implement raised sources and drains in 50 nm MOSFETs, which are shown to have excellent electrical characteristics. The thickness of the raised source/drain is varied and the effect on transistor short channel performance is characterised.

2. Selective epitaxy using a silane/dichlorosilane mixture

To investigate the effect of the SiH_4:SiH_2Cl_2 flow rate ratio on the growth rate, this ratio was varied from 0:1 to 5:1 with H_2 carrier gas constant at 100 sccm. A process temperature of 850 °C and pressure of 1 Torr were chosen as starting conditions. The growth experiments were performed on a series of silicon nitride bars and silicon windows of variable width from 2.5 μm to 20 μm to test the selectivity of the process to silicon nitride. Fig. 1 shows the growth rate as a function of silane/dichlorosilane flow rate ratio for these growth conditions. When only SiH_2Cl_2 was used in the process, the growth rate

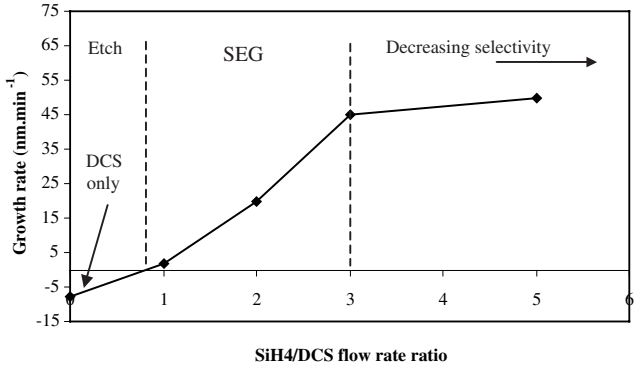

Fig. 1. Growth rate as a function of silane/dichlorosilane flow rate ratio for a growth temperature of 850 °C and a growth pressure of 1 Torr. The hydrogen carrier gas flow was constant at 100 sccm.

was negative; i.e. the excess chlorine ions in the gas phase created an etching environment. The substrate silicon was therefore selectively etched with respect to the nitride masking material. For greater SiH_4:SiH_2Cl_2 flow ratios of 3:1 and 5:1, the process becomes increasingly less selective and polysilicon begins to be deposited on the silicon nitride mask. However, for SiH_4:SiH_2Cl_2 flow ratios between 1:1 and 3:1, the growth is selective to silicon nitride. Experiments have also shown that the growth process is selective to silicon dioxide for these flow ratios.

In order to assess the effect of process temperature on selectivity, the process temperature was varied between 930 °C and 760 °C. A mixture of $SiH_4/SiH_2Cl_2/H_2$ gases was used with at flows of 10/10/100 sccm respectively. The chamber pressure remained constant throughout at 1 Torr. Selectivity was maintained throughout the entire temperature range studied. The results of these experiments are shown in the Arrhenius plot in Fig. 2. Above 900 °C, the curve shows a constant growth rate of 55 nm/min, indicating that mass transport in the gas phase is the limiting growth mechanism. Below 900 °C,

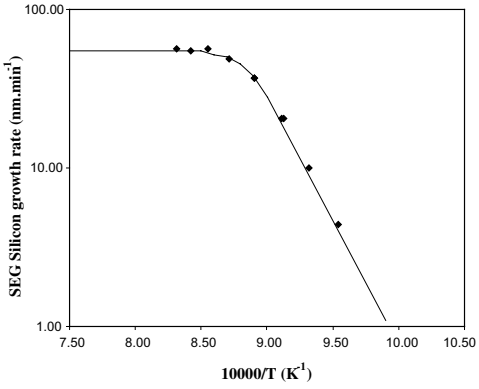

Fig. 2. Growth rate as a function of reciprocal temperature for selective silicon layers grown at temperatures in the range 760–930 °C. The growth pressure was 1 Torr and the flow rates were $SiH_4/SiH_2Cl_2/H_2$ 10/10/100.

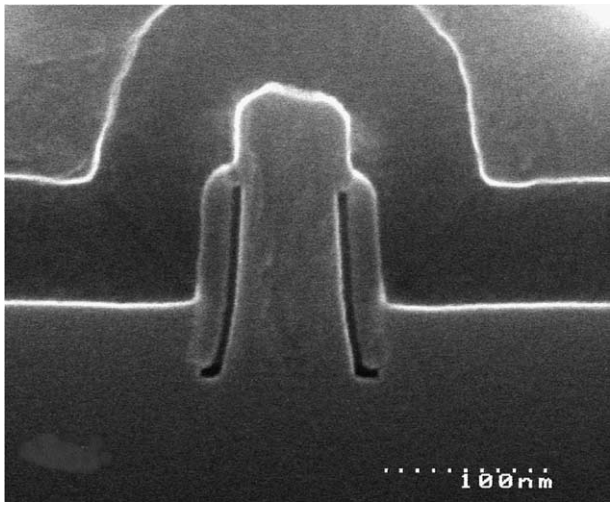

Fig. 3. Cross-sectional SEM view of an 80 nm MOSFET gate stack after raised source/drain growth. The growth was performed at 750 °C.

the growth rate decreases with decreasing temperature. This classical behaviour indicates that in this temperature range, the process is likely to be limited by a surface reaction. From this region of the curve, an activation energy of 2.4 eV (55 kcal/mol) can be calculated. This value is close to that given by Regolini et al. [8] of 2.6 eV (59 kcal/mol) who used a SiH_2Cl_2/H_2 growth process. These results suggest that the dissociation of dichlorosilane into SiHCl + HCl is likely to be the rate limiting process, since the dissociation energy of this process is 60 kcal/mol [8]. However, this growth mechanism has been achieved without the use of Cl_2 or HCl in the gas stream.

Measurements of selective epitaxial layer thickness were made in windows ranging in size from 2.5 μm to 20 μm, and the thickness was found to be constant to better than ±1%. This indicates that there are no discernable loading effects with this selective epitaxy process for the window sizes measured. The silicon growth rate for all window sizes was found to be 39.4 ± 0.4 nm/min.

Fig. 3 shows a cross-section SEM image of an 80 nm MOS transistor gate stack after the growth of a raised source/drain using $SiH_4 + SiH_2Cl_2$ in H_2 at 750 °C. It can be seen that the surface of the raised source/drain is flat, with no evidence of facets adjacent to the nitride spacer layer. Polycrystalline silicon has been deposited on top of the polysilicon gate during growth and the thickness of this layer is similar to the ≈40 nm thickness of the raised source/drain.

3. Transistor fabrication

Device processing started with the growth of a 180 nm thick LOCOS field oxide and well implantation. A 2 nm gate oxide was then grown and 150 nm of polysilicon deposited on top of this oxide to form the polysilicon gate electrode. The polysilicon was pre-doped by implantation before etch, and gates were defined by electron beam lithography. The polysilicon was then dry etched and source/drain extensions implanted.

Sidewall spacers, 25 nm thick, were created before fabrication of the raised sources and drains. Selective epitaxial silicon layers were then grown in the source and drain regions of the devices as discussed above and shown in Fig. 3. Prior to epitaxy, the wafers were cleaned using an HF etch followed by an IPA rinse [13] to give a hydrogen terminated surface. No high temperature hydrogen bake was performed prior to epitaxy and the growth was performed at 750 °C so that the total thermal budget of the process was minimized. Different growth times were used for the selective epitaxial silicon layer of 10, 8, 6 and 4 min to give a variation in the thickness of the raised source/drain (RSD). A 10 min growth gave an epitaxial silicon layer that was approximately 100 nm thick and the shorter growths gave proportionally thinner layers. After growth of the raised source/drains, the source/drain was implanted into the epitaxial silicon, and the dopants were activated by rapid thermal anneal. Device processing was completed with a back end of a BPSG inter-level dielectric and Ti/TiN/Al metallisation.

4. Electrical results

Fig. 4 shows a typical sub-threshold plot for a 50 nm NMOS transistor with a 100 nm raised source/drain. The characteristics were measured at drain/source biases of 1.5 V and 0.1 V. The transistor has an excellent characteristic, with a sub-threshold slope of 81.9 mV/dec. There is no evidence of leakage current at low drain/source bias, which indicates that there is no bridging of the epitaxy between the gate and the source/drain.

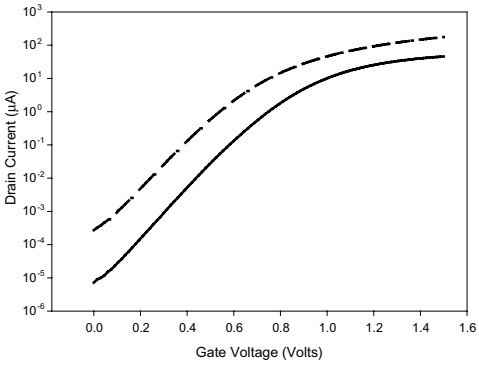

Fig. 4. Sub-threshold plot of a n-channel MOSFET with a channel length of 50 nm, channel width of 10 μm, and a 100 nm thick raised source/drain. The drain voltages for the two plots were 0.1 V and 1.5 V. Drain current is normalised to a device width of 1 μm.

No evidence of bridging was found on any of the devices measured or on any of the SEM cross-sections. DIBL at a drain bias of 1.5 V is 107 mV/V.

A plot of threshold voltage as a function of device channel length is shown in Fig. 5 for n-channel transistors with different thicknesses of raised source/drain and for a reference transistor without a raised source/drain. In all cases, the threshold voltage decreases sharply for channel lengths below about 0.2 μm due to short channel effects. The threshold voltage decrease is biggest for the reference transistor and smallest for the transistor with a 100 nm RSD. The threshold voltage decrease becomes progressively smaller as the RSD thickness increases from 40 to 100 nm. Devices with thinner epitaxial silicon layers were also measured, but the effect of the raised source/drain on the threshold voltage was small. These results indicate that the raised source/drain is suppressing short channel effects.

The threshold voltage roll-off (the difference between the threshold voltage of 50 nm devices and long channel devices) is shown in Fig. 6 as a function of the epitaxial silicon layer thickness in the raised source/drain for 50 nm n-channel transistors. The effect of the raised source/drain in reducing the threshold voltage roll-off can clearly be seen. The threshold voltage roll-off of the reference devices (with no raised source/drain structure) is 198 mV, compared to just 53 mV for the devices with the 100 nm thick raised source/drains.

Fig. 7 shows a plot of DIBL as a function of channel length for n-channel transistors with different RSD thickness. The DIBL was measured at $V_{ds} = 0.1$ V and $V_{ds} = 1.5$ V. It can be seen that raised source/drains give an improvement in DIBL performance, particularly for a 50 nm channel length. The improvement in DIBL is particularly marked for the 100 nm RSD, which has a DIBL of 107 mV/V, compared with 193 mV/V for the reference transistor.

The sub-threshold slope (S) of 50 nm devices is plotted against raised source/drain thickness in Fig. 8. The sub-threshold slopes (S) of these small devices are significantly improved by the addition of a raised source/drain. For example, the reference device has a sub-threshold slope (S) of 102 mV/dec, compared with 101.5 mV/dec, 94.8 mV/dec and 81.9 mV/dec for devices with 60 nm, 80 nm and 100 nm thick raised source/drains respectively.

Fig. 9 shows the off-current I_{off} as a function of the on-current I_{on} for n-channel transistors. I_{on} was measured at $V_{gs} = V_{ds} = 1.5$ V, and I_{off} was measured at

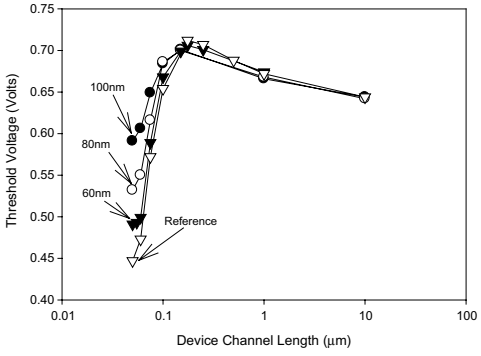

Fig. 5. Transistor threshold voltage as a function of channel length for devices with various thicknesses of raised source/drain.

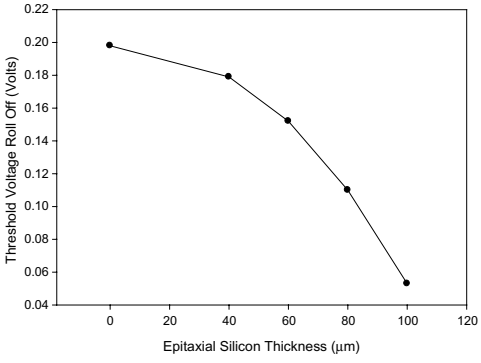

Fig. 6. Threshold voltage roll-off as a function of the thickness of the selective silicon raised source/drain.

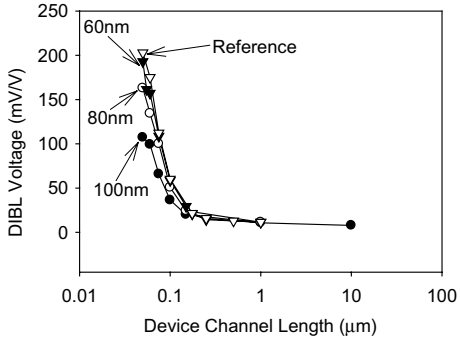

Fig. 7. DIBL voltage (in mV/V) as a function of device channel length for n-channel transistors with various thicknesses of raised source/drain. The DIBL was measured between drain voltages of 0.1 V and 1.5 V.

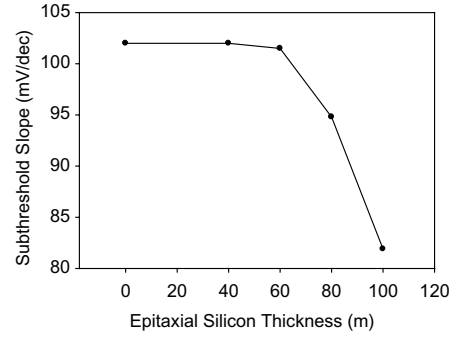

Fig. 8. Sub-threshold slope (S) as a function of raised source/drain thickness for 50 nm, n-channel transistors with various thicknesses of raised source/drain.

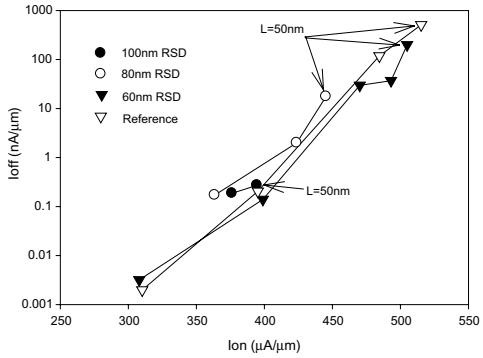

Fig. 9. Off state current, measured at $V_{gs} = 0$ V, $V_{ds} = 1.5$ V as a function of on state current measured at $V_{gs} = V_{ds} = 1.5$ V for n-channel transistors with raised source/drain thicknesses of 60, 80 and 100 nm. Devices with a channel length of 50 nm are highlighted to show how the thickness of the raised source/drain influences the I_{on}/I_{off} trade-off.

$V_{gs} = 0$ V, $V_{ds} = 1.5$ V. The 50 nm devices are marked on the graph and these devices show that while increasing the thickness of the raised source/drain reduces I_{on}, it also reduces I_{off}. However, for a given value of I_{off}, all the data lies on a single line that there is no degradation in the I_{on}/I_{off} trade-off, even for the thickest raised source/drain of 100 nm.

The above results show that the addition of the raised source/drain suppresses both the short channel effect and DIBL. This effect can be attributed to the effect of the raised source/drain (into which the source/drain implant is made) in reducing the amount of lateral diffusion of the highly doped source and drain under the sidewall spacers. This has the effect of reducing the amount of dopant diffusing into the extensions during processing. Consequently the extensions of the raised source/drain devices are shallower and more resistive than those of the silicon reference device. This effect is more marked as the thickness of the raised source drain is increased. Similar results were reported by Gwoziecki et al. [3], Lee et al. [4] and Yamakawa et al. [14] on transistors with larger geometry raised sources and drains and by Huang et al. [15] on transistors with SiGe raised sources and drains.

The above results show an increase in the steepness of the sub-threshold slope as the thickness of the raised source/drain is increased. This effect can be explained by the better gate control on the channel potential as the shallower junctions reduce the penetration of the electric field from the source and drain into the channel. This effect also accounts for the better short channel behaviour and improved DIBL. A similar improvement in sub-threshold slope S was observed by Ohguro et al. [16] in devices with channel lengths ranging from 10 μm down to 0.1 μm. In this work we saw little improvement in the device characteristics for devices with raised source/drains thinner than 60 nm. Ohguro et al. [17] also saw no improvement in DIBL for devices with 50 nm thick epitaxial layers, but better control of DIBL in devices with 100 nm thick epitaxial layers. The higher resistivity of the extensions and reduction in short channel threshold roll-off accounts for the loss of current drive in the raised devices. This can be compensated for by optimisation of the source/drain implant energy for the raised devices.

The results in Fig. 9 are very promising, and show that the inclusion of a raised source/drain gives no degradation of the overall trade-off between I_{on} and I_{off}. This result is significant for devices featuring RSD structures since it means that when an optimised source/drain implant is performed, good I_{on}/I_{off} properties are achievable. Furthermore, due to the additional silicon thickness available for salicidation, the RSD improves the compatibility of scaled devices with existing salicidation processes.

5. Conclusions

A selective epitaxy for raised sources and drains has been studied in which the growth was performed in the 1 Torr pressure regime, rather than the more common 1–40 mTorr regime used in UHV–CVD or the 10's of Torr regime used in CVD. It has been shown that selective epitaxy can be achieved using a mixture of silane and dichlorosilane, without the use of Cl_2 or HCl in the gas stream. The selectivity of the epitaxy is controlled by varying the proportion of dichlorosilane in the growth process. Pure dichlorosilane gives etching of the silicon surface, pure silane gives non-selective epitaxy and silane/dichlorosilane ratios in the range 1:1 to 3:1 give selective epitaxy. The process is facet-free and selective to silicon nitride. 50 nm MOSFETs have been fabricated incorporating raised source/drains grown using this selective epitaxy process. Devices with the raised sources and drains have improved sub-threshold slopes, reduced threshold voltage roll-off and reduced drain induced barrier lowering compared with reference transistors. This improvement in short channel characteristics increases as the thickness of the raised source/drain increases. Both I_{on} and I_{off} decrease as the thickness of the raised source/drain increases, but the overall trade-off between I_{on} and I_{off} is not degraded.

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