CMOS-compatible vertical MOSFETs and logic gates with reduced parasitic capacitance

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Abstract

This paper reports electrical results on CMOS-compatible vertical transistors and logic gates with reduced overlap capacitance. It is shown that surround-gate MOSFETs produced using the fillet local oxidation process (FILOX) have lower gate/drain overlap capacitance and consume less silicon area than comparable lateral MOSFETs. Novel logic gate structures based on partially removing the polysilicon surround gate are described and characterised.

1. Introduction

Vertical MOSFETs are potential candidates in the longer term to replace mainstream lateral devices because they offer a number of important advantages [1-3]. First, the channel length is defined using techniques other than lithography, for example epitaxy or ion implantation. Second, self-aligned double and surround gates can readily be realised with easy access to the gates. Third with surround gates, vertical MOSFETs offer increased current drive per unit silicon area [1-3]. However, vertical MOSFETs have one important disadvantage, which is higher overlap capacitances than conventional lateral devices, which has made them less competitive compared with their lateral counterpart.
Several approaches have been proposed to reduce overlap capacitance in vertical MOS devices, including selective epitaxy [4], replacement gate [5] and fillet local oxidation (FILOX) [6]. In this paper novel vertical logic gate structures are described and characterised in the surround gate FILOX process [6]. Selective removal of the surround gate to define the logic gate inputs was used to produce logic gates. Overlap capacitances are determined on transistors and gates fabricated with the FILOX process and compared with values on comparable lateral transistors. It is shown that a vertical, surround gate architecture gives a lower gate/drain overlap capacitance than obtained in comparable lateral MOSFETs and a gate/source overlap capacitance that is only slightly higher.

2. Logic gate fabrication & layout

Fig.1 shows a schematic cross-section of a vertical MOS transistor with incorporated FILOX oxide. The FILOX process gives increased oxide thicknesses on all horizontal surfaces, which isolates the gate track from the source at the bottom of the pillar and the drain at the top of the pillar [7, 8]. This dramatically reduces both, the gate/source overlap capacitance where the gate overlaps the implanted source region at the bottom of the pillar and the gate/drain overlap capacitance where the gate track overlaps the top of the pillar.

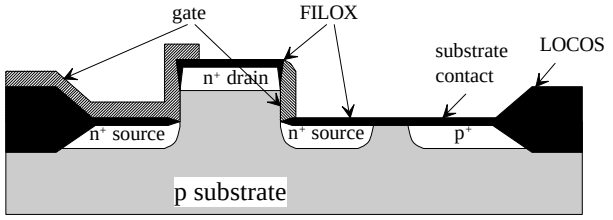

Figure 1: Cross-section of a surround gate vertical MOSFET with FILOX

Fig.2 illustrates the method used to fabricate logic gates. After the gate lithography and isotropic etch, gate fillets are left over on all vertical surfaces. In the next process step a polySi removal mask is introduced which covers portions of the pillar, depending on the type of gate required. If the whole pillar is covered, none of the gate fillet is removed and a surround gate is produced (fig.2a). If one side of the pillar is covered, a single gate is produced (fig.2b) and if two sides of the pillar are covered, a double gate is produced (fig.2c). The exposed polySi gate fillet is removed using an anisotropic polySi etch. This method allows the fabrication of single and multiple gate transistors on the same wafer and NOR and NAND gates using a variety of approaches.

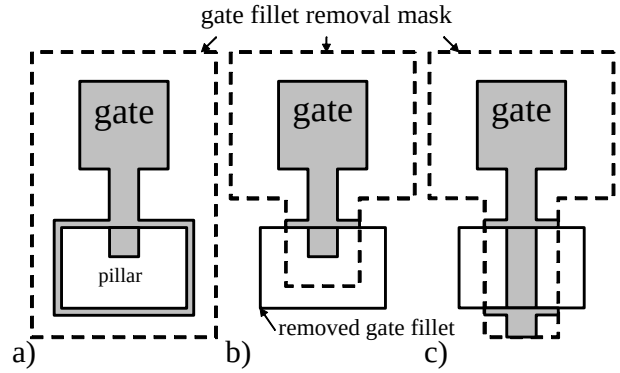

Figure 2: Top-view of a vertical MOSFET structure a) surround gate b) single gate c) double gate.

Fig.3 shows the layout of a vertical two-input NOR gate pull down circuit. The device consists of one pillar and two gates, which overlap the pillar structure from two sides. To define the two gates, the polySi removal mask was used to create polySi fillets on opposite sides of the pillar. The drain contact of this device is on the top of the pillar whilst the source and substrate contacts are at the bottom of the pillar.

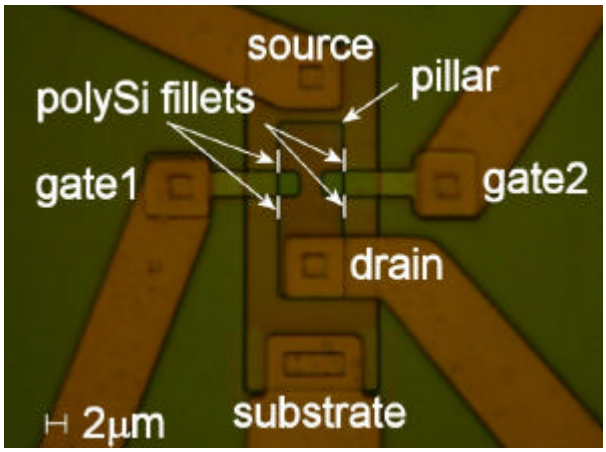

Figure 3: Top-view of a vertical NOR gate showing the gate track and polySi fillets.

Fig.4 shows the layout of a vertical two-input NAND gate pull-down circuit. This device consists of two separate pillars, with the source on top and the drain on the bottom of the first pillar and the source on the bottom and the drain on the top of the second pillar. This arrangement allows the drain of the first transistor and the source of the second to be located in a common implanted region at the bottom of the pillars.

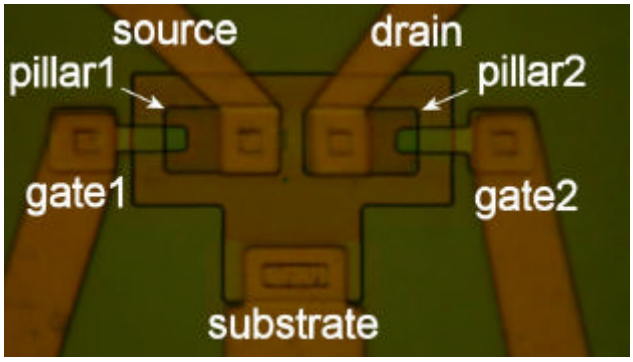

Figure 4: Top-view of a vertical NAND gate based on two pillars.

3. Results for logic gate pull-down circuits

Fig.5 shows the subthreshold characteristics for gate 1, gate 2 and for both gates of the vertical NOR gate. The characteristics of gate 1 are shifted with respect to gate 2, indicating a difference in threshold voltage. No threshold voltage control implant was used in these devices, so this difference could be due to a difference in doping or a difference in gate oxide thickness on the two sides of the pillar. A difference in gate oxide thickness could be caused by a difference in the crystallographic orientations of the two faces of the pillar due to non-symmetrical etching. The threshold voltages for gate1, gate2 and gate 1&2 were 1.24, 1.38 and 1.29V, respectively and the extracted values of subthreshold slope were 113, 114, and 114 mV/dec, respectively.

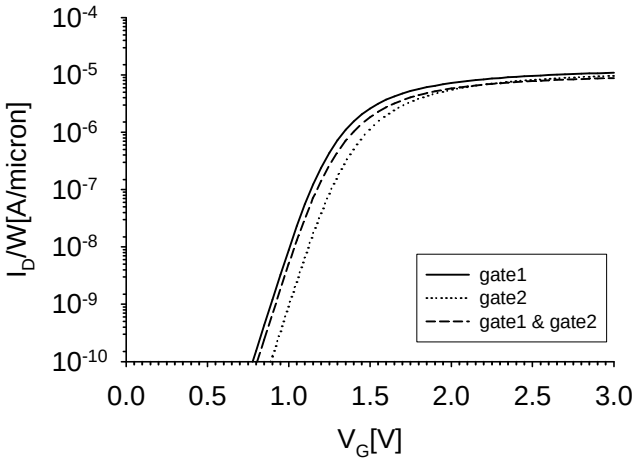

Figure 5: Subthreshold characteristic for V_{DS}=0.025V of a NOR gate vertical NMOSFET (L=105nm).

Fig.6 shows the output characteristic for the NOR gate with both gates set at 3V, with gate 1 set at 3V and gate 2 set at 0V and with gate 1 set at 0V and gate 2 set at 3V. As expected, the drain current when both gates are on is approximately equal to the sum of the individual drain currents when only one gate is on. However, the gates on the two sides of the pillar are not exactly alike, as can be seen from the different characteristics when gates 1 and two are turned on. This difference is due to the difference in threshold voltage for gates 1 and 2 as seen in fig.5.

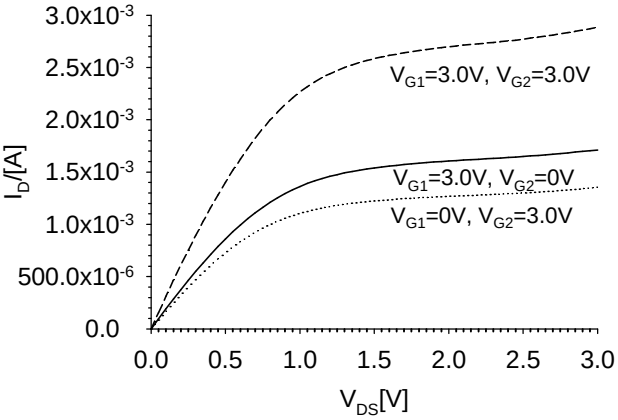

Figure 6: Output characteristic of a NOR gate vertical NMOSFET (L=105nm, W=4.5µm).

Fig.7 shows the transfer characteristics of the vertical NOR gate under consideration. For these measurements the drain was pulled to 3V using a 47kΩ resistor. There is a small asymmetry in the output characteristics for gates 1 and 2 due to the difference in threshold voltage on the two sides of the pillar, as seen in fig.5.

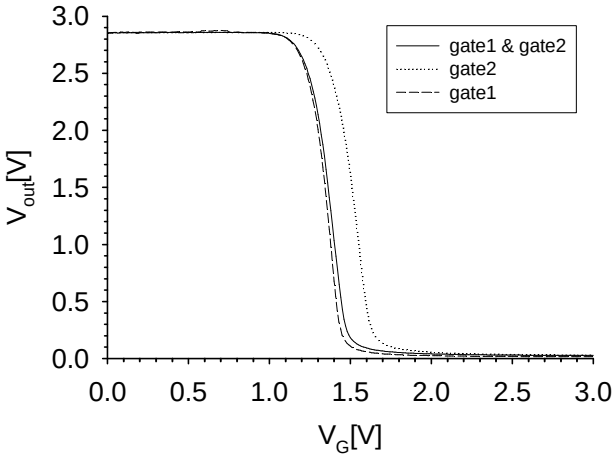

Figure 7: Transfer characteristic of a vertical NOR gate (L=105nm, W=4.5µm).

Fig. 8 illustrates the output characteristic of the vertical NAND gate for different values of gate voltage and demonstrates the expected behaviour.

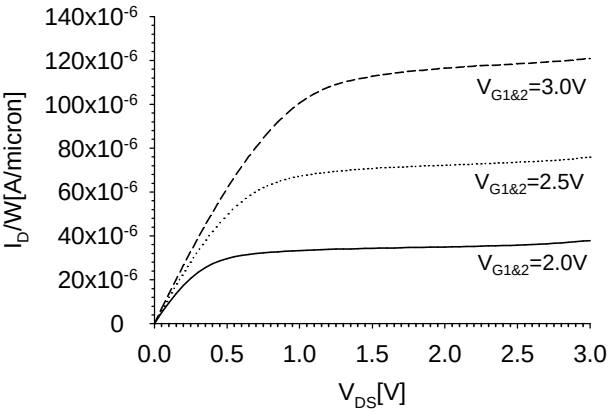

Figure 8: Output characteristic of a vertical NAND gate based on two pillars (L=2x105nm, W=32µm).

4. Characterisation of overlap capacitances

Fig.9 illustrates a SEM cross-section of a completed FILOX transistor. Several factors lead to reduced overlap capacitance. First the FILOX process increases the oxide thickness on all horizontal surfaces. Second, the nitride spacer used in the FILOX process was much thinner than the gate spacer, which allows the FILOX oxide to extend beneath the gate and reduce the gate/source overlap capacitance at the bottom of the pillar. Third, the nitride spacer was over-etched, which reduces the gate/drain overlap capacitance on the side of the pillar at the top. Fourth, the FILOX bird's beak reduces the G/D overlap capacitance on the pillar sidewall and the G/S overlap capacitance at the bottom of the pillar.

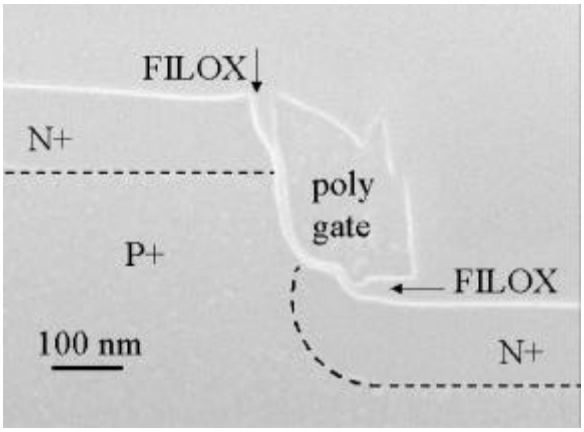

Figure 9: FESEM cross-section of a single gate vertical n-MOS structure with reduced parasitic capacitance.

To demonstrate the effectiveness of the FILOX process in reducing overlap capacitance, layouts and calculations of overlap capacitance were made for vertical and lateral MOSFETs and gates using a 100nm industrial technology as a template. Results of these calculations are shown in fig.10 for single- (fig.10a) and surround-gate (fig.10b) vertical MOSFETs.

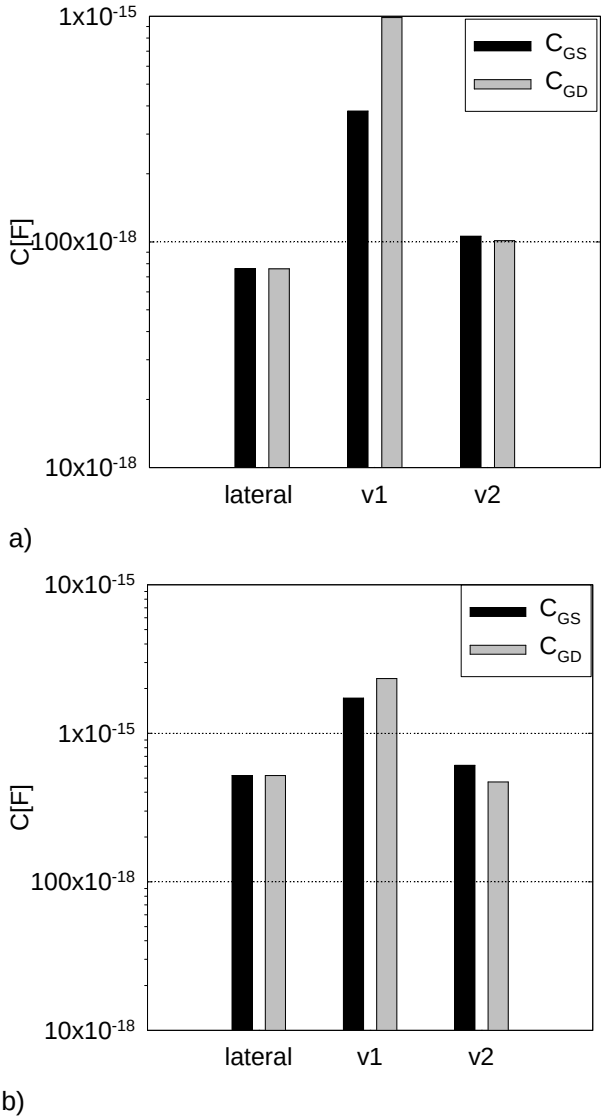

Figure 10: a) Gate/source (C_{GS}) and gate/drain (C_{GD}) overlap capacitance of a lateral, basic (v1) and optimised single gate vertical MOSFET (v2) based on 100nm design rules with W=220nm. b) Gate/source (C_{GS}) and gate/drain (C_{GD}) overlap capacitance of a lateral, basic

(v1) and optimised surround gate MOSFET (v2) based on 100nm design rules with W=1.52μm.

For the lateral transistor, gate/source and gate/drain overlap capacitances are equal due to the symmetrical arrangement of the source and drain regions. This is not the case for vertical transistors.
The FILOX single-gate vertical transistor (v2) in fig.10(a) has a 9.8 times lower gate/drain overlap capacitance than the basic vertical transistor (v1) as a result of the thicker oxide layers produced by the FILOX process. However, these values of overlap capacitance are still higher than those in the lateral transistor.
The FILOX surround gate vertical transistor in fig.10(b) has a 5.0 times lower capacitance than the basic vertical transistor (v1). Furthermore, when compared with the lateral transistor of the same channel width, the FILOX surround-gate vertical MOSFET has a 1.1 times lower gate/drain overlap capacitance and a gate/source overlap capacitance that is only 1.3 times higher. This result can be explained partly by the thicker oxide layers produced by the FILOX process and partly by the self-aligned nature of the surround gate.

5. Comparison of layout areas

Row 1 of table 1 compares the layout areas of lateral and single-gate vertical transistors with the same gate width of 0.22μm. The layout area of the single gate vertical transistor is 1.61 times higher than that of the lateral transistor, because of the extra space needed to incorporate the pillar in which the vertical transistor is produced. The single-gate vertical transistor therefore occupies more silicon area than the lateral MOSFET.
Row 2 of table 1 compares the layout areas of lateral and surround-gate vertical transistors with the same gate width of 1.52μm. In this case, the layout area of the surround-gate transistor is 1.64 times lower than that of the lateral transistor. This result can be explained by the self-aligned nature of the surround gate, which gives very efficient usage of silicon area.

Type	**Lateral** [μm^2]	**Vertical** [μm^2]	**Lateral/ vertical**
Transistor (W=0.22μm)	0.496	0.796 single gate	0.62
Transistor (W=1.52μm)	1.302	0.796 surround gate	1.64
NOR gate (W=0.22μm)	1.159	1.597	0.73
NOR gate (W=1.52μm)	2.765	1.764	1.57
NAND (W=0.22μm)	0.832	1.159	0.72
NAND (W=1.52μm)	2.184	1.159	1.88

Table 1: Device areas of lateral and vertical single and surround gate structures based on 100nm technology.

The areas of vertical and lateral two-input NOR gates are also compared in table 1 and show a larger area for short channel widths but a smaller area for long channel widths, consistent with the results for the transistor layouts. The layout areas of lateral and vertical NAND gates are also compared in table 1 and show the same trend as the NOR gate, namely a larger area for short channel widths but a smaller area for long channel widths.

6. Conclusions

We have demonstrated and characterised logic gate structures fabricated in a low overlap capacitance vertical MOSFET process. Layout areas of surround gate vertical transistors have been shown to be 1.64 times smaller than those of conventional lateral transistors with the same gate width. A similar trend is seen for NAND and NOR layouts. The low overlap capacitance FILOX surround-gate process gives lower values of gate/drain overlap capacitance than in conventional lateral transistors, and a gate/source overlap capacitance that is only slightly higher.

7. Acknowledgement

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8. References

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