A new approach to the fabrication of CMOS compatible vertical MOSFETs incorporating a dielectric pocket

E. Gili*, T. Uchino*, M. M. A. Hakim*, C.H. de Groot*, P. Ashburn*, S. Hall†
∗ School of Electronics & Computer Science, University of Southampton, Southampton, UK
Email: eg02r@ecs.soton.ac.uk
†Dep. of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UK

***Abstract*— Vertical MOSFETs built on the sidewalls of dry etched silicon pillars and with ion implanted source/drain are CMOS compatible and simple to fabricate but require high body doping concentration in order to suppress short channel effects. The incorporation of an oxide layer (called dielectric pocket) between drain and body suppresses short channel effects and allows the threshold voltage and the performance of the devices to be optimised. In this paper we propose a novel, CMOS compatible and high throughput dielectric pocket fabrication process. A thin undoped amorphous silicon layer is deposited in order to connect the drain and the channel of the MOSFET around the perimeter of the dielectric pocket. This amorphous silicon layer and the underlying silicon substrate are then anisotropically dry etched to fabricate the vertical channel of the device. This concept will allow integration of sub-100nm vertical MOSFETs in CMOS technologies with relaxed lithography rules (eg 0.35μm technology). SEM cross sections of optimised active pillars demonstrate the feasibility of this approach. Furthermore we demonstrate the role of the polysilicon drain in suppressing Transient Enhanced Diffusion and controlling the channel length of the devices.**

I. Introduction

The International Technology Roadmap for Semiconductors includes double and surround gate vertical MOSFETs (VMOSFETs) as one of the possible alternatives to extend CMOS technology to and beyond the 45nm node [1]. This approach has several advantages. First, the gate length is controlled by non-lithographic methods, allowing ultra-short channels with relaxed lithography rules and lower processing costs. Second, surround gate or double gate structures allow more channel width and drive current per unit of silicon area. Third, the channel length is decoupled from the packing density, which makes VMOSFETs suitable for DRAM and Low Leakage applications.
A common method to fabricate VMOSFETs is to dry etch silicon pillars and then define the channel length by source/drain ion implantation [2] (see figure 1A). This approach provides high throughput and is CMOS compatible but does not feature shallow source/drain extensions, pockets or threshold voltage adjustment. This enhances the short channel effects (SCEs) of the devices, giving rise to DIBL, subthreshold current degradation and bulk punchthrough. A high dose body ion implantation is required to counteract these effects, leading to several drawbacks, such as unacceptable threshold voltage values, increase of body factor, junction capacitance and junction leakage current. In the meantime, avalanche breakdown at the source/substrate junction and parasitic bipolar effects degrade the performance of the devices (see figure 1A). A possible solution is thin channel, fully depleted double gate VMOSFETs, but this approach requires aggressive electron beam lithography [3] or challenging processing [4, 5]. Another promising approach features an ultrathin vertical channel on the sidewall of an oxide pillar, achieving fully depleted operation without requiring expensive lithography techniques but at the expense of CMOS compatibility [6].
A new solution to the drawbacks of VMOSFETs is the incorporation of an oxide dielectric pocket (DP) between the drain and the body of the device (see figure 1B), as has been proposed and evaluated by numerical simulations by Donaghy et al. [7, 8]. This concept incorporated a thin silicon channel grown by epitaxy on the sidewalls of a pillar etched in a silicon-oxide-polySi stack. Unfortunately epitaxial growth is expensive, reduces throughput and is hardly CMOS compatible. In this paper we describe and demonstrate a novel concept for integration of DP in vertical MOSFETs with a CMOS compatible, low cost and high throughput fabrication process, which does not involve epitaxial growth or challenging lithography.

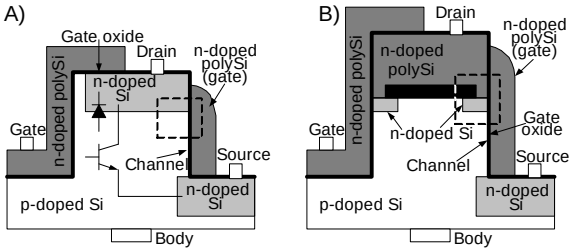

Fig. 1. Comparison of schematic cross-sections of vertical nMOSFETs with ion implanted source and drain: conventional structure (figure A) and device incorporating a DP (figure B).

II. The concept of dielectric pocket

The introduction of a DP between HDD and body was first proposed as an alternative to pocket ion implantation in order to suppress SCEs in conventional lateral MOSFETs [9]. This approach, though, increases considerably cost and complexity of the conventional CMOS fabrication process as it requires careful tuning of buried spacers overetch followed by selective epitaxial growth of source

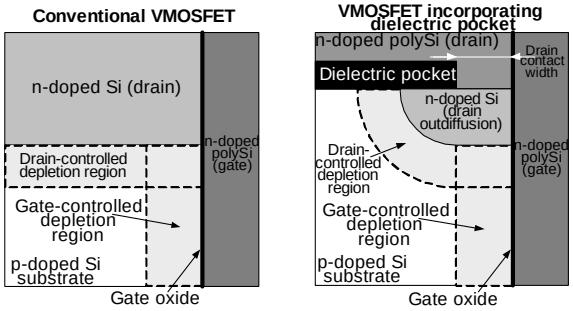

Fig. 2. Drain/channel junction of a VMOSFET incorporating DP and of a conventional VMOSFET; the figure shows the gate-controlled and the drain-controlled depletion regions in the body, assuming on-state operation ($V_D > 0$ and $V_G > V_t$); the regions represented correspond to the dotted lines in figure 1

and drain.

In VMOSFET technology the introduction of a pocket between drain and body is considerably simpler because the oxide pocket and the polySi drain of the device are deposited before pillar dry etch (see figure 1B). Figure 2 shows how the DP suppresses the SCEs. In conventional VMOSFETs [2] the absence of both source/drain extensions and pocket ion implantation leads to performance degradation when the channel length is scaled down. In the center of the transistor pillar the body potential is completely independent of the gate bias, thus giving rise to bulk punchthrough. On the contrary in the new structure the DP insulates the body of the device from the drain except for the contact region between DP and gate oxide (see figure 2). The drain outdiffusion suppresses the SCEs in the same way as shallow drain extensions in planar MOSFETs. In this way it is possible to tune the threshold voltage by reducing the body doping concentration without triggering SCEs and the other performance degradation factors described in the introduction. The DP moreover reduces significantly the area of the drain/body p-n junction (see figure 1).

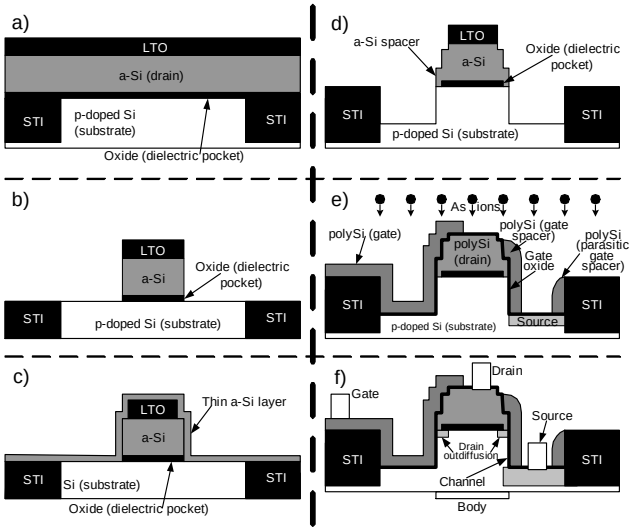

Fig. 3. Process flow of the novel fabrication process of VMOSFETs incorporating a DP.

III. Novel fabrication process of VMOSFETs incorporating a dielectric pocket

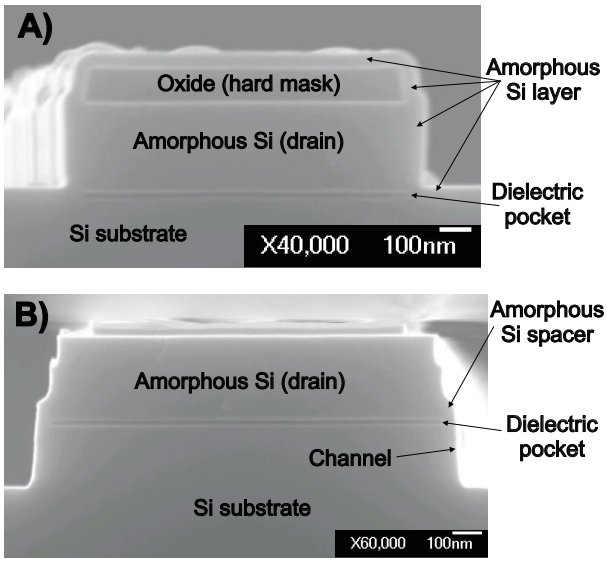

Fig. 4. SEM cross sections of the active pillar A) after the deposition of the thin amorphous Si layer (see figure 3c) and B) after channel dry etch (see figure 3d); the channel anisotropic dry etch was performed in HBr plasma with electrode power = 60W.

The process flow of the novel fabrication process of VMOSFETs incorporating a DP is summarised in figure 3. After body doping and field oxidation (STI or LOCOS), a thermal oxide/amorphous Si/LTO (Low Temperature Oxide) stack is deposited on the wafer (figure 3a). Then a hard mask is patterned in the LTO layer. After resist strip the amorphous Si and thin oxide layers are patterned by selective Si anisotropic dry etch followed by selective oxide anisotropic dry etch (figure 3b). A short wet etch in hydrofluoric acid is then performed in order to remove the native oxide from the pillar sidewall and from the horizontal Si surface. Then an undoped amorphous Si layer is deposited in a furnace by LPCVD (Low Pressure Chemical Vapor Deposition) at 560°C (figure 3c). It is worth pointing out that this is a standard, high throughput CMOS process step performed in a LPCVD furnace. An SEM cross section of the active transistor pillar at this stage of the fabrication process is shown in figure 4A. The picture shows that the drain sidewall is perfectly vertical and that the amorphous silicon layer is very uniform and conformal. This allows precise control of the drain contact width between DP and gate oxide (see figure 2) which depends on the amorphous layer thickness.

The channel of the device is patterned by anisotropic dry etch in a HBr plasma (figure 3d). The channel length can be controlled by timing the dry etch. The electrode power in the etching chamber determines the energy of the ions incident on the silicon surface. This sets the etch rate and the shape of the pillar sidewall. Figure 5 shows that if the electrode power is too low (30W in figure 5A) the sidewall is not perfectly vertical, while if it is too high (100W in figure 5B) the ions are partially reflected by the silicon surface and thus a notch forms in the sidewall underneath the DP. An intermediate electrode power (60W in figure 4B) yields

vertical sidewalls. The double step visible on the pillar sidewall in figure 4B is due to the wet etch in hydrofluoric acid performed in order to remove the native oxide before amorphous silicon deposition. Due to the low density of the LTO oxide, its etch rate is higher than that of the thermal dielectric pocket oxide. As a result in our experiment 4nm of the dielectric pocket and 25nm of the LTO hard mask were removed during wet etch. This gives rise to a step in the pillar sidewall after amorphous silicon deposition (see figure 3c) and to a double step in the drain sidewall after pillar dry etch (see figure 3d). After channel definition a sacrificial oxide is thermally grown on the pillar sidewall and then selectively removed by wet etch in hydrofluoric acid in order to eliminate the dry etch damage from the Si surface. During this step the LTO hard mask is removed from the top of the pillar. Then, after gate oxidation, a polysilicon gate is deposited and patterned by dry etch to leave sidewall spacers (figure 3e). A polySi track overlaps the pillar to ensure gate connection. The formation of parasitic gate spacers adjacent to the field oxide can enhance gate parasitic capacitance. Nevertheless, if STI (and not LOCOS) is used for field isolation, this effect can be minimised. Moreover, an extra clearance mask can be used to protect the active transistor pillar and remove these spacers by selective polysilicon etch if required. The process is completed by source/drain ion implantation (figure 3e), activation anneal (RTA) and back-end processing (figure 3f).

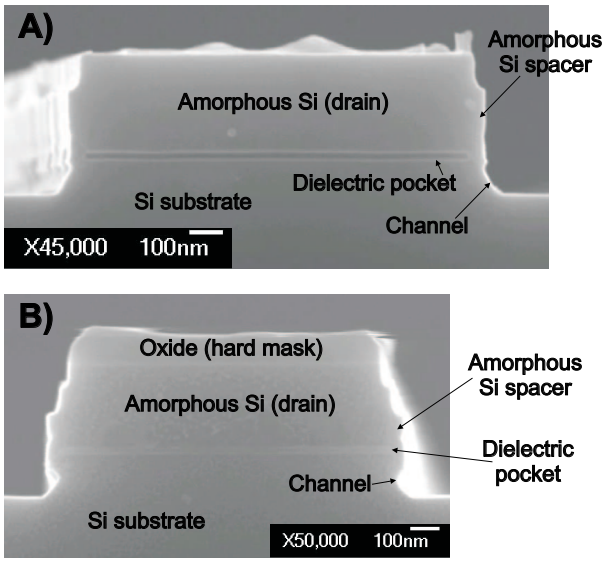

Fig. 5. SEM cross sections of the active pillar after channel anisotropic dry etch (see figure 3d) with different electrode power (P); P = 30W (figure A) and P = 100W (figure B).

The process described is fully CMOS compatible. It does not involve epitaxial growth and thus guarantees high throughput. It does not require any challenging lithography technique or non-standard processing and thus it allows devices with ultra-short channel length to be integrated in a technology with more relaxed photolithography, thereby reducing processing costs. As the thin amorphous Si layer is deposited before pillar etch (see figure 3c), the channel is etched directly in the monocrystalline silicon substrate (see figure 3d), which guarantees a good quality Si/oxide interface and Si channel. Moreover the performance of the device can be controlled by varying the thickness of the thin amorphous silicon layer during LPCVD deposition. In this way the drain contact width can be optimised, DP and shallow drain extensions suppress SCEs and the body doping concentration can be lowered for V_t adjustment.

IV. Polysilicon drain

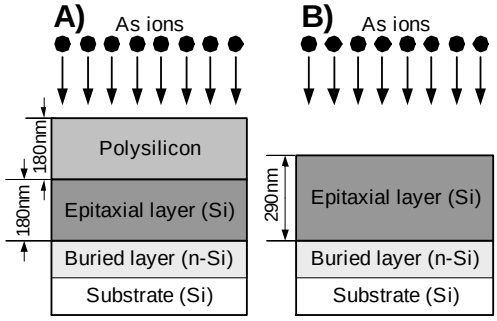

Fig. 6. Test structures fabricated in order to compare As diffusion with (figure A) and without (figure B) polySi cap layer.

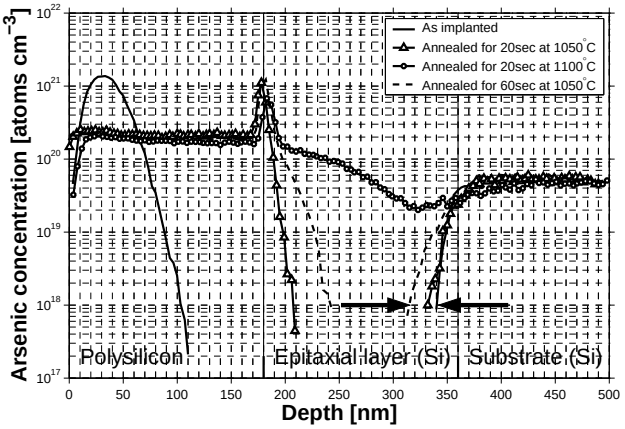

Fig. 7. SIMS profile for evaluation of As diffusion induced by RTA anneal in a test structure with polySi drain layer on top of monocrystalline silicon grown by epitaxy (figure 6A); the arrows indicate As outdiffusion from the buried layer for an anneal at 1050°C for 60 seconds.

In a vertical MOSFET incorporating dielectric pocket the drain electrode is made of polySi instead of single crystal Si as in conventional VMOSFETs (see figure 1). In the process flow described above the drain is doped by As ion implantation. In order to evaluate the suitability of this approach we compared test structures with and without polySi drain, as shown in figure 6. After buried layer ion implantation in a Si substrate and recrystallisation anneal, a monocrystalline Si layer was grown by epitaxy. Then in a process split (see figure 6A) a 180nm thick polySi layer was deposited in a furnace by LPCVD, while in the other case (see figure 6B) the epitaxial Si layer was left uncapped. This was followed by As ion implantation (4×10^{15}cm^{-2}, 50keV) and RTA anneal. Figures 7 and 8 show the As profile before RTA (labeled "as implanted") and after anneals with different conditions.

In the polySi layer, arsenic diffusion can be explained by a

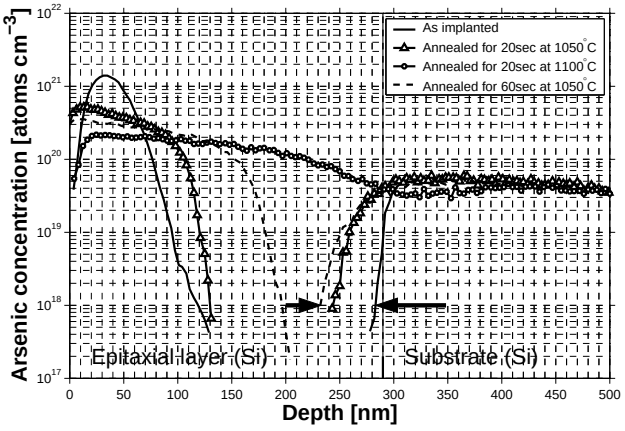

Fig. 8. SIMS profile for evaluation of As diffusion induced by RTA anneal in monocrystalline silicon grown by epitaxy without polySi cap (figure 6B); the arrows indicate As outdiffusion from the buried layer for an anneal at 1050°C for 60 seconds.

grain-boundary diffusion model. Impurity atoms that diffuse inside each crystallite have diffusivities comparable to those found in single crystal silicon. On the contrary, the diffusivity of impurity atoms that diffuse along grain boundaries can be up to 100 times larger than in a single crystal lattice [10]. As a consequence the RTA anneal is enough to diffuse the impurities throughout the polySi layer. When they reach the polySi/Si interface, the As diffusion coefficient drops dramatically. This results in a steep p-n junction for a 20 sec anneal at 1050°C (see figure 7).

Another advantage of this approach is that it allows the position of the drain-body junction to be accurately controlled. A drawback of the conventional VMOSFET architecture [2] is that, while the bottom source/body junction is self-aligned to the gate spacer, the position of the top drain/body junction is influenced both by the ion implantation profile and by dopant diffusion after RTA. On the contrary in a device with polySi drain the position of the drain/body junction is set by the position of the polySi/Si interface. The junction depth can then be tuned by choosing temperature and duration of the RTA and it is independent of the ion implantation energy.

The introduction of a polySi drain has a fundamental advantage compared to its single crystal counterpart. The drain ion implantation is performed in the polySi layer, so that the drain/body junction is formed in undamaged single crystal silicon. This should improve the quality of the junction in terms of leakage currents. Moreover, the absence of damage in the silicon substrate reduces transient enhanced diffusion. This is demonstrated by comparing figures 7 and 8. Assuming a substrate with uniform doping concentration of $1\times10^{18}\text{cm}^{-3}$, figure 7 (see arrows) shows that an anneal of 60 sec at 1050°C yields an outdiffusion of 25nm from the ion implanted buried layer if the drain ion implantation is performed in polySi (see figure 6A). In the same conditions but with drain ion implantation performed in single crystal Si (figure 6B), dopant outdiffusion from the buried layer is 55nm (see arrows in figure 8), more that double than in the polySi-capped structure. This allows better control of the channel length in sub-50nm VMOSFETs with polySi drain.

V. Conclusions

The novel fabrication concept that we have introduced in this paper is a CMOS compatible process designed to suppress short channel effects in ultra-short channel vertical MOSFETs by incorporating a dielectric pocket. It guarantees high throughput and low fabrication costs because it involves only standard CMOS fabrication process steps and it does not require epitaxial growth. Moreover, this novel concept can be implemented without any challenging lithography and thus it allows RF devices with very short channel length to be integrated in a technology with relaxed design rules (eg 0.35μm technology). In this paper we have demonstrated its feasibility through SEM cross sections of the active silicon pillar, which is patterned by anisotropic dry etch in a HBr plasma. The electrode power of the anisotropic dry etch is the key parameter to optimise the shape of the pillar sidewall. The width of the drain contact between the gate oxide and the dielectric pocket is set by the thickness of the thin amorphous silicon layer and can be optimised for suppression of short channel effects. The channel length is controlled with precision thanks to the polysilicon drain, which moreover provides a steep drain/body junction profile. Furthermore the polysilicon drain is efficient in reducing Transient Enhanced Diffusion of source/drain impurities. This has been demonstrated by SIMS profiles on test structures.

Acknowledgements

The authors would like to acknowledge the support of the European Commission for funding the SINANO project.

References

[1] *International Technology Roadmap for Semiconductors (ITRS) - Emerging Research Devices*. http://public.itrs.net, 2004.

[2] T. Schulz, W. Rosner, L. Risch, A. Korbel, and U. Langmann. Short-channel vertical sidewall MOSFETs. *IEEE Trans. Electron Devices*, 48(8):1783–1788, 2001.

[3] J. Moers, S. Trellenkamp, M. goryll, M. Marso, A. van der Hart, and S. Hogg et al. Top contacts for vertical double-gate MOSFETs. *Microelectronic Engineering*, 64:465–471, 2002.

[4] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki. Ultrathin Channel Vertical DG MOSFET Fabricated by Using Ion-Bombardment-Retarded Etching. *IEEE Trans. Electron Devices*, 2004.

[5] T.Schulz, W.Roesner, L.Risch, and U.Langemann. 50-nm Vertical Sidewall Transistors with High Channel Doping Concentrations. *IEDM Tech. Dig.*, pages 61–64, 2000.

[6] Haitao Liu and Johnny K. O. Sin. Characterization of the Ultra-Thin Vertical Channel CMOS Technology. *IEEE Trans. Electron Devices*, 51(1):106–112, January 2004.

[7] D. Donaghy, S. Hall, C. H. de Groot, V. D. Kunz, and P. Ashburn. Design of 50-nm vertical MOSFET incorporating a dielectric pocket. *IEEE Trans. Electron Devices*, 51(1):158–161, January 2004.

[8] D.C Donaghy, S. Hall, V.D. Kunz, C.H. de Groot, and P. Ashburn. Investigating 50nm channel lenght vertical MOSFETs containing a dielectric pocket, in a circuit environment. *ESSDERC Conf. Proc.*, pages 499–502, 2002.

[9] M. Jurczak, T. Skotnicki, R. Gwoziecki, M. Paoli, B. Tormen, P. Ribot, D. Dutartre, S. Monfray, and J. Galvier. Dielectric Pockets - A New Concept of the Junctions for Deca-Nanometric CMOS Devices. *IEEE Trans. Electron Devices*, 48(8):1770–1775, August 2001.

[10] S.M. Sze. *VLSI Technology*. McGraw Hill, 1988.