Effect of transition from PD to FD operation on the depletion isolation effect in vertical MOSFETs

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Abstract-**We study the effect of transition from partially depleted to fully depleted operation on the depletion isolation effect in vertical MOSFETs. The impact of the body contact during this transition is exemplified. It is found that for pillar thickness > 120 nm the body contact is effective and for pillar thickness < 60 nm is ineffective. In VMOS devices with pillar thicknesses of 60-120 nm, even though the existence of depletion isolation is identified, substrate conduction is found to reduce floating body effects and improve the breakdown voltage. We show that the reduction of the pillar thickness results in the gradual ineffectiveness of the body contact. The impact of substrate conduction on the breakdown voltage and kink behavior is also gradually reduced.**

I. INTRODUCTION

Aggressive scaling of CMOS devices has highlighted the requirement for fully depleted double or surround gate MOSFETS for decananometer Si CMOS [1]. Excellent control of short channel effects, ideal subthreshold slope and increased drive current per unit area have made these devices extremely promising for high density, low voltage, and low power DRAM, SRAM, and ULSI applications. Technologically these fully depleted double or surround gate MOSFETs can be realized using DG SOI [2], FINFETs [3] or vertical MOSFETs (VMOS) [4].

Though a major advantage of DG SOI and finfet technologies is the ease of device isolation, in most cases the body is left floating and hence these devices suffer from floating body effects. An extensive amount of work has been done on floating body effects in both partially depleted (PD) and fully depleted (FD) planar silicon on insulator (SOI) transistors [5-7]. VMOS devices have the advantage that it is easier to make a body contact and hence, the floating body effect is less severe than in planar SOI MOSFETs. But with the scaling of pillar thickness the floating body effect is also observed in VMOS devices during source on top mode of operation even if a body contact is provided [8]. This effect has been termed depletion isolation [8] and is caused by the penetration of the depletion region of the bottom drain junction towards the center of the pillar and the eventual isolation of the pillar from the body contact as shown in fig. 1(b) and also compared with planar SOI MOSFETs (fig. 1(a)). Terauchi et al [8] found depletion isolation in PD VMOS transistors and showed how this effect influenced the output and substrate current characteristics. However no work has been reported on FD VMOS transistors or on the transition from PD to FD operation and the impact of substrate conduction during this transition. In this article a comprehensive investigation of the transition from PD to FD operation on the depletion isolation is done during source on top mode of operation. Subsequently the impact of the body contact on depletion isolation is reported at various pillar thickness to gain physical insight into the behavior of thin pillar body contacted VMOS devices.

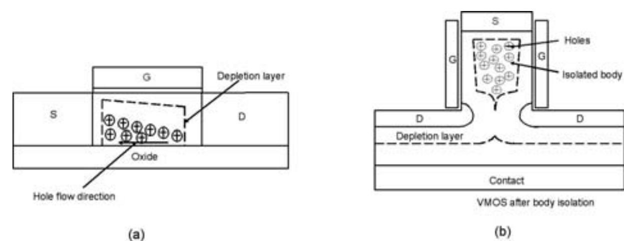

Fig. 1. Schematic cross-sectional view of a) planar SOI and b) VMOS device operated in the depletion isolated mode.

II. MODELING PROCEDURE

100 nm channel length vertical ion-implanted double gate nMOSFETs with different pillar thickness (T_{Si}) were simulated using the Silvaco Atlas device simulator [9]. The gate oxide thickness was 2 nm and the gate electrode chosen was a metal with a work function of 4.5 V. The body doping density was 10^{18} cm^{-3} and in the source/drain region a lightly doped region of 10^{19} cm^{-3} surrounded a heavily doped region of 10^{20} cm^{-3}.

A 2D coupled Poisson's drift-diffusion solver was used to investigate the device operation. The dependence of carrier mobility on the parallel and transverse fields was accounted for by using the Lombardi CVT model [9]. The mobility parameters in the simulator were calibrated against a bulk silicon transistor [9]. In particular the mobility degradation due to surface roughness arising from dry etch of vertical pillar was accounted for by adjusting the surface roughness factor in the model. It is found that satisfactory agreement between simulated and experimental values [4] are obtained when surface roughness factor of CVT model is reduced to δ(elec) = 2.91×10^{13} and δ(holes) = 1.027×10^{13}. Impact ionization (II) was modeled by the Selberherr law for the generation rate and the optimized model parameters for submicron bulk silicon transistors were used [10].

III. RESULTS & DISCUSSIONS

Fig. 2 shows output characteristics of the

simulated VMOS transistor with and without a body contact, for three different pillar thicknesses and for source on top mode of operation. In the thick pillar VMOS device with a body contact (Fig. 2(a)), ideal characteristics are obtained with no evidence of floating body effects at high drain voltages. In contrast in the VMOS device without a body contact, a breakdown kink can be seen at a drain voltage of around 4.4V, and the values of drain current are higher than equivalent values in the body contacted device at all drain voltages.

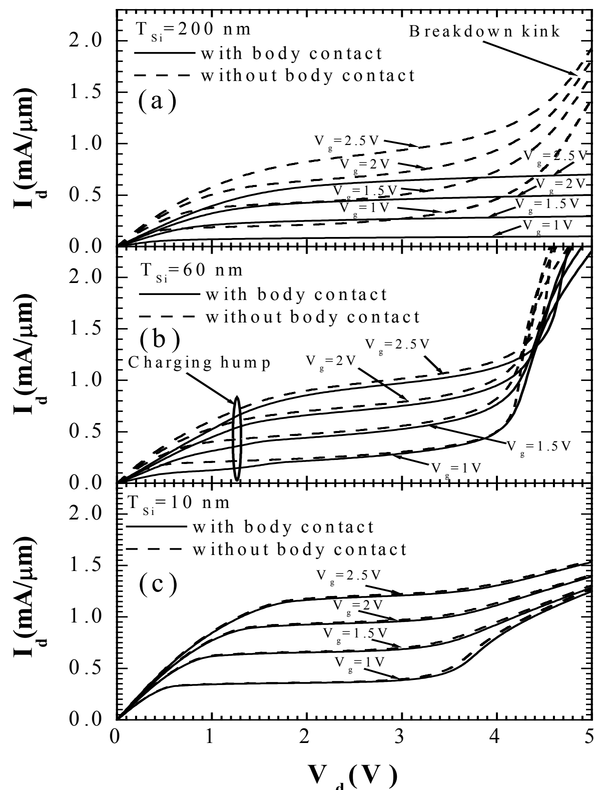

Fig. 2. Output characteristics (I_{DS} vs V_D) of the simulated ion-implanted VMOS device with and without a body contact during source on top mode of operation at pillar thicknesses of a) 200 nm, b) 60 nm and c) 10 nm.

For the intermediate pillar thickness in fig. 2(b), the VMOS device without a body contact shows similar characteristics to the equivalent device in fig. 2(a), although the breakdown kink is sharper and the values of drain current at a given drain voltage are slightly higher. In contrast, the body contacted device is considerably different than the equivalent device in fig. 2(a). In particular, the device shows a sharp breakdown kink at a drain bias around 4.45V, higher values of drain current and the presence of a hump at a drain voltage of around 1.2 V. When comparing characteristics of the devices with and without a body contact, it can be seen that the difference in current between the VMOS device with and without the body contact is reduced and the breakdown kink of the body contacted device occurs at a slightly higher drain voltage.

For the thinnest pillar in fig. 2(c), the characteristics for VMOS devices with and without a body contact are very similar, indicating that the body contact is ineffective at this pillar thickness. The values of drain current are significantly higher than those for the device in fig. 2(b), and the breakdown kink is less severe.

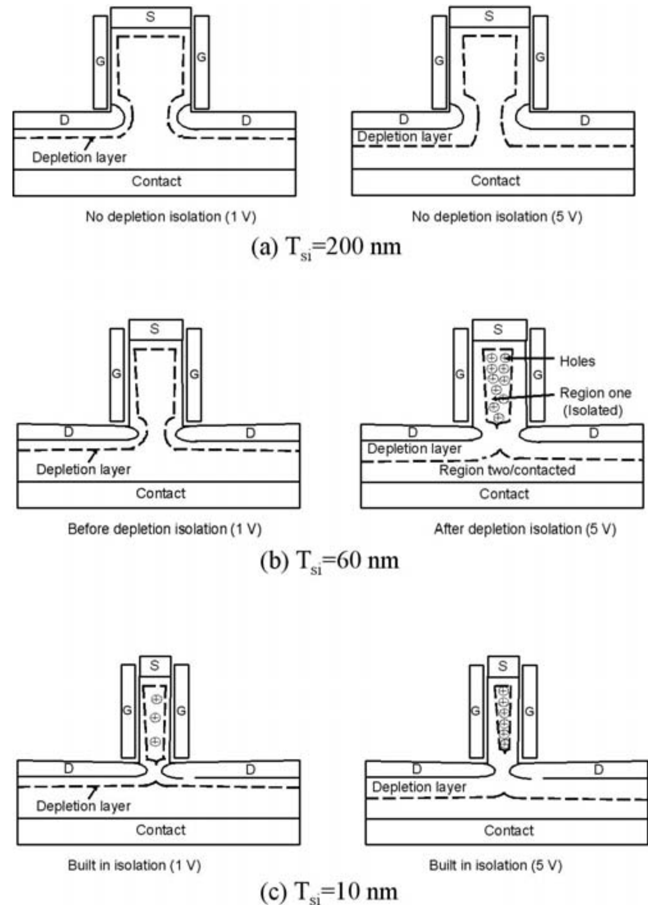

Fig. 3. Schematic cross-sectional view of the body contacted VMOS device before and after depletion isolation. Dashed line represents depletion layer edge. a)200 nm, b) 60 nm and c) 10 nm.

Fig. 3 shows the schematic cross-sectional view of the body contacted VMOS device at low and high drain bias for the pillar thicknesses shown in fig. 2. In the thick pillar VMOS device, shown in fig 3(a) (corresponding to fig 2(a)), no depletion isolation occurs within the range of drain biases shown in fig. 2. Therefore, no body charging occurs and the output characteristic of the body contacted VMOS device does not exhibit any breakdown kink and charging hump. Fig. 3(b) shows the VMOS device with intermediate pillar thickness (corresponding to fig. 2(b)), where the drain bias dependent depletion isolation is clearly evident and hence, the output characteristics of the body contacted VMOS device exhibited a breakdown kink. The charging hump found at 1.2 V reflects the body charging after depletion isolation. In the body contacted VMOS device, charging starts after depletion isolation (charging lag). Therefore, the total body charging is lower than for the device without a body contact and the device

exhibits slightly better breakdown behaviour at this pillar thickness even after depletion isolation. In the very thin pillar case of fig. 3(c) (corresponding to fig. 2(c)) the depletion region isolates the pillar even at low drain bias. Therefore, the output characteristics of the VMOS devices with and without body contact are found to be similar and no charging hump is visible (fig. 2(c)). A moderate breakdown kink is also found at this pillar thickness, which has already been explained by Fossum et al. for fully depleted SOI MOSFET [5].

Fig. 4 shows the normalized breakdown current of VMOS transistors with and without body contact at a drain bias of 5V (breakdown regime) as a function of pillar thickness. The normalized breakdown current is calculated using the equation, *Normalized breakdown current (%)* = $(I_{D\ with\ II}-I_{D\ without\ II})/I_{D\ without\ II} \times 100$. Three different regimes of VMOS device operation can be identified. In the thick pillar region, the pillar is not isolated and no kink is evident in VMOS devices with a body contact. In the depletion isolation region, though a depletion isolation associated kink is observed, the normalized breakdown current is always lower than in the VMOS device without a body contact. In the thin pillar region, VMOS devices with and without body contact show the same kink characteristics, exemplifying the ineffectiveness of the body contact.

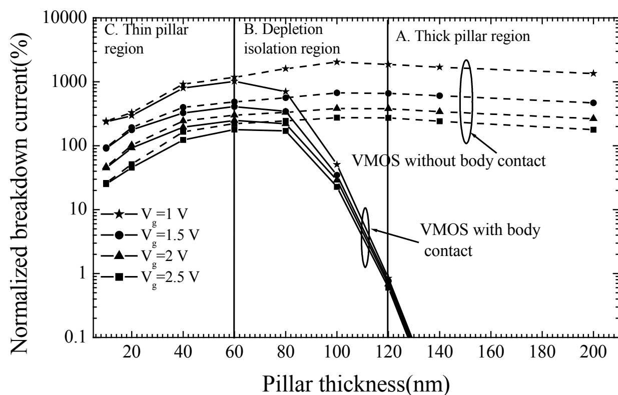

Fig. 4. Comparison of the normalized breakdown current of VMOS devices with and without body contact as a function of pillar thickness for several values of gate voltages.

The effect of substrate conduction on the VMOS device at various pillar thickness is evident from the results in fig. 2 and fig. 4. A gradual reduction of the difference in current between the VMOS devices with and without a body contact is observed with reducing pillar thickness together with an associated improvement of the breakdown voltage (fig. 2) and a reduction of the normalized breakdown current (fig. 4). This is due to the combined action of earlier depletion isolation and the reduction of the initial source-body potential barrier (ϕ_{SB}), with the scaling of the pillar thickness [6]. Earlier depletion isolation reduces the difference in body charging between the VMOS device with and without a body contact, and a lower ϕ_{SB} means a lower amount of free holes available for body charging [6]. Therefore, the difference in the normalized breakdown current between the device with and without a body contact is gradually reduced with the scaling of the pillar thickness.

To further clarify the point, we have simulated the decrease in ϕ_{SB} ($\Delta\phi_{SB}$) and the relative increase in the recombination rate (*ΔRecombination rate*$_{relative}$) due to $\Delta\phi_{SB}$, when the body contact is not provided. $\Delta\phi_{SB}$ and *ΔRecombination rate*$_{relative}$ were determined at the source junction in the middle of the pillar. These results are presented in table I for different pillar thickness. The *ΔRecombination rate*$_{relative}$ was calculated using the equation, *ΔRecombination rate*$_{relative}$ = (*Recombination rate* $_{without\ body\ contact}$-*Recombination rate* $_{with\ body\ contact}$)/ *Recombination rate* $_{with\ body\ contact.}$ In the thick pillar devices (120 to 200 nm) a drastic reduction of ϕ_{SB} (high *ΔRecombination rate*$_{relative}$) is found when the body contact is not provided, supporting the conclusion that the body is not isolated at these pillar thickness. However, $\Delta\phi_{SB}$ (*ΔRecombination rate*$_{relative}$) is found to decrease with decreasing pillar thickness, clearly indicating the gradual ineffectiveness of the body contact.

Table I

$\Delta\phi_{SB}$ and *ΔRecombination rate*$_{relative}$ at V_g=1.5V and V_d=5V

Pillar thickness (nm)	$\Delta\phi_{SB}$ (eV)	*ΔRecombination rate*$_{relative}$(/scm^3)
200	0.96151	1.32E+11
140	0.954	5.40E+10
120	0.9383	1.06E+10
100	0.31278	56400
80	0.01492	0.568
60	0.009	0.307
20	0.00525	0.104
10	0.0045	0.0349

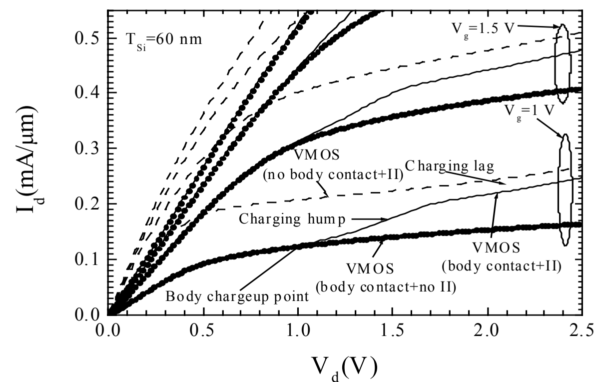

Fig. 5 Comparison of the output characteristics of fig. 2(b) with the simulation result of the same device without impact ionization and the body contact.

Fig. 5 compares the low field output characteristics of the device presented in fig. 2(b) with the output characteristics of the same device with a body contact but without impact ionization. The output curve of the latter VMOS device represents the situation without any body charging. The identical characteristics for the

body contacted devices with and without impact ionization at low drain biases (≤ 1V) clearly indicates that the body is not isolated at these voltages. For drain voltages above 1V, a hump in the output characteristics of the body contacted devices can be seen, indicating the drain bias for body charging (V_{db}) by free holes present in the body. The difference in current between the devices with and without a body contact for drain biases above 1V indicates that floating body effects are less severe in the body contacted devices even after depletion isolation.

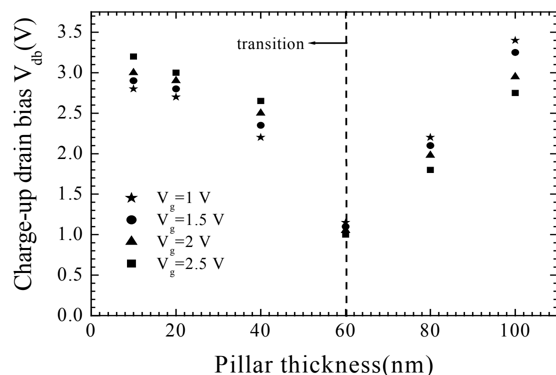

Fig. 6 Charge-up drain bias (V_{db}) as a function of pillar thickness and for several values of gate voltage.

Fig. 6 shows the simulated values of charge-up drain bias (V_{db}) as a function of pillar thickness for several values of gate voltage. A transition is observed in the dependence of V_{db} at a pillar thickness of 60 nm. For pillar thickness ≥ 60 nm, V_{db} decreases with reducing pillar thickness and also decreases with increasing V_g at a given pillar thickness. But for pillar thickness <60 nm, the opposite trends are observed. This is due to the competing mechanisms of earlier depletion isolation and increased recombination due to the reduced source-body potential barrier (ϕ_{SB}) with the scaling of the pillar thickness [6]. In thicker pillar VMOS devices the initial ϕ_{SB} is higher and therefore, the reduced ϕ_{SB} and the associated increase in recombination, induced by the reducing pillar thickness is small. Therefore, for pillar thickness ≥ 60 nm, earlier depletion isolation due to the reduction of the pillar thickness dominates which gives a decrease in V_{db} with pillar thickness scaling. But for pillar thickness < 60 nm, the initial ϕ_{SB} is lower and therefore, the reduction of ϕ_{SB} with decreasing pillar thickness causes a significant increase in recombination. As a result, the reduction in ϕ_{SB} and the associated higher recombination at the source dominates over earlier depletion isolation. This causes V_{db} to increase with decreasing pillar thickness.

The same mechanism also causes the transition in the dependence of V_{db} on V_g at a pillar thickness of 60 nm. For pillar thickness ≥ 60 nm, the earlier depletion isolation due to an increased depletion width resulting from an increased V_g dominates and V_{db} decreases with increasing V_g. In contrast for pillar thickness < 60 nm, recombination dominates and V_{db} increases with increasing V_g.

A transition in the dependence of the normalized breakdown current on pillar thickness is also seen in fig. 4 at a pillar thickness of 60 nm. For pillar thickness ≥ 60 nm, the normalized breakdown current of the body contacted device increases with decreasing pillar thickness due to the earlier onset of depletion isolation. For pillar thickness < 60 nm, the normalized breakdown current decreases with decreasing pillar thickness due to increasing recombination at the source. This behaviour for pillar thickness < 60 nm represents FD regime of operation and corresponds to the film thickness scaling effect of planar SOI MOSFETs [5-7]. In contrast, for pillar thickness ≥ 60 nm, the behavior is due to drain/gate bias dependent depletion isolation, where the drain depletion region merges at the bottom of the pillar.

IV. CONCLUSION

We have studied the effect of the transition from partially depleted to fully depleted operation on the depletion isolation effect in vertical MOSFETs. The impact of the body contact during this transition has been investigated and the body contact is found to be completely effective for pillar thickness > 120 nm and ineffective for pillar thickness < 60 nm. For pillar thicknesses of 60-120 nm, even though the existence of depletion isolation is identified, the body contact is found to be partially effective giving a reduced normalized breakdown current and improved breakdown voltage. With the scaling of the pillar thickness the effectiveness of the body contact is seen to gradually reduce and the impact of substrate conduction on the breakdown voltage and kink behavior is also found to gradually reduce.

ACKNOWLWDGEMENTS

The authors would like to acknowledge the support of the Commonwealth High Commission and European Union (SINANO).

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