The structural and electrical properties of thermally grown TiO$_2$ thin films

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Abstract
We studied the structural and electrical properties of TiO$_2$ thin films grown by thermal oxidation of e-beam evaporated Ti layers on Si substrates. Time of flight secondary ion mass spectroscopy (TOF-SIMS) was used to analyse the interfacial and chemical composition of the TiO$_2$ thin films. Metal oxide semiconductor (MOS) capacitors with Pt or Al as the top electrode were fabricated to analyse electrical properties of the TiO$_2$ thin films. We show that the reactivity of the Al top contact affects electrical properties of the oxide layers. The current transport mechanism in the TiO$_2$ thin films is shown to be Poole–Frenkel (P–F) emission at room temperature. At 84 K, Fowler–Nordheim (F–N) tunnelling and trap-assisted tunnelling are observed. By comparing the electrical characteristics of thermally grown TiO$_2$ thin films with the properties of those grown by other techniques reported in the literature, we suggest that, irrespective of the deposition technique, annealing of as-deposited TiO$_2$ in O$_2$ is a similar process to thermal oxidation of Ti thin films.

1. Introduction

Titanium dioxide (TiO$_2$) is a popular material with many applications in electronics and optoelectronics due to its high permittivity and refractive index [1, 2]. It has been investigated for static random access memory (SRAM) applications [3, 4], and more recently as the body oxide of tunnel transistors [5–7]. Understanding the structural and electrical properties of the TiO$_2$ thin films is critical for the successful implementation of this material. Various techniques are used to grow TiO$_2$, e.g. plasma oxidation [8], plasma-enhanced chemical vapour deposition (PECVD) [9], direct electron-beam evaporation [10] and metal organic chemical vapour deposition (MOCVD) [11]. The metal oxide semiconductor (MOS) capacitor structure is of fundamental importance for device application of TiO$_2$ thin films grown on Si substrates.

However, electrical properties of the oxide layer are affected by the growth technique due to reactions at the oxide/Si substrate interface and those at the metal/TiO$_2$ interface are influenced by the choice of top electrode metal [2]. As-deposited TiO$_2$ layers produced by plasma oxidation, PECVD, direct electron-beam evaporation and MOCVD normally exhibit high leakage currents, and a post-deposition anneal at high temperature (above 500 °C) in oxygen or nitrogen ambient is required to reduce the leakage current. The improvement in the oxide properties grown at higher temperatures are often counter-balanced by an increased thermal budget and the growth of an SiO$_2$ layer at the TiO$_2$/Si interface.

Thermal oxidation of Ti thin films is a simple method to grow a uniform oxide layer in oxygen ambient, and produces minimal surface roughness. In a previous work [7], we fabricated TiO$_2$ thin films by thermal oxidation of e-beam evaporated Ti thin film and showed that thermal oxidation of Ti thin film at 550 °C gave minimum leakage current. One of the issues related to thermal oxidation is the interfacial oxide and the diffusion of Ti and O atoms into the Si substrate. In the present work we used time of flight secondary ion mass spectroscopy (TOF-SIMS) to analyse the composition and the depth profile of the thermally grown oxide at 550 °C on Si substrates. We fabricated MOS capacitors to study the electrical properties of the TiO$_2$ thin films. We used both Pt and Al top contacts to investigate the effects of the top electrode on the electrical properties and discuss the current transport mechanisms in the TiO$_2$ thin films. We compare leakage currents in these layers with as-deposited and annealed oxides reported in the literature, and discuss the effects of annealing on the as-deposited oxide layers.

2. Experimental details

Titanium (Ti) thin films of thicknesses of 7 and 10 nm were deposited on RCA-cleaned and HF-treated standard 4 inch diameter, low-resistivity (0.01–0.02 Ω cm) n-type and p-type Si substrates by vacuum e-beam evaporation of 99.9999% of Ti metal without any substrate heating. The evaporation pressure was 2.25×10^{-6} Torr, and the evaporation rate of Ti was 0.3 nm s^{-1}. The oxide was subsequently formed by thermal oxidation at 550 °C for 30 min. The oxygen flow rate was 5000 sccm. MOS capacitors were fabricated to characterize the TiO$_2$ thin films. 300 nm Pt or 1000 nm Al top contacts were formed by vacuum evaporation using shadow masks. The back contacts consisted of a 1000 nm thick Al layer, which was deposited by vacuum evaporation as well. High doping in Si ensured that the back contacts were Ohmic.

TOF-SIMS measurements were performed with an ION-TOF TOF.SIMS 5 instrument. For erosion a 500 eV Cs$^+$ beam with a target current of 52 nA was applied to an area of $300 \times 300\ \mu\text{m}^2$. A 25 keV Bi$_3^+$ beam, with a target current of 0.33 pA, was used for analysis. The analysed area was approximately $100 \times 100\ \mu\text{m}^2$. The polarity of the secondary ions was positive in order to follow MCs$^+$ cluster ions. X-ray diffraction (XRD) was performed with a Siemens D5000 x-ray diffractometer. Cross-sectional scanning electron microscopy (SEM) was done using a Hitachi S-4800 microscope to visualize the oxide layers grown. Current–voltage (I–V) characteristics were obtained at room temperature and low temperatures using the HP4155A parametric analyser. The bias was applied to the back contact (Si substrate) while the top contact was kept at the ground potential. Positive and negative bias sweeps were started from zero. Low-temperature measurements were performed by mounting the samples on a liquid nitrogen cryostat, controlled by a Biorad DL4960 temperature controller. Capacitance–voltage (C–V) characterization was done at room temperature at 1 MHz using a HP4280A C-meter. The bias was either ramped from inversion or ramped from zero without any noticeable difference. The area of the top contact pads used in most of the measurements was $270 \times 271\ \mu\text{m}^2$.
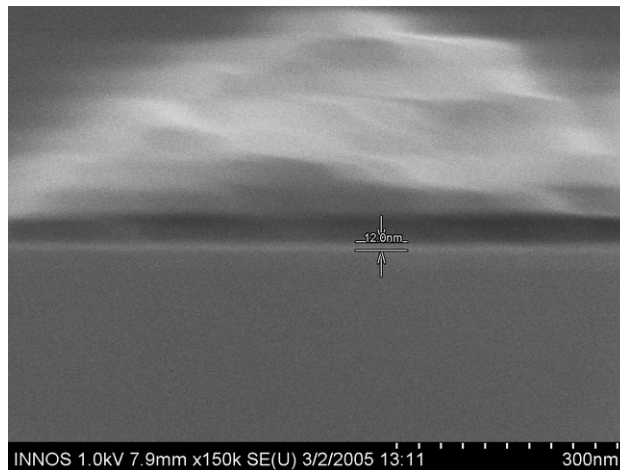
Figure 1. Cross-sectional field emission of SEM micrograph of the oxide grown from a 7 nm Ti layer. The oxide layer appears as a bright band in the diagram.

3. Results and discussion

3.1. Structural analysis

Figure 1 shows the cross-sectional SEM picture of the oxide layer grown from a 7 nm Ti film. It is observed that the thickness of the oxide layer is about 12 nm, which agrees well with the expected thickness-expansion factor of 1.8 when Ti is fully oxidized to TiO$_2$. X-ray diffraction shows that thicker thermally oxidized Ti layers grown at 550 °C are amorphous, which most likely applies to our 12 nm films as well. This is in agreement with the literature, as thermally oxidized Ti will only be transformed to rutile phase at longer oxidation time or at higher oxidation temperatures [12].

Figure 2 shows the SIMS profile of a sample grown from a 7 nm thick Ti film. It is observed that the TiO$_2$ signal decays slowly from the surface and falls sharply after 10 nm and is only detected for depths <12 nm. This value provides a good estimate for the oxide thickness and agrees with the nominal thickness of TiO$_2$ and the SEM picture. The Ti signal from the oxide region exhibits a long tail that extends into the Si substrate. This could be due to diffusion of Ti atoms into the Si as diffusivity of Ti in Si is $1.45 \times 10^{-2} \exp(-1.79\ eV/kT)$ cm^2 s^{-1}, which is about one order of magnitude higher than that of O in Si [13]. Furthermore, an increase of the CsTi ion formation efficiency in the Si compared to the TiO$_2$ matrix cannot be excluded [14]. Notably, SiO$_2$ and titanium silicate (TiSiO$_3$) signals are also detected in this region and both peak at a depth of approximately 10 nm. This indicates that the interfacial layer has formed by reactions among Ti, Si and O atoms. This is likely in the light of the reports that titanium silicide formed at temperatures above 400 °C [15, 16]. In our case, the presence of oxygen at high temperature leads to the formation of SiO$_2$ and titanium silicate at the interface. The peak of the SiO$_2$ signal at the surface is most likely due to a polysiloxane (PDMS) contamination of the sample surface from the plastic sample container. In summary, the SIMS depth profile confirms that the total oxide thickness is about 12 nm and there is an interfacial layer of 4 nm titanium silicate.

3.2. Electrical analysis

3.2.1. Current–voltage (I–V) and capacitance–voltage (C–V) characterization.
The I–V characteristics of the TiO$_2$ MOS capacitors are shown in figure 3. It is noted that the leakage
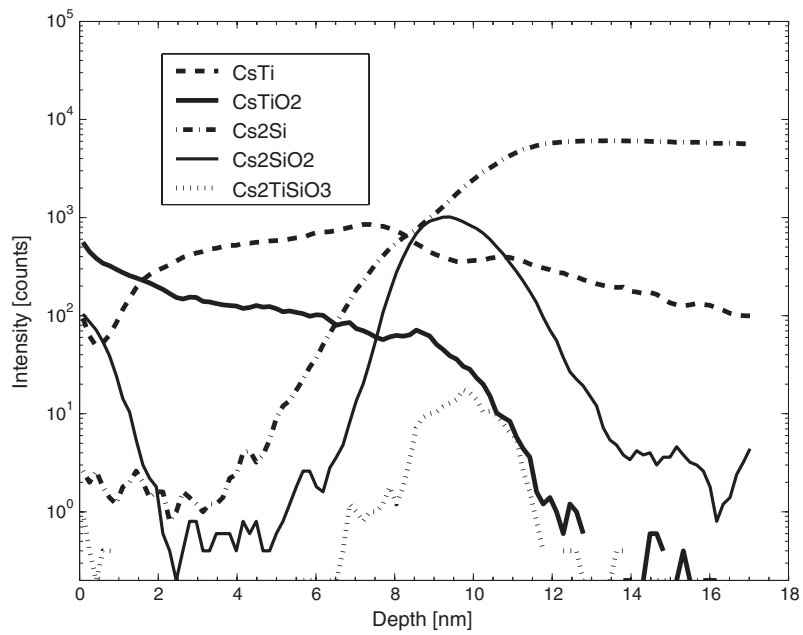
Figure 2. TOF-SIMS data of the oxide grown by thermal oxidation of a 7 nm Ti layer at 550 °C.
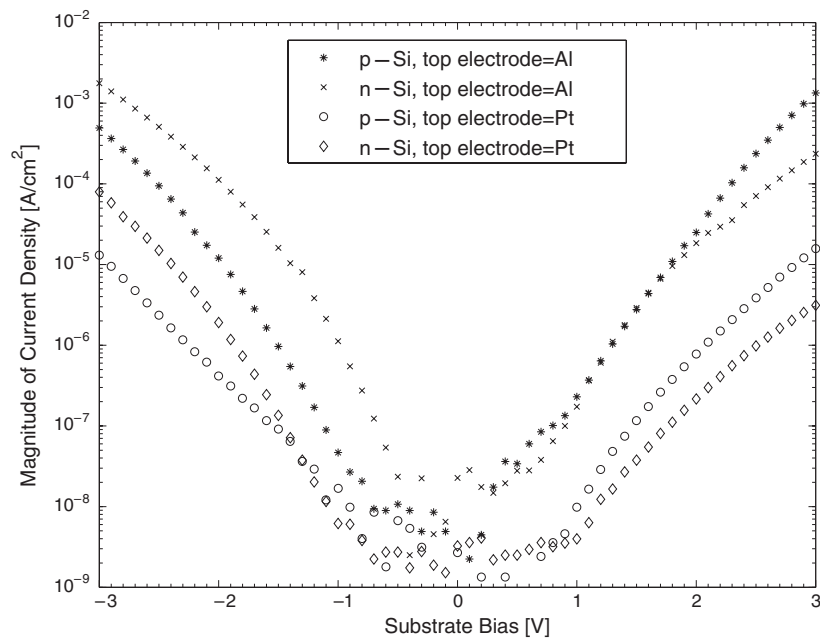
Figure 3. The room temperature current voltage characteristics of the 18 nm TiO$_2$ thin films. The capacitors with Al top contact give higher leakage current than those with Pt top contact.

current is higher in the capacitors with Al top electrode, regardless of the type of substrate. It has been shown that the choice of the top electrode material can affect I–V and C–V
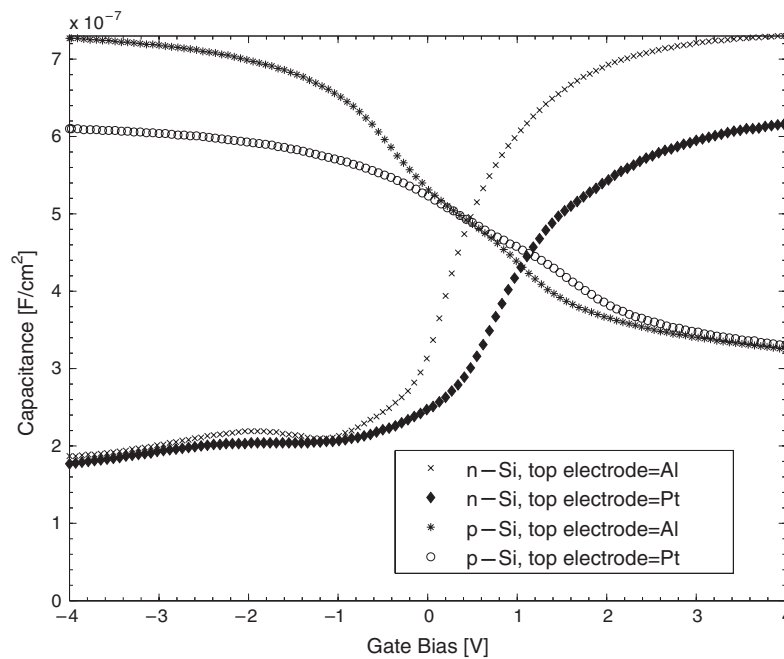
Figure 4. The capacitance–voltage characteristics of the 18 nm TiO$_2$ thin films at room temperature. The capacitors with Al top contact show higher accumulation capacitance than those with Pt top contact.

characteristics due to reactivity of the metal with the underlying oxide at the metal/oxide interface [17]. Al is more reactive than Ti as the heat of formation of alumina is higher than titania [18]. Therefore, Al atoms tend to react with oxygen of the underlying TiO$_2$ and create an interfacial layer of oxygen-deficient titanium oxide, which has a lower resistivity and allows more leakage current. This is not the case for Pt.

The results of $C–V$ measurements are shown in figure 4. Two distinct characteristics are observed. Firstly, the capacitors with Al top electrode have higher accumulation capacitance than the capacitors with Pt top electrode. If the oxide thickness is the same, the accumulation capacitance should be similar regardless of the top electrode. However, as mentioned before, the Al top electrode may react with TiO$_2$ and reduce the effective oxide thickness. As the capacitance is inversely proportional to the oxide thickness, the accumulation capacitance of the capacitors with Al top electrode will show higher value than those with the Pt top electrode. Secondly, the minimum capacitances C_{min} of the capacitors on n-Si substrate are lower than those on the p-Si. This is due to the fact that for the similar resistivity, the p-Si substrate has a higher doping concentration than the n-Si substrate [19] and the capacitance is proportional to the square root of the doping density.

Table 1 shows the accumulation capacitance, the oxide thickness and the dielectric constant of the capacitors. As there is minimal reaction between the Pt top electrode and the oxide, the dielectric constant is calculated from the accumulation capacitance of the capacitors with Pt top electrode assuming the nominal oxide thickness of 18 nm, as confirmed by SEM [7]. The calculated dielectric constant is then used to calculate the effective thickness of the oxide in the capacitors with Al top electrode, by assuming that the dielectric constant of the thermally grown oxide is similar. This is likely as all the oxides are grown simultaneously under the

Table 1. Summary of the capacitance–voltage analysis of the samples with TiO_2 grown from 10 nm of Ti thin film at 550 °C. The ϵ_r of capacitors with Pt top contact was calculated using the nominal thickness of the TiO_2 thin films (18 nm TiO_2 for 10 nm of Ti). The ϵ_r of capacitors with Al top contact was assumed to have the same value as capacitors with Pt top contact. The oxide thickness of the capacitors with Al top contact was determined using the ϵ_r.

Sample	C_{ox} (F m^{-2})	d_{ox} (nm)	ϵ_r	Q_i (cm^{-2})
p-Si, top contact = Pt	6.16×10^{-3}	18.0	12.5	6.19×10^{12}
p-Si, top contact = Al	7.30×10^{-3}	15.2	12.5	2.23×10^{12}
n-Si, top contact = Pt	6.10×10^{-3}	18.0	12.4	-1.03×10^{12}
n-Si, top contact = Al	7.27×10^{-3}	15.1	12.4	-4.58×10^{12}

same conditions. This analysis suggests that the top 3 nm of the TiO_2 are depleted in oxygen due to the Al top contact.

By comparing the C–V characteristics of the capacitors with the ideal simulated C–V curves, the flat-band voltage V_{FB} of the capacitors can be estimated. The oxide charge density of the capacitors Q_i can be calculated using the following formula [19]:

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_{ox}} \tag{1}$$

where Φ_{ms} is the work function potential difference between the metal and the semiconductor. The values of the charge density in the capacitors are summarized in table 1 and are all above 10^{12} cm^{-3}. These are similar to the values reported in the literature [9, 10]. It is noted that the oxide charge is negative for n-Si and positive for p-Si. This indicates that Fermi-level pinning happens at the interface of the TiO_2 and Si, possibly due to the amphoteric nature of the metal–Si bonds [20].

3.2.2. Current transport mechanism. We chose a Pt/TiO_2/p-Si capacitor to analyse the current transport mechanisms in our thermally grown TiO_2 thin films in more detail. Due to the large work function of the Pt, the current is expected to consist predominantly of electrons and holes from the Si substrate for negative and positive substrate bias, respectively. Figure 5 compares the I–V characteristics of a Pt/TiO_2/p-Si capacitor at room temperature and at 84 K. It is shown that the current flowing through the device is strongly temperature dependent. As the thermally grown TiO_2 has high interface charge density as shown by C–V analysis, Poole–Frenkel (P–F) emission due to the traps or defects in the oxide is possible. The J–V relationship of the P–F emission can be expressed as

$$J = A_{PF} V \exp\left[-\frac{q}{kT} \left(\Phi_T - \sqrt{\frac{qV}{\pi \epsilon_{dyn} \epsilon_0 d_{ox}}} \right) \right] \tag{2}$$

where A_{PF} is a constant, k is the Boltzmann constant, q is the electronic charge, T is the temperature, Φ_T is the barrier height for the traps/defects in the oxide, ϵ_{dyn} is the dynamic dielectric constant of the oxide, ϵ_0 is the permittivity of free space, d_{ox} is the oxide thickness and V is the applied bias. ϵ_{dyn} can be determined from the slope (B_{PF}) of a linear $\ln J/V$ versus $\sqrt{V}$:

$$B_{PF} = \frac{q}{kT} \sqrt{\frac{q}{\pi \epsilon_{dyn} \epsilon_0 d_{ox}}}. \tag{3}$$

The $\ln J/V$ versus $\sqrt{V}$ P–F plot is shown in figure 6. The slope of the straight line results in an ϵ_{dyn} of 7.89. As pointed out by O'Dwyer [21], only a self-consistent dynamic dielectric constant
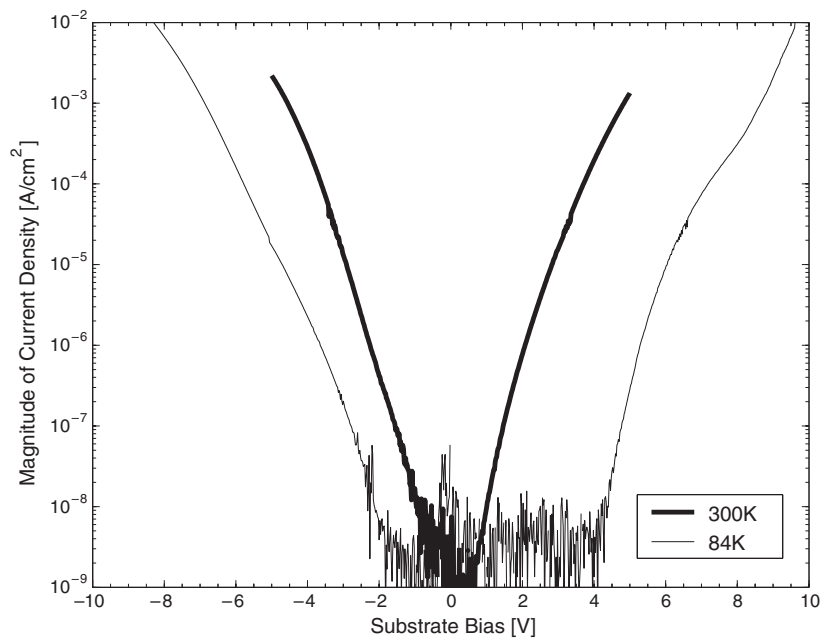
Figure 5. The comparison of the $I-V$ characteristics of the 18 nm TiO$_2$ thin films at room temperature and at 84 K.
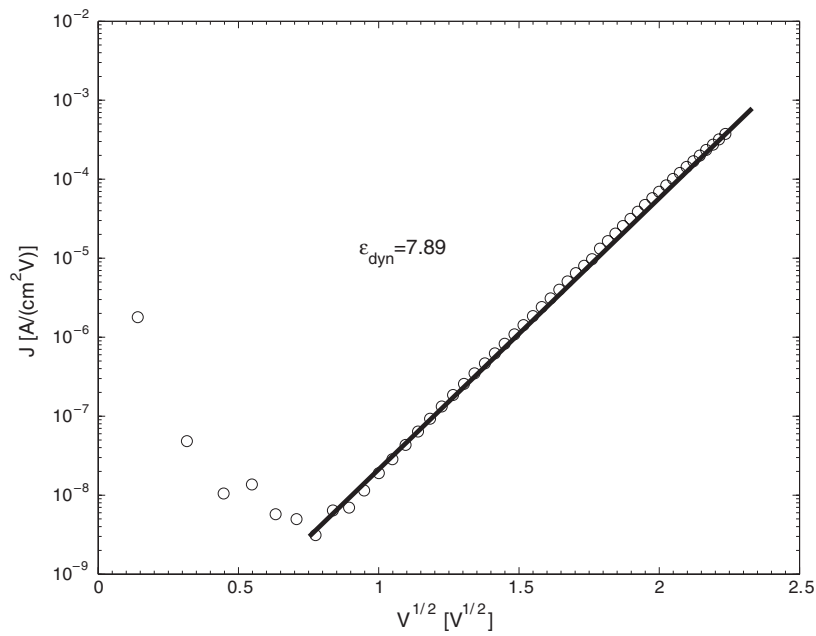
Figure 6. The Poole–Frenkel plot of a 18 nm TiO$_2$ thin film at room temperature. The straight line is a fit to (2).

can ensure that the current conduction is due to P–F emission, i.e. $\epsilon_{opt} < \epsilon_{dyn} < \epsilon_{static}$ [22]. The optical dielectric constant ϵ_{opt} can be determined from the refractive index of TiO$_2$, η.

$\epsilon_{opt} = \eta^2 = 2.75^2 = 7.56$. The static dielectric constant, ϵ_{static}, is obtained from the C–V measurement, which is 12.5. The ϵ_{dyn} determined is within the expected range. Thus, P–F emission is the dominant current transport mechanism at room temperature.

At 84 K the thermal activation mechanisms, such as P–F emission, will be suppressed. Therefore, tunnelling processes, which are temperature independent, could be the dominant current transport mechanism at low temperature. At high bias, the Fowler–Nordheim (FN) tunnelling of electrons (holes) through the triangular barrier to the conduction band (valence band) of oxide will occur. The F–N tunnelling current can be expressed as

$$J = A_{FN} V^2 \exp\left(-\frac{B_{FN}}{V}\right) \tag{4}$$

where A_{FN} and B_{FN} are constants, and B_{FN} can be expressed as

$$B_{FN} = \frac{8\pi \sqrt{2m^* m_0}(q\Phi_B)^{3/2} d_{ox}}{3qh} \tag{5}$$

m^* is the tunnelling effective mass of the charge carrier in the tunnel barrier, m_0 is the free electron rest mass, h is the Planck's constant and Φ_B is the barrier height of oxide. If the dominant current transport mechanism is F–N tunnelling, then the graph of $\ln(J/V^2)$ versus $1/V$ will show a linear line of slope $-B_{FN}$.

When there are traps or defects in the oxide, trap-assisted tunnelling could occur through the traps [23, 24]. It is a two-step tunnelling process: first, the electron from the Si substrate will tunnel into the traps, then, it will tunnel to the conduction band of the oxide. The J–V relationship for trap-assisted tunnelling is quite similar to F–N tunnelling except for the V^2 prefactor, and is given by

$$J = A_{TAT} \exp\left(-\frac{B_{TAT}}{V}\right) \tag{6}$$

where A_{TAT} is a constant. The trap activation energy, $q\Phi_T$, can be determined from the slope (B_{TAT}) of the linear $\ln J$ versus $1/V$, where

$$B_{TAT} = \frac{8\pi \sqrt{2m^* m_0}(q\Phi_T)^{3/2} d_{ox}}{3qh}. \tag{7}$$

The F–N plot of the Pt/TiO$_2$/p-Si capacitor at negative substrate bias is shown in figure 7. There is a linearity of about three orders of magnitude at high bias. This is due to the F–N tunnelling of electrons in the inversion layer of the p-Si substrate. The TiO$_2$/Si potential barrier $\Phi_{TiO_2/Si}$ at the conduction band is determined from the slope of the straight line and (5), which gives $\Phi_{TiO_2/Si} = 0.73$ V. Figure 7 also shows that in the F–N plot of the Al/TiO$_2$/p-Si capacitor the evidence of F–N tunnelling is less convincing. However, it has similar characteristics to that in our previous work [7], although with slightly lower current density. This indicates that the thermal oxidation process is repeatable. The difference in the current density could be due to the different O$_2$ flow rate in the experiments.

Figure 8 shows the F–N plot of a Pt/TiO$_2$/p-Si capacitor at positive substrate bias. It is noted that there are four significant regimes shown in the F–N plot. At low bias (regime A), hopping conduction is the dominant current transport mechanism, as shown by the J versus V hopping plot in figure 9. The current increases sharply for a bias greater than 4.5 V, due to trap-assisted tunnelling (regime B). This is followed by a quasi-saturation stage (regime C) for biases between 6.5 and 8 V. A similar phenomenon was observed by Wong *et al* [25] in thermally nitrided SiO$_2$. For bias above 8 V, F–N tunnelling can occur (regime D).
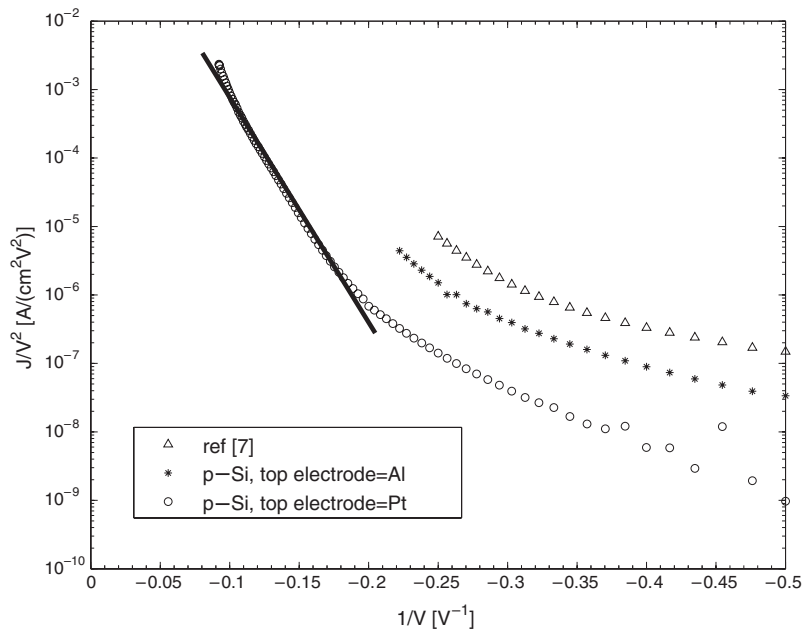
Figure 7. The Fowler–Nordheim plot of the 18 nm TiO$_2$ thin films at 84 K, at negative substrate bias. The straight line is a fit to (4).
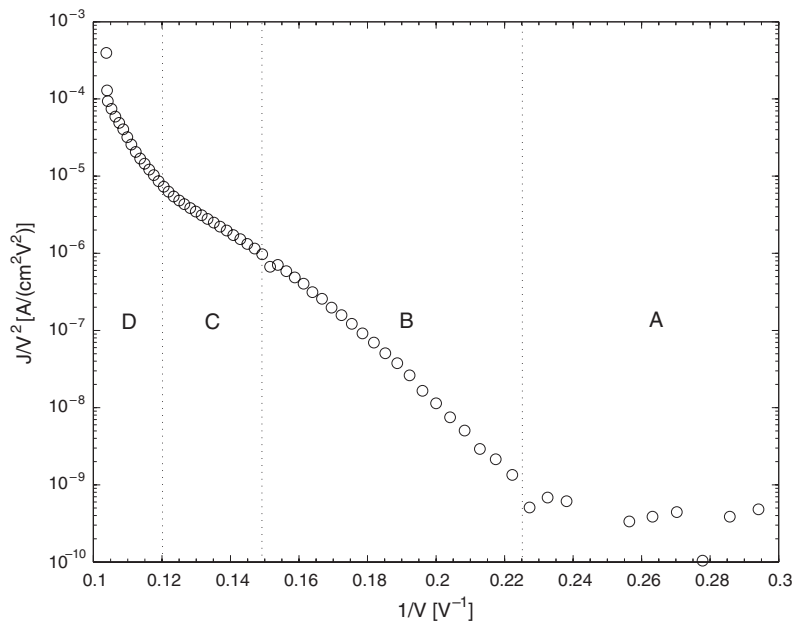

Figure 8. The Fowler–Nordheim plot of a 18 nm TiO$_2$ thin film at 84 K and positive substrate bias. The four different regimes indicate four different mechanisms in the oxide.

Figure 10 shows the ln J versus $1/V$ trap-assisted tunnelling plot. It is clear that for biases between 4.5 and 6 V, the current transport mechanism is due to trap-assisted tunnelling
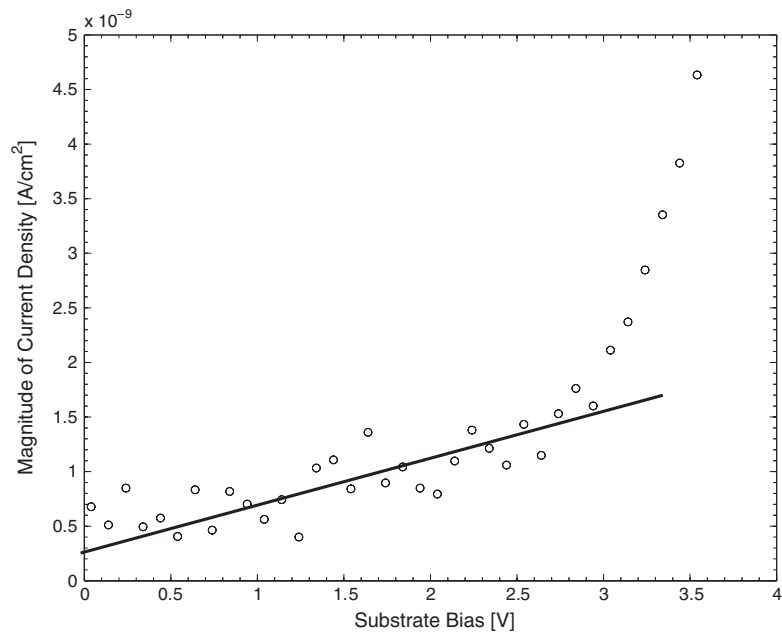
Figure 9. The hopping conduction plot of an 18 nm TiO$_2$ thin film at 84 K and at low positive substrate bias. The straight line is a guide for the eyes.
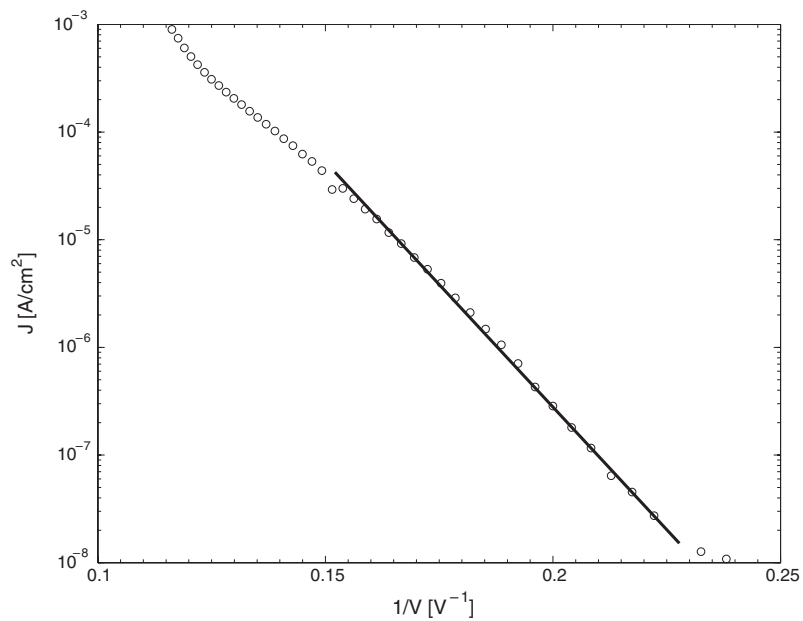
Figure 10. The trap-assisted tunnelling plot of the 18 nm TiO$_2$ thin film (Pt top electrode, p-Si substrate) at 84 K and positive substrate bias. The straight line is a fit to (6).

of holes. Using (7), the trap activation energy is found to be 0.90 eV, which appears to be the *D* traps observed earlier by Klusek *et al* [26] at 0.6 eV below the Fermi level in heavily
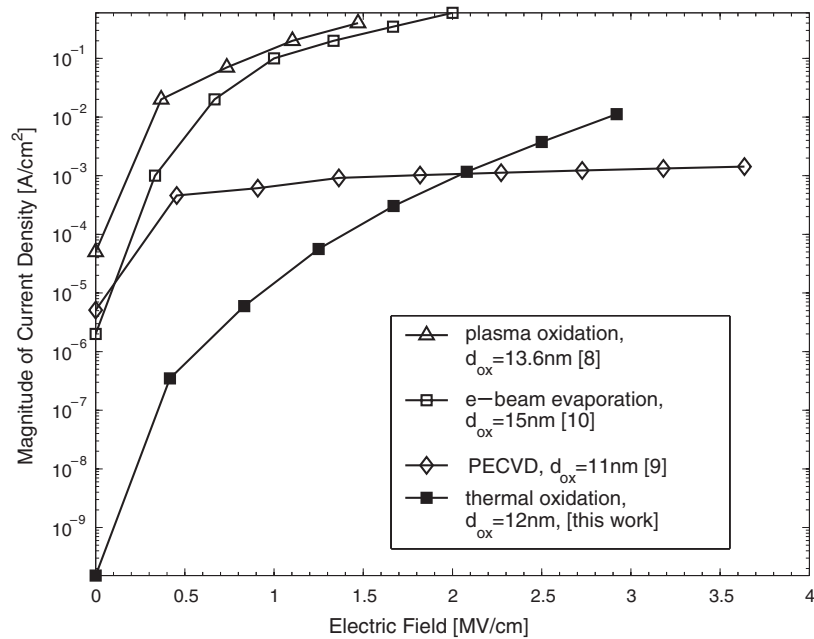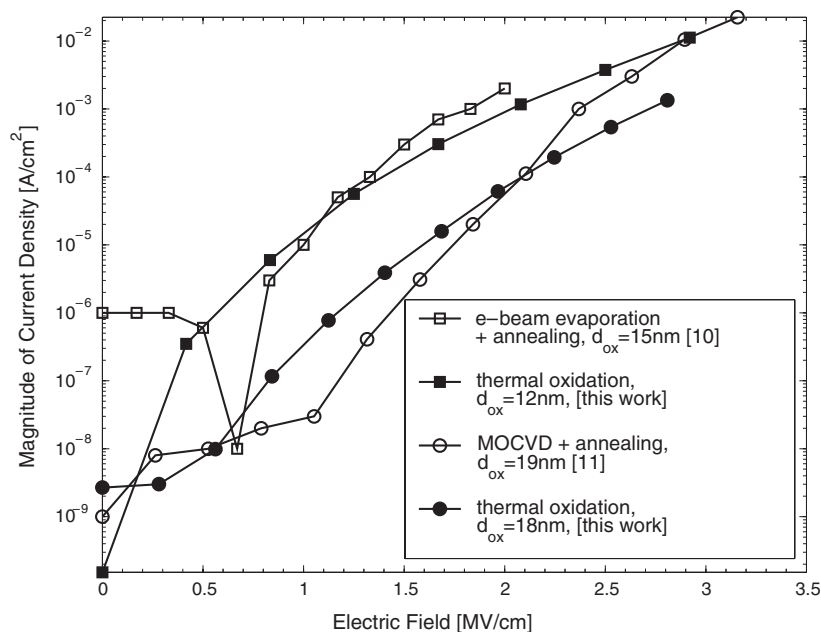
Figure 11. The comparison of the $I-V$ characteristics of 12 nm TiO$_2$ grown by thermal oxidation with plasma oxidation [8], e-beam evaporation [10] and PECVD [9]. The thermally grown TiO$_2$ was fabricated by oxidizing 7 nm of Ti thin film at 550 °C.

reduced TiO$_2$. The filling of this trap level by holes in our samples led to the saturation of current in regime C in figure 8. We did not see the better known trap level at 0.7 eV below the conduction band [27, 28] as the substrate here is p type and holes are the majority charge carriers.

3.3. Comparison of fabrication methods

In this section, we compare the electrical characteristics of our thermally grown TiO$_2$ thin films with those of layers grown by other fabrication methods reported in the literature. Figures 11 and 12 show leakage currents flowing through similar MOS capacitors where oxide layers of similar thicknesses were deposited by different techniques. The graphs show $I-V$ characteristics of the capacitors under accumulation conditions only to ensure that the leakage current is not influenced by the depletion region in the silicon substrate. Figure 11 compares the $I-V$ characteristics of our thermally grown TiO$_2$ with those of as-deposited oxide layers grown by other techniques [8–10]. It is observed that the leakage current in the thermally grown TiO$_2$ is about three orders of magnitude lower than that in plasma-oxidized TiO$_2$ [8] and in e-beam deposited TiO$_2$ [10]. At low bias, thermally grown TiO$_2$ also has a lower leakage current than in PECVD-grown TiO$_2$ [9]. As the leakage current in other techniques is unacceptably high, post-deposition treatments are usually performed in oxygen. Leakage currents in capacitors using thermally grown TiO$_2$ with those using annealed oxides grown by other techniques are compared in figure 12. The devices have similar structures and oxide thicknesses. The MOCVD-grown TiO$_2$ was post-annealed at 750 °C in O$_2$ [11] while the e-beam grown TiO$_2$ was annealed at 700 °C in O$_2$ for 60 min [10]. From figure 12, it is clear that leakage currents in our thermally grown TiO$_2$ thin films are very similar to those in the post-growth annealed oxide layers.

Figure 12. The comparison of the I–V characteristics of thermal oxidized TiO_2 with other fabrication methods with post-deposition annealing: MOCVD [11] and e-beam evaporation [10]. The 12 and 18 nm thermally grown TiO_2 were fabricated by oxidizing 7 and 10 nm Ti thin film at 550 °C, respectively.

It is evident that as-deposited titanium oxide layers produced by plasma oxidation [8], PECVD [9], e-beam evaporation [10], MOCVD [11] etc often exhibit high leakage current and post-growth anneals at high temperatures help to reduce this [10, 11]. Interestingly, the annealed oxide layers exhibit I–V characteristics similar to those of thermally grown titanium oxide. Hence we suggest that, irrespective of the deposition technique, annealing of the as-deposited TiO_2 in O_2 is a similar process to thermal oxidation of Ti thin films.

4. Conclusions

We fabricated MOS capacitors with both Pt and Al top electrodes to study the structural and electrical properties of the TiO_2 thin films. The oxide layers are grown by thermal oxidation of e-beam evaporated Ti layers at 550 °C for 30 min. TOF-SIMS depth profiling shows the existence of an interfacial layer of 4 nm titanium silicate in a typical 12 nm thick TiO_2 thin film. The I–V and C–V analysis indicates that the Al top electrode can react with the oxygen in the TiO_2 thin films at the Al/TiO_2 interface, and the top 3 nm of the TiO_2 are depleted in oxygen due to that reason. The current transport mechanism in TiO_2 at room temperature is P–F emission, due to the traps/defects in the oxide. At low temperatures and low bias, the dominant mechanism is hopping conduction. F–N tunnelling due to electrons is observed at low temperature and high bias. The TiO_2/Si barrier at the conduction band is 0.73 eV. Quasi-saturation is observed in the I–V characteristic at low temperature. We believe that this is due to filling of defect-related traps above the valence band with holes during the trap-assisted tunnelling process. The trap activation energy is 0.90 eV, which was observed earlier by another group.

We compared the leakage current density of the thermally grown TiO$_2$ thin films with as-deposited and annealed oxide layers grown by other techniques. Thermally grown TiO$_2$ thin films have lower leakage current densities than those of as-deposited oxides, and exhibit leakage current densities similar to those of annealed oxides. We suggest that deposition of TiO$_2$ followed by annealing is equivalent to direct thermal oxidation of metallic Ti films and produces similar oxide quality in terms of leakage currents.

Acknowledgment

Note added in proof. We dedicate this article to the fond memory of our microfabrication facility in the University of Southampton, which was destroyed by a devastating fire on 30 October 2005. This work was one of the last completed there.

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