A NEW VERTICAL POWER MOSFET WITH EXTREMELY REDUCED ON RESISTANE AND HIGH SWITCHING SPEED BY MULTILAYER STRUCTURE

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Abstract

A vertical power MOSFET's whose n-drift region is stacked by alternate pn structure named as MULTILAYER POWER MOSFET has been proposed for high voltage application with extremely low onresistance. However, the device capacitance increases by a significant amount that has the possibility to reduce the switching speed of the devices. Therefore, a trade off is established to reduce RC time constant by changing the thickness of the stacking. The electrical characteristics of a CONVENTIONAL POWER MOSFET having trench contact for the source and body regions are compared with that of our proposed multilayer structure. The device prooves itself as a high performance MOSFET with high speed and high storage capacity.

1. INTRODUCTION

In recent years, power MOSFET's have been widely applied to a variety of power electronic systems owing to there high speed performance and excellent thermal stability[1]. The channel resistance of these devices, which is determined by the total gate width in the chip, occupies a major part in the total on-resistance. Reducing on-resistance product was mainly limited through the increase in packing density and modifying gate source junctions. Few significant improvements were provided through VDMOSFET[2] and UMOSFET[3] structures. Also RMOSFET by a RIBE technique[4] and advanced self-aligned technologies[5]; TC-UMOSFET's [6], by burying selective CVD tungsten in the trenches for the contacts [7,8] provides low on-resistance. However all the device structures and masking technology was mainly limited to the channel resistance reduction. But in this paper, we proposed further reduction of ON-resistance product of power MOSFET's by providing multilayer structure in the n-drift region. This paper also describes the effect of multilayer structure in input capacitance and a trade off is established for number of stacks of layers so as to limit input capacitance and provide us with high switching speed and in addition high storage capability device.

2.DEVICE STRUCTURE

As example of CONVENTIONAL vertical device, the structure of an n-channel, trench gated, vertical MOSFET

is shown in Figure 1. In vertical devices high breakdown voltage is realized in the wide depletion region in the low



Fig. 1. Structure of n-channel, trench gated conventional vertical MOSFET.

concentration n-drift region of n-drift/p-well junction. In MULTILAYER devices (Figure 2), the n-drift regions of conventional devices are simply replaced by a number of alternately stacked, p and n type, thin semiconductor layers. These multilayer structures act as a pn junction or as a drift region with high performance. Low specific on resistance of MULTILAYER devices is ensured by the number of parallel current paths and on resistance is inversely proportional to the number of parallel layers.



Fig. 2. Multilayer, trench gated, vertical MOSFET.

Simplest multilayer structure shown in the Fig. 3, with dimensions l_x , l_y , l_z , respectively in the *x*, *y*, *z*, directions, consists of a number of alternately stacked, p- and n-type, thin, semiconductor layers with thickness 'd' and volume doping of N_a , and N_d respectively. For ease of

understanding this structure is treated as an ideal multilayer field effect transistor (*FET*) comprising a number of n-type channels and p-type gates.



Fig. 3. Multilayer structure treated as ideal Multiple FET.

3.DEVICE CHARACTERISTICS AND DISCUSSIONS

3.1 Breakdown Voltage

To obtain full depletion of multilayer structures, the depletion region growing from pn junctions must be connected to the neighboring depletion layers before breakdown takes place as shown in figure 3. Assuming step pn junctions at z = 0 and perfect depletion, when the leading edges of the depletion region are at $Z = Z_p$ and $Z = Z_n$ - d, respectively, in p and n layers, or when the depletion region merge, using Poisson's equations, we get,

$$q.N_d.d = 2.e.|E_z|_{\max} = 2.a.e.E_c....(1)$$

Where, α is an optimum coefficient and E_c is the critical electrical field of the semiconductor material. This optimum coefficient has the value between 0 and 1, provides us with the flexibility so that $|E_z|_{max}$ is less than E_c . Using equation (1) and assuming equal doping of N_a and N_d , expression for breakdown voltage can be written as:

$$V_{b} = (1 - a) \cdot E_{c} \cdot L_{v} \cdot \dots \cdot \dots \cdot (2)$$

3.2 On Resistance

On-resistance of vertical power MOSFET is the sum of the channel resistance (R_{ch}) and the resistance of the epitaxial drain buffer region (R_{epi}). R_{ch} is mainly minimized by packing density control which is significant for low voltage application. As we are interested in high voltage power MOSFET, we mainly look after R_{epi} region by multilayering epitaxial drain buffer region along with the processes reported for packing density control. In case of our proposed MULTILAYER vertical device, if y-plane is the principal plane of the chip and current flows in the y-direction, we can simulate it just a parallel connection of multiple FET as shown in Fig 3. Sheet resistance of the device (R_{on} . A_{y}) can be written as:

$$(R_{on}.A_{y}) = \frac{2d}{L_{z}} \cdot \frac{L_{y}}{\mathbf{m}_{n}.q.N_{d}.d.L_{x}} \cdot (L_{x}.L_{z}) \dots \dots (3)$$

Using poisson's relationship(Eq. 1), expression of V_b (Eq. 2), (Eq. 3) and considering an optimum value α of 1/2 we get,

$$R_{oN} A_{y} = 4.d. \frac{V_{b}}{me.E_{c}^{2}}$$
.....(4)

The ideal specific on resistance of conventional vertical MOSFET is given by [10],

$$R_{ON}.A_{v} = \frac{27}{8}.\frac{V_{b}^{2}}{me.E_{c}^{3}}.....(5)$$

If we take ratio of the specific on resistance of MULTILAYER FETs to that of the conventional devices, there is $(1.185 \times d \times E_c)/V_b$ times reduction of sheet resistance of MULTILAYER MOSFET. It seems possible to minimize the thickness of stacked layers, 'd' to around 10nm before quantum effect severely takes place and thickness of stacked layers, L_z and L_x , are severely limited by technology and the order of 100µm. Therefore, in semiconductor multilayer devices, the reduction of the specific 'ON' resistance by 4-5 orders of magnitude from that of CONVENTIONAL devices is possible.

Using relationship between optimal doping concentration N_d , optimal thickness of drift region W_d , the electric field and the mobility respectively with the breakdown voltage [9,10], the ideal specific 'ON' resistance of silicon, majority carrier, vertical MULTILAYER device, as a function of breakdown voltage and stack width can be calculated. Those are, for MULTILAYER device,

$$R_{on}.A_{y} = 1.98 \times 10^{-1}.d^{\frac{5}{4}} V_{b}(\Omega.cm^{2}).....(6)$$

And CONVENTIONAL device,

$$R_{on}.A_{v} = 8.3 \times 10^{-9}.V_{b}^{5/2} (\Omega.cm^{2}).....(7)$$

Typical values of 'ON' resistance versus breakdown voltage with stack with as parameter is plotted along with CONVENTIONAL device as shown in Fig. 4. It has been observed that with the increase of stack layers, the 'ON' resistance decreases significantly. It is also observed that above 200 volt, the MULTILAYER vertical device is

very effective in resistance reduction and at very high voltage resistance reduction ratio is very good.



Fig. 4. Relationship between on-resistance product $(R_{on}A_y)$ and breakdown voltage (V_b) of conventional TC-UMOSFET and MULTILAYER MOSFET at various stacking.

3.3 Input Capacitance

In multilayer device in addition to the normal gate to sourge and parasitic capacitances there are lots of junction capacitance in the drift region. Using relationship between optimum doping concentration N_d and breakdown voltage V_b [9,10], interrelation of junction capacitance, stack width d and breakdown voltage V_b can be expressed as,

$$C_i = 6.36 \times 10^{-10} d^{-1/2} V_b^{-3/5} A....(8)$$

Where C_j is the junction capacitance and A is the area. If device dimension is L_z cube with d as stack width, then L_z/d is the number of stacks and $(L_z/d-1)$ is the number of pn junctions. So gate to drain capacitance without taking into account overlap capacitance is contribution of $(L_z/d-1)$ times junction capacitance. Considering overlap capacitance to the calculated value of C_{gd} for various breakdown voltage region, with stacking width as parameter and taking account of gate to source capacitance, input capacitance can be calculated.

Fig. 5 shows the variation of input capacitance with the variation of breakdown voltage for particular number of stack. The figure shows that the input capacitance increases with the increase of number of stacks. It is also observed that the input capacitance decreases with increased breakdown voltage design and above 1000V input capacitance of CONVENTIONAL TC device starts increasing and becomes higher than some of the MULTILAYER device, hence provides option for using

our proposed device as high speed switches at high voltage region.



Fig. 5. Relationship between input capacitance and breakdown voltage for both TC-UMOS and MULTILAYER TC-UMOS at various stacking.

3.4 Switching Speed

Switching speed of any MOSFET depends upon RC time constant of a device. The relationship between RC time constant and breakdown voltage with the number of layers as parameter is shown in Fig. 6. It is observed that above 300V RC of MULTILAYER vertical device is always less than CONVENTIONAL TC-UMOS device. Three types of behavior are prominent. Below 200V RC constant of MULTILAYER device is always greater than



Fig. 6. The product of input capacitance and onresistance as a function of the breakdown voltage for both TC-UMOS and MULTILAYER TC-UMOS at various stacking.

conventional TC device and RC constant increases with increased number of layers. Between 200 to 300V proper selection of layers are required for providing less RC constant than CONVENTIONAL device. However, above 300V, RC constant of MULTILAYER device is always less than CONVENTIONAL TC device. This is because above 300V, Ron of MULTILAYER device start decreasing than that of the CONVENTIONAL device and above 1000V input capacitance of CONVENTIONAL device also starts to be greater than MULTILAYER device. Between this increased input capacitance of MULTILAYER device is compensated by its decreased ON-resistance product and becomes effective from 200V. It is also observed that at the very high voltage high layering decreases Ron so much that increase of input capacitance is over compensated and RC constant of high layered device is lower than that of the low layered



Fig. 7. Relationship between RC time constant and no of stack layers with breakdown voltage as parameter.

device. Fig 7 shows variation of RC time constant with no of stacks taking breakdown voltage as parameter. From which we can see that, it will be fruitful to apply with stacking greater than 100, where RC constant tends to be almost constant. Also too much high stacking is not feasible due to fabrication complexity and associated quantum effects. So MULTILAYER device is very effective for 300<Vb<10000V (breakdown voltage of Si) and 100<n<1000 for this particular dimensions(drift region of 50 micro-meter cube) considered.

4.CONCLUSION

The relationships between ideal specific 'ON' resistance and breakdown voltage for Si majority carrier multilayer of alternate pn vertical MOSFETs have been theoretically derived and compared with that of the CONVENTIONAL TC-UMOS devices. It is found that the specific 'ON' resistance of majority carrier MULTILAYER VERTICAL MOSFETS can be reduced to less than 1/100 that of the conventional device. Since multilayer structure increases the input capacitance, proper choice of number of alternate pn layers reduces the time constant of the device, which is less than that of the CONVENTIONAL device. It may be applied for switches with fast response, small delay time and at a time high data storage capacity. Number of parallel current paths ensures low specific 'ON' resistance and high current with same applied voltage compared with that of the CONVENTIONAL device and R_{on} can be reduced according to some scaling law as R_{on} reduces with increased stacking per unit area. These devices with high input capacitance provides good storage capacity and can be applied for CCD, storage memory devices, etc. The device is found very effective for high breakdown voltage device. Therefore, finally we can conclude that MULTILAYER VERTICAL devices are indeed high performance device.

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