Briefs

Effects of Neglecting Carrier Tunneling on Electrostatic Potential in Calculating Direct Tunneling Gate Current in Deep Submicron MOSFETs

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***Abstract*—We investigate the validity of the assumption of neglecting carrier tunneling effects on self-consistent electrostatic potential in calculating direct tunneling gate current in deep submicron MOSFETs. Comparison between simulated and experimental results shows that for accurate modeling of direct tunneling current, tunneling effects on potential profile need to be considered. The relative error in gate current due to neglecting carrier tunneling is higher at higher gate voltages and increases with decreasing oxide thickness. We also study the direct tunneling gate current in MOSFETs with high-K gate dielectrics.**

***Index Terms*—Direct tunneling current, MOSFET modeling, quantum effects, wave function penetration.**

I. Introduction

Current scaling down of MOSFET feature sizes has led to the fabrication of devices in the sub-100 nm regime, with gate-oxide thickness equal to less than 2 nm. In such devices, a high gate current flows due to the direct tunneling (DT) of inversion carriers. A number of studies have been reported in the literature on the modeling of direct tunneling gate current [1]–[9]. The electrostatic potential in silicon near silicon–gate-oxide interface is typically determined from the self-consistent solution of Schrödinger's and Poisson's equations. Closed boundary conditions commonly used for the solution of Schrödinger's equation are that the wave function goes to zero at silicon–gate-oxide interface and at some point deep inside the bulk [10]. However, due to the finite potential barrier height, some penetration of the wave function into the gate oxide occurs [5], [11]. This penetration is actually responsible for the DT gate current. Because of the computational involvement associated with the common solution techniques of Schrödinger's equation with open boundary conditions, in many studies, the potential profile is determined self-consistently neglecting the DT of the carriers, and the tunneling current is calculated in a postprocessor outside the self-consistent loop [2]–[5]. A comparison between closed and open boundary models for gate current calculation has been performed in [12], but in this study too, while using open boundary conditions, the effects of tunneling within the self-consistent loop are neglected. It is already known that the effects of carrier tunneling on potential profile is nontrivial [9], [13]. This raises questions on the accuracy of calculation of the tunneling current in a postprocessor. Recently, the DT current has been calculated considering the effects of carrier tunneling on the potential profile [7]–[9]. As stated above, inclusion of tunneling effects within the self-consistent loop results in a computationally time consuming numerical procedure.

In fact, accurate modeling of DT current depends on a number of factors such as modeling of the gate dielectric material and interface states. According to the International Technology Roadmap for semiconductors (ITRS), by 2005, the gate leakage current should be modeled within an accuracy of 40% [14]. Therefore, each of these factors should be studied carefully. In this brief, we focus on only one effect and study the validity of the approximation, which neglects the effects of carrier tunneling on potential profile and calculates the tunneling current in a postprocessor. A numerically efficient technique, proposed recently [15], has been applied in the calculation of the DT current with and without considering tunneling within the self-consistent loop. Simulated results are compared with experimental data.

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II. Theory

We use the logarithmic derivative technique of the retarded Green's function, G^R, to solve one-dimensional (1-D) Schrödinger's equation in the direction normal to the silicon–gate-oxide interface (z direction) with open boundary conditions. This method is discussed in details in Refs. [11], [15]. The logarithmic derivative of the retarded Green's function G^R is defined by

$$Z_i = \frac{2\hbar}{im_{zi}} \left[\frac{\partial G_i^R(z, z'; E)}{\partial z} \Big/ G_i^R(z, z'; E) \right] \tag{1}$$

where G_i^R is the retarded Green's function for the ith valley at point z due to a unit excitation at point z'. Since by definition, first-derivative of G^R is discontinuous at $z = z'$, two boundary conditions are required to calculate Z_i as a function of z. To obtain these conditions, it is assumed that the value of the potential deep inside the gate metal is constant at $V(-\infty)$, and the value of the potential deep inside bulk silicon is also constant at $V(\infty)$. $V(\pm\infty)$ are readily known and are given by the bulk values. This assumption implies that the wave function deep inside the semiconductor is exponentially decaying ($(E < \mathrm{eV}(\infty))$ and deep inside the gate metal, the wave function is a plane wave $(E > \mathrm{eV}(-\infty))$. From the properties of one-dimensional (1-D) Green's functions, it can be shown [15] that for all $z > z'$

$$Z_i(z, z'; E) = Z_i^+(z; E) \tag{2}$$

and for all $z < z'$

$$Z_i(z, z'; E) = Z_i^-(z; E) \tag{3}$$

i.e., Z_i^+ (Z_i^-) does not depend on z' as long as $z > z'$ ($z < z'$). $Z_i^\pm$ can be calculated as functions of z following a method analogous to the impedance transformation technique of microwave transmission lines [15].

In the presence of tunneling, the Hamiltonian for the MOS structure becomes non-Hermitian and the eigenenergies become complex, where the real part gives the energy of the jth quasi-bound state in the ith valley, E_{ij}, and the imaginary part is related to the lifetime, τ_{ij}. In order to avoid determining complex eigenenergies of a non-Hermitian matrix, we evaluate the local 1-D density-of-states (DOS) N_{1-D} at some point within the quantum well in terms of $Z_i^\pm$ [15]

$$\begin{aligned} N_{1-D_i}(z; E) &= -\frac{1}{\pi} \Im\mathrm{m}\left[G_i^R(z, z; E) \right] \\ &= \frac{4}{\pi\hbar} \Im\mathrm{m}\left[\frac{i}{Z_i^+(z; E) - Z_i^-(z; E)} \right]. \end{aligned} \tag{4}$$

E_{ij}'s are calculated by locating the peaks of N_{1-D_i} and $\tau_{ij} = \hbar/2\Gamma_{ij}$. Here, Γ_{ij} is the full-width at half-maximum (FWHM) of the energy broadened DOS around the jth quasi-bound state in the ith valley. Once E_{ij}s are calculated, corresponding wave functions, including penetration into the gate-dielectric, are evaluated in a straightforward manner using [15, (9)]. One-dimensional Poisson's equation is solved for the combined metal–oxide-semiconductor regions. As the inversion charge density, required for the solution of Poisson's equation, is described in terms of wave functions calculated with open boundary conditions, the effects of tunneling on the electrostatic potential within the self-consistent loop are taken into account. After the convergence of the self-consistent loop, the DT gate current is determined from the relationship

$$J = \sum_{ij} \frac{eN_{ij}}{\tau_{ij}} \tag{5}$$

where N_{ij} is the concentration of the inversion carriers in the jth state of the ith valley [10]. In order to calculate J without considering tunneling effects on potential profile, Schrödinger's equation within the self-consistent loop is solved with the usual closed boundary condition that the wave function goes to zero at the silicon–gate-dielectric interface.

III. Results and Discussions

The results of our numerical calculations for nMOSFETs are presented in this section. Calculations are performed at room temperature and values for different parameters for (100) silicon are taken from [10]. We have taken the substrate doping concentration N_A to be 5×10^{17} cm^{-3} and polysilicon doping density $N_{\rm poly} = 10^{20}$ cm^{-3}. These values are the same as used in [4]. The effective mass of electrons in gate-oxide region has been a topic of controversy. Using a detailed microscopic theory, Städele *et al.* have shown that the electron effective mass in oxide is not a constant and have questioned the validity of effective mass approximation in gate oxide. However, such microscopic models make routine device simulation computationally prohibitive. Therefore, the more common practice is to represent electrons in gate-oxide region by a constant effective mass, treated as a fitting parameter. We, too describe electrons in gate oxide by a constant effective mass $m_{ox} = 0.5m_0$ with a parabolic dispersion. This value was originally proposed by Weinberg [17] and has been used successfully in [4], [6] to model experimental DT current. It may be mentioned that our open boundary conditions for the solution of Schrödinger's equation will remain unaffected even if the gate-oxide region is represented by a microscopic model, since these condictions are applied deep inside the gate metal as well as deep inside the bulk silicon and do not depend on how the oxide is modeled.

Fig. 1 shows the calculated DT gate current with and without considering carrier tunneling effects on the self-consistent electrostatic potential. Results are also compared with the experimental data of [4] for the same widths of the gate oxide. It is found that excellent agreement between simulated and experimental values is obtained when carrier tunneling effects on electrostatic potential are incorporated in the calculation. The DT current is underestimated when it is evaluated in a postprocessor outside the self-consistent loop. The relative errors in the DT currents due to the neglect of the tunneling effects, for the devices studied in Fig. 1, are presented in Fig. 2. Fig. 2 also shows the errors in devices with gate-oxide thickness $T_{\rm ox} = 0.5$ nm and 1.0 nm. We observe that the errors are significant for the entire range of the gate voltage. The error increases with increasing gate voltage since, at higher gate voltages, the effects of carrier tunneling on electrostatic potential become more dominant [13]. Moreover, the error also increases with a reduction in gate-oxide thickness. Therefore, we conclude that the effects of neglecting carrier tunneling on potential profile in calculating DT current becomes more dominant with device scaling.

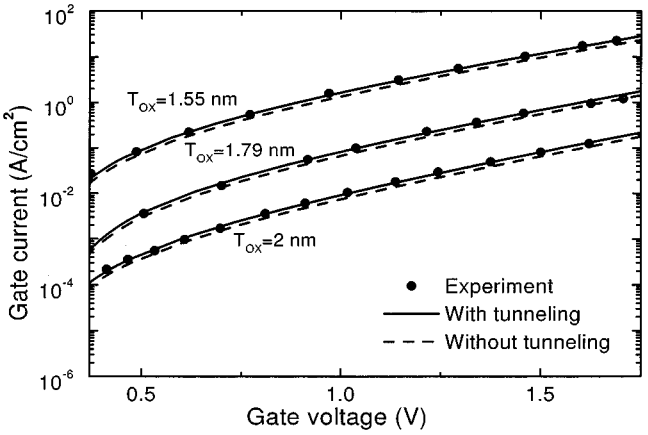

Fig. 1. Comparison of simulated DT gate currents, calculated with and without considering carrier tunneling effects on electrostatic potential, with experimental results (from [4]). Here, SiO_2 is the gate-dielectric material.

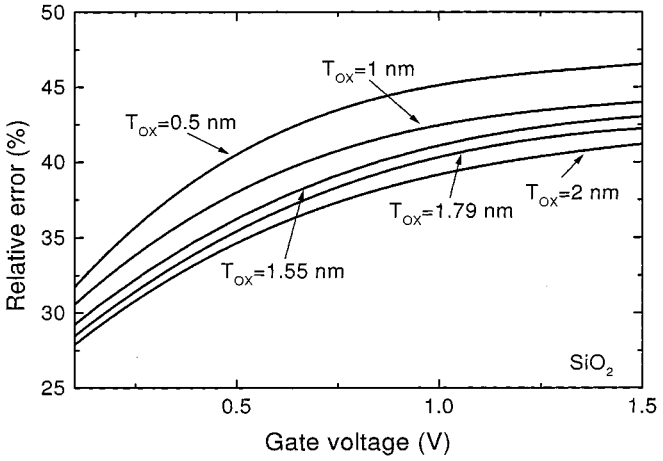

Fig. 2. Relative errors due to neglecting carrier tunneling effects in DT gate currents for devices with different SiO_2 thickness.

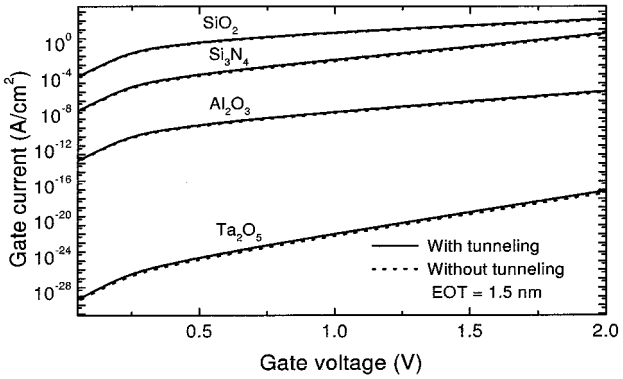

Fig. 3. Simulated DT gate currents in MOSFETs with high-K gate-dielectrics for an EOT $= 1.5$ nm, calculated with and without considering carrier tunneling effects on electrostatic potential.

Next, we study DT current in MOSFETs with high-K gate dielectrics. Aluminum with a work function equal to 4.1 eV is considered as the gate metal for the devices studied in Figs. 3 and 4. Substrate doping density is the same as that for the devices studied in Fig. 1. Fig. 3 is the plot of DT currents for devices with different

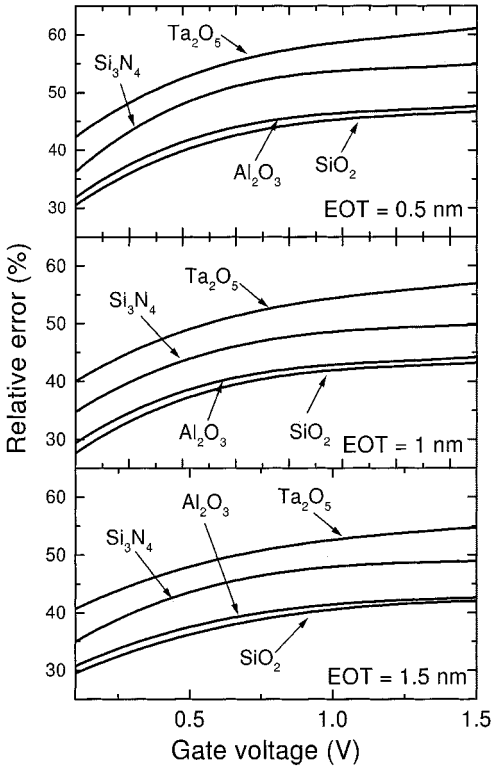

Fig. 4. Relative errors due to neglecting carrier tunneling effects in DT currents through high-K dielectrics of three different equivalent-oxide thickness (EOT).

TABLE I
DIELECTRIC CONSTANTS AND CONDUCTION BAND OFFSETS AT SILICON–DIELECTRIC INTERFACE FOR DIFFERENT DIELECTRIC MATERIALS USED IN OUR CALCULATION FROM [18]

Material	Dielectric constant (K)	ΔE_C (eV) to silicon
SiO_2	3.9	3.2
Si_3N_4	7	2
Al_2O_3	9	2.8
Ta_2O_5	26	1-1.5

gate dielectrics for an equivalent-oxide thickness (EOT) of 1.5 nm. In the absence of any widely accepted model for electron effective mass in gate-dielectric region, we assume that it is the same as that in SiO_2, i.e., $0.5m_0$ with a parabolic dispersion. The values of the dielectric constants (K) and the conduction-band offsets at silicon-gate-dielectric interface, ΔE_C have been taken from [18] and are given in Table I. As expected, the DT current decreases with an increase in K because of the increase of the physical oxide thickness. Fig. 4 shows the relative errors in the DT currents for three different EOT. The error increases with decreasing ΔE_C. We have numerically verified that with a reduction in potential barrier height for inversion electrons at silicon–gate-dielectric interface, the effects of carrier tunneling on electrostatic potential increases even for the same EOT. Consequently, the error in the tunneling current also increases. Again, we find that for a given dielectric, the error is higher for lower EOT.

IV. CONCLUSION

We have studied the validity of the assumption of neglecting carrier tunneling effects on electrostatic potential in calculating direct tunneling gate current in deep submicron MOSFETs. It is concluded that for accurate modeling of the DT gate current, tunneling effects on potential profile should be taken into account. Neglect of the tunneling effects on potential profile leads to an underestimation of the DT current. The relative error is significant over the entire range of the gate voltage and increases with decreasing oxide thickness. We have also studied the DT current in MOSFETs with high-K gate dielectrics. Results show that the error in calculating the tunneling current for the same EOT increases with decrease in the potential barrier height at silicon–gate-dielectric interface. Also, for a given gate dielectric, the error increases with device scaling.

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