Computationally efficient quantum-mechanical technique to calculate the direct tunneling gate current in metal-oxide-semiconductor structures

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We propose a computationally efficient, accurate and numerically stable quantum-mechanical technique to calculate the direct tunneling (DT) gate current in metal-oxide-semiconductor (MOS) structures. Knowledge of the imaginary part Γ of the complex eigenenergy of the quasi-bound inversion layer states is required to estimate the lifetimes of these states. Exploiting the numerically obtained exponential dependence of Γ on the thickness of the gate-dielectric layer even in the sub-1-nm-thickness regime, we have simplified the determination of Γ in devices where it is too small to be calculated directly. It is also shown that the MOS electrostatics, calculated self-consistently with open boundary conditions, is independent of the dielectric layer thickness provided that the other parameters remain unchanged. Utilizing these findings, a computationally efficient and numerically stable method is developed for calculating the *tunneling current–gate voltage* characteristics. The validity of the proposed model is demonstrated by comparing simulation results with experimental data. Sample calculations for MOS transistors with high-K gate-dielectric materials are also presented. This model is particularly suitable for DT current calculation in devices with thicker gate dielectrics and in device or process characterization from the tunneling current measurement. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1589173]

I. INTRODUCTION

Current scaling of metal-oxide-semiconductor field-effect-transistors (MOSFET) has led to the fabrication of devices in the sub-100-nm regime. In such devices, a large gate current flows due to the direct tunneling (DT) of inversion carriers. This DT current is important from both device performance and characterization points of view. Many studies have been reported on the modeling of direct tunneling gate current.[1–12] These studies can be broadly classified into a semiclassical (SC)[2–4] and a quantum-mechanical (QM)[1,7–9] method. SC techniques are based on the calculation of the transmission probability, usually employ the WKB approximation, and often ignore the two-dimensional (2D) nature of the inversion electrons. A modified WKB approximation has been proposed in Ref. 5 to include the effects of reflections from potential discontinuities. This approximation has been applied in Ref. 6 with reasonable success to obtain quantitative agreement between model and experiment. On the other hand, QM methods consider the finite lifetime of the quasi-bound, 2D inversion carriers. QM methods are preferred when Schrödinger's equation is to be solved with open boundary conditions including the effects of wave function penetration into the gate dielectric. A number of recent studies have compared the two DT current calculation techniques in MOS devices.[8,10,11] While the QM methods have a more rigorous physical basis and provide more accurate simulation results, they are also numerically more complicated to apply in practical situations. Because of the numerical difficulties, meaningful results could hardly be obtained in Ref. 10 using a QM method for MOS structures with gate-oxide thickness greater than 3 nm, even though calculation of the tunneling current through such thick oxide layers is necessary in many applications, e.g., flash memory devices and device and process characterization from the tunneling current measurement. For this reason, in spite of the known accuracy of the QM methods, SC techniques are often used although many of the approximations involved in the SC techniques cannot yet be physically justified.

In this article, we propose a computationally efficient technique to calculate the DT gate current in MOSFETs using a QM method. This technique is accurate and is free from the numerical limitations of the existing QM methods. The effect of wave function penetration on self-consistent electrostatic potential is also accounted for. This effect has recently been shown to be an important factor for accurate modeling of DT current.[12]

II. MATHEMATICAL MODEL

In our QM model, we make the approximations usually invoked in most DT current calculations.[1–12] One-dimensional (1D) calculation is performed to determine the self-consistent potential profile. We assume that the tunneling rate is small enough so that the inversion carriers can be taken to be in thermal equilibrium. The conduction electrons are described in terms of single-band effective mass Hamiltonian and electrons in the gate-dielectric region are represented by a constant effective mass m_{ox} with a parabolic dispersion relationship. Although a few recent studies have focused on determining m_{ox} in SiO_2 and a number of other

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high-K dielectric materials,[13] in the absence of detailed knowledge about the bandstructures of the dielectric materials, m_{ox} is still widely treated as a fitting parameter.

When electrons tunnel out of a MOS inversion layer, the system becomes quasibound with finite lifetimes of the inversion carriers. In such a system, the eigenenergies are complex quantities: $E_{ij} \rightarrow E_{ij} + i\Gamma_{ij}$. Here, the real part E_{ij} is the energy of the jth quasi-bound state in the ith valley and the imaginary part Γ_{ij} is related to the lifetime τ_{ij} of the corresponding state following the relationship $\tau_{ij} = \hbar/2\Gamma_{ij}$. According to the QM methods, the DT current is calculated from the known values of τ_{ij} using Eq. (1):

$$J = \sum_{ij} \frac{eN_{ij}}{\tau_{ij}}, \tag{1}$$

where, N_{ij}, the concentration of the inversion electrons in the jth state of the ith valley, is given by

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{E_F - E_{ij}}{kT}\right)\right]. \tag{2}$$

In Eq. (2), n_{vi} is the valley degeneracy, m_{di} is the density-of-states (DOS) effective mass of electrons, and E_F is the Fermi energy.

Many different schemes have been proposed to calculate Γ. In Ref. 7, Schrödinger's equation has been discretized using a finite difference technique. As a consequence of using open boundary conditions, the Hamiltonian matrix, defined over a finite region of interest, becomes non-Hermitian. Numerical determination of the complex eigenvalues of the non-Hermitian matrix provides an estimation of Γ. Reference 14 has shown that the energy derivative of the phase of the reflection coefficient (determined using the transfer matrix formalism) around the energies of each quasi-bound state has a Lorentzian form and its full width at half-maximum (FWHM) is equal to Γ. This method has been applied in Refs. 10 and 11 to calculate the lifetimes. However, from a numerical standpoint, direct calculation of such a derivative is difficult.[11] Therefore, a suggestion has been made in Ref. 11 to calculate Γ from the diagonal element of the transfer matrix. Since the transfer matrix method itself suffers from numerical instability, we have earlier proposed another means for calculating Γ in Ref. 15. In a truly bound system, the 1D local DOS, N_{1D}, is given by a series of delta functions at the eigenenergies. When leakage occurs, N_{1D} broadens in energy and becomes a Lorentzian function. Γ can be estimated from the FWHM of the energy broadened N_{1D}. The Green's function formalism is applied to estimate N_{1D}. The 1D local DOS, by definition, is related to the diagonal element of the retarded Green's function G^R:[16]

$$N_{1D}(z;E) = -\frac{1}{\pi} \Im\mathrm{m}[G^R(z,z;E)], \tag{3}$$

where z direction is normal to the silicon–dielectric interface. The diagonal element of G^R can easily be calculated with open boundary conditions using the logarithmic derivative technique, which has been described in detail in Ref. 16. An advantage of this technique is that it is free from any matrix manipulation, and consequently, it is computationally efficient and numerically stable.

Although Γ and τ can be calculated in a straightforward way using Eq. (3), it requires N_{1D} to be resolved in energy with sufficient accuracy to calculate the FWHM. Normally, in devices with gate-oxide thickness (T_{ox}) equal to less than 2.5 nm, this poses no serious limitation. However, in structures with $T_{ox} \geqslant 3$ nm, Γ is very small and its determination demands precisions which are much higher than usual thus requiring very high computational time. A similar situation arises in modeling MOSFETs with high-K gate-dielectric materials. As T_{ox} goes below 1 nm, to reduce the DT gate current and to increase reliability, the ITRS roadmap has called for possible replacement of SiO_2 by high-K gate dielectric materials.[17] Due to the higher physical thickness of the high-K dielectric layers for a given equivalent oxide thickness (EOT), the tunneling rate decreases and Γ becomes rather small in these devices. Also in many cases, such as trend studies for a particular technology and parameter extraction, it is necessary to perform DT current calculations many times for the same basic structure. Due to the necessity of solving Schrödinger's and Poisson's equations iteratively with open boundary conditions each time, the problem becomes computationally arduous and often accuracy must be compromised in order to achieve higher speed. In the following sections, we address both these issues and provide an alternate way to perform these calculations.

III. CALCULATION OF Γ

In this section, we numerically calculate the imaginary part of the complex eigenenergy, Γ, for a number of device structures with different gate-dielectric materials, and propose an empirical expression for Γ. This expression can be used to estimate Γ efficiently in devices where it is too small to be calculated accurately by direct evaluation of the FWHM.

Numerical results are obtained by self-consistent solution of coupled Schrödinger's and Poisson's equations. Effects of wave function penetration on the self-consistent potential profile are taken into account by solving Schrödinger's equation with open boundary conditions within the self-consistent loop and by solving Poisson's equation over the entire MOS structure.[12] nMOS devices are assumed to be fabricated on (100) silicon. Values of different parameters for (100) silicon are given in Ref. 18. As already mentioned in Sec. II, we have treated m_{ox} as a fitting parameter with a value equal to $0.5m_0$ for SiO_2 as well as for other dielectrics. This value for SiO_2 has been obtained by fitting simulated DT current with experimental data.[19] A metal gate with a work function equal to 4.1 eV is considered. The conduction band offsets of various dielectrics with silicon, ΔE_C, and the dielectric constants, K, of these materials are taken from Ref. 20 and are presented in Table I.

Figure 1 shows calculated Γ of the lowest energy state as a function of the physical layer thickness for three gate-dielectric materials. Substrate doping density $N_A = 10^{18}$ cm^{-3}. Each curve is for a fixed inversion carrier den-

TABLE I. Dielectric constants and conduction band offsets at silicon–dielectric interface for different dielectric materials used in our calculation (see Ref. 20).

Material	Dielectric constant, K	ΔE_C to silicon (eV)
SiO_2	3.9	3.2
Si_3N_4	7	2
Ta_2O_5	26	1.3

sity, $N_s=\Sigma_{ij}N_{ij}$. It is observed that for a given N_s, Γ decreases exponentially with increase in dielectric layer thickness for all the materials. At higher thickness of the dielectric layers, the exponential dependence is *expected* to hold, but it is found to be valid even for a dielectric layer thickness of 0.5 nm, where Γ is within two orders of magnitude of the real part of the complex energy. In practical devices, there is usually some residual oxide between the high-K dielectric and the silicon substrate. This is due to the presence of native oxide formed during fabrication. Also in some cases, SiO_2-high-K dielectric stacks are fabricated intentionally to achieve a better control over the interface state density and barrier properties.[20] Therefore, we investigate Γ for the stack-gate structures. Figure 2 shows Γ of the lowest energy state for two stack-gate structures as a function of EOT for different values of N_s. The stacks consist of a 0.5 nm native oxide layer between high-K material and silicon substrate. The value of m_{ox} and N_A are the same as those used in Fig. 1. We see from Fig. 2 that Γ of the stack structures also depend on EOT in an exponential manner. We have also calculated Γ for higher energy states (results not shown) and its dependence on dielectric layer thickness or EOT has been found to be similar to that of the lowest state. From these results, we propose the following empirical expression for Γ as a function of dielectric layer thickness:

$$\Gamma=\Gamma_O e^{-T_{ox}/L}, \tag{4}$$

where Γ_O and L are empirical constants. T_{ox} in Eq. (4) represents physical thickness in the case of pure dielectric layers, and EOT in dielectric stacks. It should be noted that Eq. (4) remains valid as long as Γ for each state is much smaller than the separation between the energies of the adjacent quasi-bound states.

Γ for the lowest energy state is plotted as a function of the thickness of the dielectric layer for three different dielectric materials in Fig. 3 for $N_A=2\times10^{18}$ cm^{-3}. Other parameters are the same as those used in Fig. 1. Electron effective mass m_{ox} in the gate-dielectric region also has an important effect on Γ. m_{ox} in general, decreases with decreasing ΔE_C.[13] Figure 4 is the plot of Γ for Si_3N_4 and Ta_2O_5 gate dielectrics where m_{ox} values of 0.4 and $0.25m_0$ have been used for Si_3N_4 and Ta_2O_5, respectively. From the results presented in Figs. 1–4, it is evident that Eq. (4) remains valid for a wide range of parameter values and Γ_O and L are functions of the dielectric material, substrate doping density N_A, inversion carrier density N_s, and electron effective mass in dielectric region m_{ox}. Table II summarizes the extracted values of Γ_O and L (physical thickness) as functions

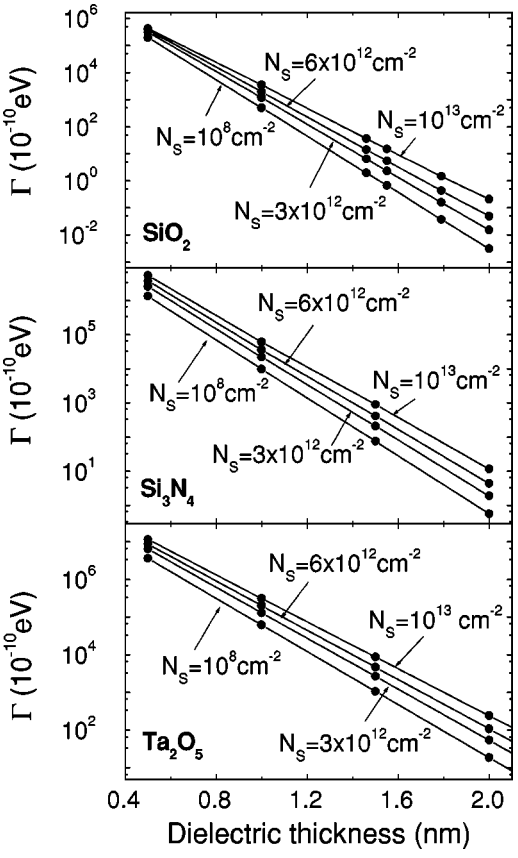

FIG. 1. Imaginary part of the lowest eigenenergy, Γ, as a function of physical thickness of various gate dielectric layers at different inversion charge densities, N_S. Substrate doping density $N_A=10^{18}$ cm^{-3}.

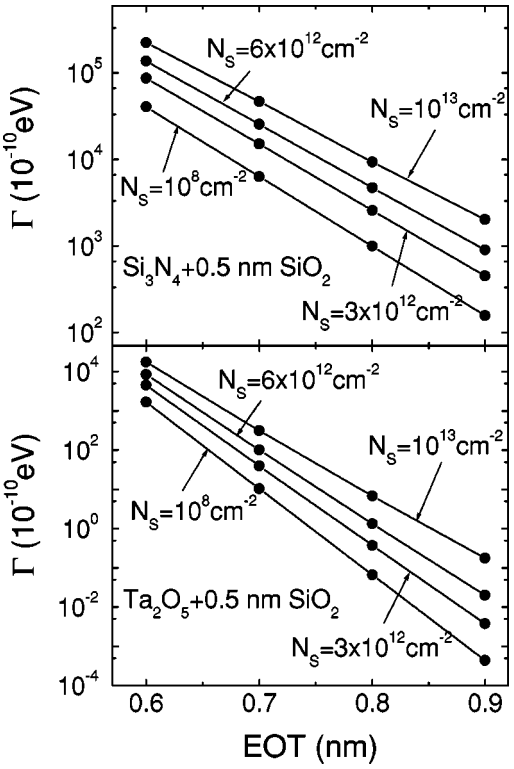

FIG. 2. Γ, as a function of equivalent oxide thickness (EOT) for stack gate structures at different inversion charge densities, N_S. Substrate doping density $N_A=10^{18}$ cm^{-3}.

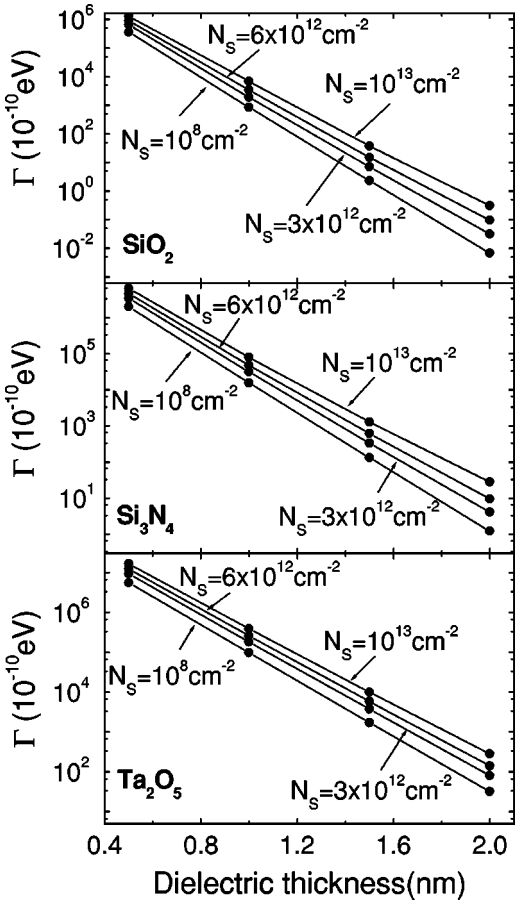

FIG. 3. Γ vs physical thickness of various gate dielectric layers at different N_S for a substrate doping density $N_A=2\times10^{18}$ cm^{-3}.

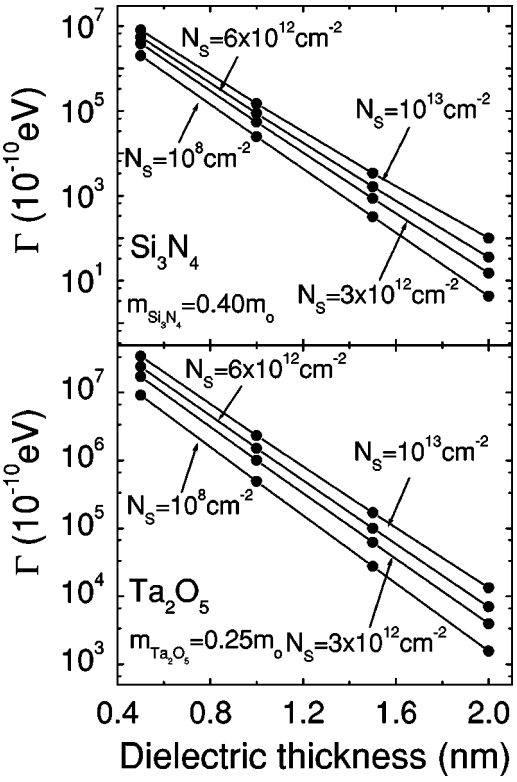

FIG. 4. Γ vs physical thickness of two gate dielectric layers for different values of electron effective mass in gate-dielectric region.

of MOS physical parameters. It is shown that L depends very weakly on N_s and N_A, but is sensitive to changes in ΔE_C. Γ_O increases with increasing N_A and N_s and also increases with decreasing ΔE_C. A reduction in $m_{\rm ox}$ causes Γ_O to decrease slightly with a corresponding increase in L.

Equation (4) can be used in a useful way to estimate Γ in devices with thicker dielectrics or with different dielectric layer thicknesses. For a given gate-dielectric material, N_A and $m_{\rm ox}$, we calculate Γ for each N_s corresponding to two small values of EOT by direct evaluation of the FWHM. Since Γ is relatively large for these devices, determination of the FWHM faces no numerical difficulty. These results are used to obtain Γ_O and L for each N_s. Equation (4) is then applied to find Γ for different values of EOT without having to perform any additional calculation. Equation (4) is applicable even where direct estimation of the FWHM is beyond the precision limit of the compiler. In order to investigate the regime of validity of Eq. (4), Γ has also been calculated with an energy or gate bias dependent $m_{\rm ox}$. As long as $m_{\rm ox}$ does not depend on $T_{\rm ox}$, the form of Eq. (4) is found to remain valid. It should also be pointed out that although we have reached Eq. (4) using the Green's function formalism, this relationship is quite general and is independent of the technique employed to calculate Γ. Therefore, any of the existing methods[7,11,14,15] may be used along with Eq. (4) to estimate Γ efficiently in devices where it is too small to be determined directly.

IV. DT GATE CURRENT

In order to calculate the DT current, in addition to Γ, it is necessary to estimate N_{ij} [Eq. (2)]. N_{ij}, in turn, depends on E_{ij} measured relative to the Fermi energy. E_{ij} is usually determined from the self-consistent solution of Schrödinger's and Poisson's equations. Figure 5 shows the real part of the lowest eigenenergy E_{11} for three different dielectric materials as a function of the dielectric layer thickness for a given substrate doping density. While for the same N_s, E_{11} varies from dielectric to dielectric due to different amount of wave function penetration into the gate-dielectric region, for a given N_s and a given dielectric material, E_{11} is independent of the layer thickness even down to 0.5 nm. E_{ij} is known to be independent of dielectric material and $T_{\rm ox}$ when Schrödinger's equation is solved with closed boundary conditions,[18] but even the use of open boundary conditions does not make E_{ij} depend on $T_{\rm ox}$ for the range considered here. The same trend is also observed for higher subbands (results not shown). This implies that N_{ij} remains unaffected as the dielectric layer thickness is changed keeping other parameters the same. Consequently, to calculate the DT current in devices with different dielectric layer thicknesses, N_{ij} obtained for a device with a thinner dielectric layer during estimation of Γ_O and L may be used instead of resolving Schrödinger's equation each time. To calculate the gate voltage corresponding to a certain inversion carrier density N_s, one typically uses Eq. (5):

$$V_{GS}=V_{\rm ox}+\varphi_s+\varphi_{ms}+V_{\rm poly}. \quad (5)$$

TABLE II. Extracted values of Γ_O and L [Eq. (4)] for different combinations of MOS physical parameters.

Physical parameters		Dielectric materials and m_{ox}					
		SiO_2 ($m_{ox}=0.5m_0$)		Si_3N_4 ($m_{ox}=0.5m_0$)		Si_3N_4 ($m_{ox}=0.4m_0$)	
N_A (cm^{-3})	N_s (cm^{-2})	Γ_O (meV)	L (nm)	Γ_O (meV)	L (nm)	Γ_O (meV)	L (nm)
10^{18}	10^8	10.5	0.082	18.3	0.102	16.2	0.114
	3×10^{12}	16.3	0.086	30.0	0.105	26.9	0.118
	6×10^{12}	19.4	0.089	37.9	0.108	34.2	0.121
	10^{13}	22.2	0.094	47.0	0.112	42.9	0.125
2×10^{18}	10^8	15.3	0.083	25.5	0.103	22.7	0.115
	3×10^{12}	22.0	0.086	37.3	0.107	33.5	0.119
	6×10^{12}	25.9	0.088	44.4	0.110	40.2	0.123
	10^{13}	30.1	0.091	52.5	0.114	48.2	0.127

Here, V_{ox} is the voltage drop across the dielectric layer, φ_s is the silicon surface potential, φ_{ms} is the work function difference, and V_{poly} is the voltage drop due to depletion effects in the polysilicon gate. We have verified that even in strong inversion, the relationship $V_{ox}=T_{ox}F_{ox}$ can be used to estimate the voltage drop across the dielectric layer with an error less than 1%. Here, F_{ox} is the electric field within the dielectric at the silicon–dielectric interface. In Fig. 6, silicon surface potential φ_s for different dielectrics are presented as a function of the dielectric layer thickness. Again we find that φ_s is different for different dielectrics due to wave function penetration effects (the differences increasing with increasing N_s), but for a given dielectric material and a given N_s, φ_s does not depend on the thickness of the dielectric layer for a thickness as low as 0.5 nm. We have also observed that V_{poly} is independent of the thickness of the dielectric layer. From the above discussion, it is evident that the need for solving Schrödinger's and Poisson's equations self-consistently each time is completely *eliminated* in calculating the DT current through dielectric layers of different thicknesses. Once MOS electrostatics is self-consistently solved for two structures with thinner gate dielectric layers, the obtained information can be used in a computationally efficient and straightforward way to accurately determine the DT current and the corresponding gate voltage in similar structures at any other dielectric layer thickness. Thus the problem of calculating the *tunneling current–gate voltage characteristics* is greatly simplified for cases where it is necessary to perform the calculation in a device with a thick dielectric layer or in similar structures with many different dielectric layer thicknesses. Such situations may arise in flash memory devices and in device and process characterization by tunneling current measurement.

We now check the validity of the proposed model by comparing our simulated DT current with experimental data. For this purpose, we consider MOS devices with SiO_2 gate dielectric. The substrate and the polysilicon doping densities are 5×10^{17} and 10^{20} cm^{-3}, respectively. Figure 7 is the plot of our simulated DT current evaluated using two different techniques. Both techniques use Eq. (1) for the current calculation. In the first method, Γ_{ij} for all four devices is obtained by direct evaluation of the FWHM of the energy broadened 1D DOS and MOS electrostatics is independently calculated each time. In the second method, Γ_{ij} for the two devices with $T_{ox}=1.46$ and 1.55 nm are estimated by direct

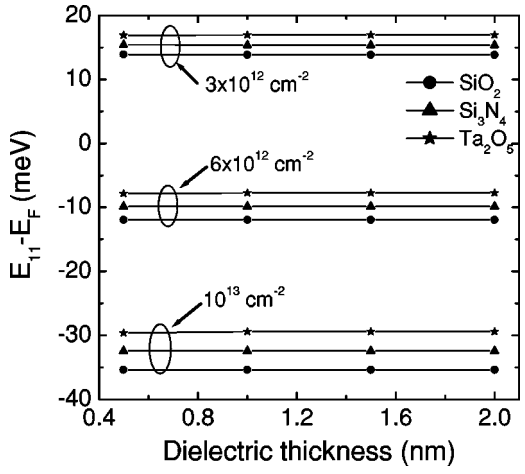

FIG. 5. Real part of the lowest eigenenergy, measured relative to the Fermi energy, as a function of the physical thickness of various gate dielectric layers.

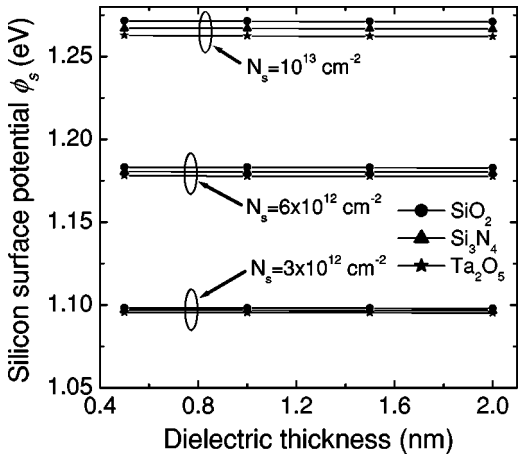

FIG. 6. Silicon surface potential φ_s as a function of the physical thickness of various gate dielectric layers.

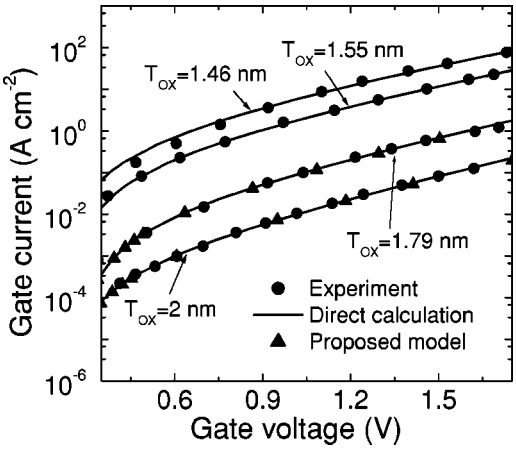

FIG. 7. Comparison of the simulated DT gate current, calculated by two different approaches, with experimental result from (Ref. 6) Here SiO_2 is the gate-dielectric material.

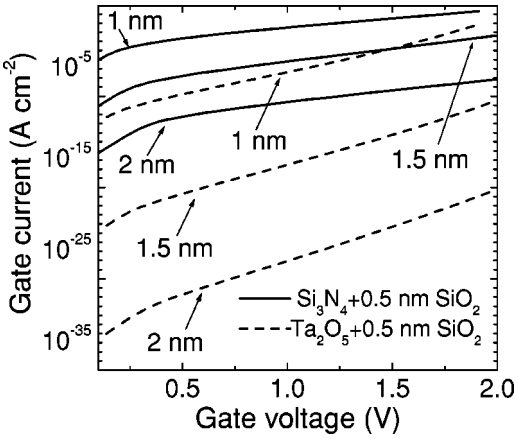

FIG. 9. Simulated DT gate current in MOSFETs with stack-gate structures for different values of EOT. Calculations are performed using the proposed technique.

calculation of the FWHM. These values are used to obtain Γ_O and L at each N_s. Equation (4) then gives Γ_{ij} required to calculate the DT gate current in the two devices with thicker gate-oxide layers. N_{ij}, φ_s, V_{poly}, and F_{ox} for the two thicker devices are also obtained from the corresponding values in the thinner devices. Results of the two simulation techniques are found to be identical. Excellent agreement between simulation and measurement (data taken from Ref. 6) is achieved which demonstrates the accuracy of the proposed method.

Next, the proposed technique is applied to calculate DT gate current in MOS structures with high-K gate dielectrics where direct evaluation of Γ requires extremely high numerical precision. Device parameters are as mentioned in Sect. III. Figure 8 shows DT gate current as a function of gate voltage for Si_3N_4 and Ta_2O_5 gate-dielectric materials at three values of EOT. As expected, for a given EOT, the current decreases significantly with increase in dielectric constant. This is due to the fact that the physical thickness of the dielectric layer increases with an increase in the dielectric constant when EOT remains fixed. Higher slope of the gate current for Ta_2O_5 dielectric has been attributed to its lower value of ΔE_C, in agreement with the results of Ref. 7. In Fig. 8, we have calculated gate current as low as 10^{-45} A cm^{-2} without running into any numerical difficulty. Such low current would have been extremely difficult to calculate using the existing QM techniques.

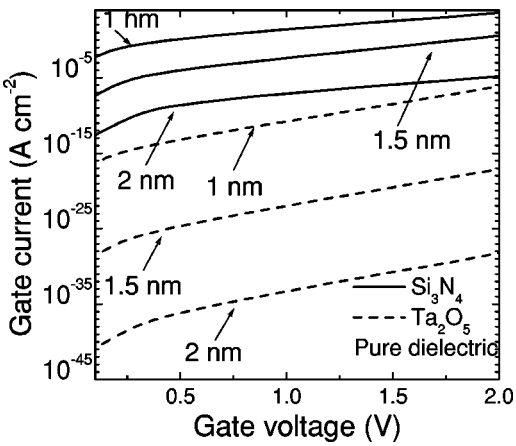

FIG. 8. Simulated DT gate current in MOSFETs with pure high-K gate-dielectric materials for different values of EOT. Calculations are performed using the proposed technique.

Finally, we study the gate current through dielectric stacks in Fig. 9. The stack structures are described in Sec. III. Again, using the proposed technique, we have been able to estimate very low values of the gate current without any computational difficulty. It is observed that the gate current increases sharply when a pure high-K dielectric layer is replaced by a stack structure with the same EOT. The reason for this increase is the reduction in the physical thickness of the dielectric layer as pointed out in Ref. 7. This phenomenon is particularly stronger in devices with higher EOT and lower ΔE_C.

V. CONCLUSIONS

We have proposed a computationally efficient, accurate, and numerically stable QM technique for calculating the direct tunneling gate current in MOS devices. Utilizing the numerically obtained exponential dependence of the inverse lifetime of the quasi-bound states on dielectric layer thickness, we have suggested an easy way for estimating lifetimes in devices with thicker gate dielectrics where direct determination is very difficult due to numerical limitations. When DT current in many similar devices with different dielectric layer thicknesses is to be calculated, independence of the MOS electrostatics on the thickness of the dielectric layer eliminates the need for self-consistent solutions of Schrödinger's and Poisson's equations in all structures except for two with thinner dielectric layers. As a consequence, calculation of the tunneling current is greatly simplified. The validity of our method has been demonstrated by comparing simulated results with experimental data. Sample calculations of the DT gate current in MOSFETs with high-K gate dielectric have been presented which shows the effectiveness of the proposed technique.

[1] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, IEEE Electron Device Lett. **18**, 209 (1997).

[2] A. Schenk and G. Heiser, J. Appl. Phys. **81**, 7900 (1997).
[3] E. M. Vogel, K. Z. Ahmed, B. Hornung, W. K. Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, IEEE Trans. Electron Devices **45**, 1350 (1998).
[4] H. Y. Yang, H. Niimi, and G. Lucovsky, J. Appl. Phys. **83**, 2327 (1998).
[5] L. F. Register, E. Rosenbaum, and K. Yang, Appl. Phys. Lett. **74**, 457 (1999).
[6] N. Yang, W. K. Henson, J. R. Hauser, and J. J. Wortman, IEEE Trans. Electron Devices **46**, 1464 (1999).
[7] S. Mudanai, Y.-Y. Fan, Q. Ouyang, A. F. Tasch, and S. K. Banerjee, IEEE Trans. Electron Devices **47**, 1851 (2000).
[8] E. Cassan, P. Dollfus, S. Galdin, and P. Hesto, IEEE Trans. Electron Devices **48**, 715 (2001).
[9] K. Alam, S. Zaman, M. M. Chowdhury, M. R. Khan, and A. Haque, J. Appl. Phys. **92**, 937 (2002).
[10] A. D. Serra, A. Abramo, P. Palestri, L. Selmi, and F. Widdershoven, IEEE Trans. Electron Devices **48**, 1811 (2001).
[11] R. Clerc, A. Spinelli, G. Ghibaudo, and G. Pananakakis, J. Appl. Phys. **91**, 1400 (2002).
[12] M. M. A. Hakim and A. Haque, IEEE Trans. Electron Devices **49**, 1669 (2002).
[13] Y.-C. Yeo, T.-J. King, and C. Hu, Appl. Phys. Lett. **81**, 2091 (2002).
[14] G. Gildenblat, B. Gelmont, and S. Vatannia, J. Appl. Phys. **77**, 6327 (1995).
[15] A. Rahman and A. Haque, Solid-State Electron. **45**, 755 (2001).
[16] A. Haque and A. N. Khondker, J. Appl. Phys. **84**, 5802 (1998).
[17] The International Technology Roadmap for Semiconductors (ITRS); available on-line at http://public.itrs.net/Files/2001ITRS/home.htm
[18] F. Stern, Phys. Rev. B **5**, 4891 (1972).
[19] A. Ghetti, C.-T. Liu, M. Mastrapasqua, and E. Sangiorgi, Solid-State Electron. **44**, 1523 (2000).
[20] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).