On-Chip Timing Measurement Architecture with Femtosecond Resolution

M. Collins, B. M. Al-Hashimi and P. R. Wilson

Abstract: A new timing measurement architecture based on the time-to-digital conversion technique is presented. The architecture occupies a small silicon area (200μm by 185μm) in a 0.12μm CMOS process and can achieve tens of femtoseconds timing resolution which is the highest reported to-date.

Introduction: The International Technology Roadmap for Semiconductors (ITRS'05) is predicting that by 2010 clock frequencies of high performance VLSI devices will increase into tens of GHz. To perform timing measurements of such devices, timing measurement architectures with capabilities of tens of femtoseconds will be required. A solution to this requirement involves placing a single time measurement architecture directly onto the same silicon as the device under test [1]. Timing architectures with different timing resolutions have been proposed (Table.1). As can be seen, whilst the various architectures are capable of achieving timing resolutions in the picoseconds range, no single architecture reported to-date is capable of achieving femtosecond resolution. This letter describes a new on-chip timing measurement architecture with femtosecond resolution.

Architecture Description: The proposed timing measurement (TM) architecture (Fig. 1) is based on the time-to-digital conversion (TDC) technique [2]. The architecture has three components: an analogue mixer, a low-pass filter (LPF) and an analogue-to-digital converter (ADC). The mixer and the LPF converts a phase difference (time) between the input and a reference signal into a dc voltage, V_{dc}, that is proportional to the phase difference. The ADC converts this dc voltage into a digital output code, (D_0 to D_N), which corresponds to the time difference between the input signal and the reference signal. In implementing the TM architecture, it is necessary to keep the design as simple as possible to minimise the area overhead, yet capable of achieving the required timing resolution. These characteristics are requisites if such architectures are to be integrated on the same silicon as the DUT. An additional requirement is that the TM architecture must operate at a power supply voltage of 1.2V required by the chosen technology. This has the benefit of being low power and compatible with modern CMOS technologies. As a result of these requisites, a cascode mixer (Fig.2) was chosen.

Transistors M3 and M4 form a constant current source, the inputs, *Vin* and *Vref***,** are applied to the gates of transistors M1 and M2 respectively and the resulting modulated output is taken from the drains of transistors M2 and M4. To realise the LPF of the proposed TM architecture, a 2^{nd}-order switched-capacitor (SC) filter with f_c = 100 kHz was used. To reduce charge injection and clock feedthrough, dummy transistors and an appropriate clocking scheme was used. The key to achieving femtosecond timing resolution using the proposed architecture is the implementation of a high resolution ADC. Hence, the ΔΣ ADC was selected as apposed to Nyquist rate ADCs due to it's high resolution and it's conversion accuracy does not depend on precise component matching. The ΔΣ ADC (Fig. 1) consists of a ΔΣ modulator and a decimation filter. There exists numerous ΔΣ ADC architectures [6] and the choice usually involves trade-offs between resolution, circuit complexity and stability. Through extensive simulations, we have found that a 1^{st}-order ΔΣ ADC with an oversampling ratio (OSR) of 32 is sufficient to achieve femtosecond timing resolution avoiding stability and complexity issues often associated with higher-order converters. The 1^{st}-order modulator (Fig. 3) is based on a SC implementation, where Φ1 and Φ2 are non-overlapped clocks. Φ1d and Φ2d have their falling edges delayed compared to Φ1 and Φ2 to reduce charge injection. VrefP and VrefM are reference voltages required by the DAC of the ΔΣ modulator. The operational amplifier (OPAMP) used in the integrator is a critical element in the ΔΣ modulator. Any integrator leakage resulting from the finite dc gain of the opamp reduces the modulator attenuation of the quantization noise at low frequencies. Hence, the required minimum dc gain is chosen slightly larger than the OSR. The OPAMP (Fig. 4) employed in the modulator (Fig.3) is based on the folded cascode topology [6]. The bias circuitry is not shown for simplicity. The OPAMP transistor sizes have been designed to achieve a DC gain of 60dB. Numerous topologies of decimation filters have been reported with various trade-offs in complexity and performance. In order to meet our key requisites, (small area, low voltage and high resolution capability), a sinc filter based on the accumulate and dump architecture [6] was selected. This type of filter outputs a running average of the single bit input data stream form the modulator. The filter's topology consists of a counter, a clock divider and a register making it economically suitable for TM architectures as it is small and easy to integrate.

Results: To verify the performance of the proposed TM architecture, simulations were made using BSIM3v3 foundry models for a 0.12μm CMOS process. Fig. 5 shows the output of the LPF when an

input phase delay of two 1 GHz clock signals is varied from 0 to 500fs. As expected, there is a linear relationship between the voltage output and the phase difference of the input. It should be noted that this linearity is achieved over femtoseconds range through the use of the analogue mixer and LPF architecture. This is currently not achievable with TM architectures based on time-to-voltage conversion [4] reported to-date and this is a key requisite to achieving TM architectures with femtosecond resolution. To further demonstrate the operation of the proposed TM architecture, Fig. 6 shows a simulation with two input clock signals (Clock_in and Clock_ref) with a phase difference ($\Delta\Phi$) of 40fs. The output from the mixer and the LPF is shown in the third and forth plots respectively and the output from the $\Delta\Sigma$ modulator is shown in the fifth plot. The total silicon area of the proposed TM architecture is 200μm by 185μm, making it ideal for on-chip time measurements.

Conclusion: A new on-chip time measurement architecture based on the TDC method is proposed. This has been achieved through appropriate selection of mixer, filter and data conversion techniques. Simulations using BSIM3v3 models for a 0.12μm CMOS process show that measurements are capable with a resolution of 40fs which is the highest reported to-date. Such timing resolution is needed for future VLSI devices.

Acknowledgement: The UK/EPSRC financial support under grant no. GR/S95770 is acknowledged.

References:

[1] P. M. Levine and G. W. Roberts, "High-resolution flash time-to-digital conversion and calibration for system-on-chip," *IEE Proceedings on Computers and Digital Techniques*, vol. 152, no. 3, pp. 415-426, 2005.

[2] P. Dudek, S. Szczpanksi, and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," *IEEE Trans. on Solid-State Circuits*, vol. 35, no. 2, pp. 240-247, 2000.

[3] T. Xia and J.-C. Lo, "Time-to-Voltage Converter for On-Chip Jitter Measurement," *IEEE Trans. on Instrumentation and Measurement*, vol. 52, no. 6, pp. 1738-1748, 2003.

[4] C.-C. Chen, P. Chen, C.-S. Hwang, and W. Chang, "A Precise Cyclic CMOS Time-to-Digital Converter with Low Thermal Sensitivity," *IEEE Trans. on Nuclear Science*, vol. 52, no. 4, pp. 834-838, 2005.

[5] M. Collins, B. M. Al-Hashimi, and N. Ross, "A Programmable Time Measurement Architecture for Embedded Memory Characterization," *Proceedings of the 10th IEEE European Test Symposium (ETS'05)*, pp. 128-133, 2005.

[6] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*: John Wiley & Sons, 1997, ISBN: 0-471-14448-7.

Authors' Affiliations:

M. Collins, B. M. Al-Hashimi and P. R. Wilson (School of Electronics and Computer Science, University of Southampton, Highfield, Southampton, S017 1BJ, United Kingdom)

Figures and Tables:

Table 1 Recent work on Time Measurement

Timing Measurement Architecture	Timing Resolution
Flash [1]	5ps
Vernier delay line [2]	5ps
Time-to-Voltage Conversion [3]	14ps
Pulse Shrinking [4]	57.3ps
Programmable Time-to-Voltage Conversion [5]	103ps

Fig. 1 Proposed Time Measurement Architecture (TMA)

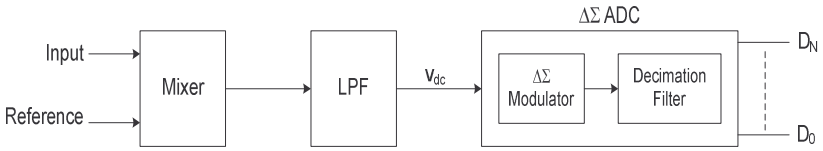

Fig. 2 Cascode Mixer

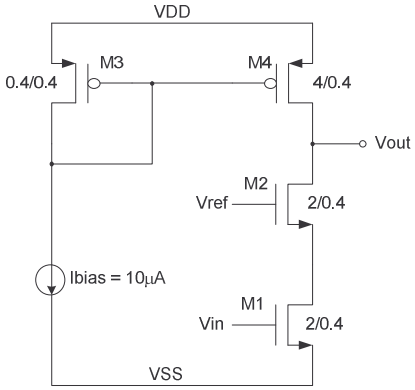

Fig. 3 1st order switched-capacitor ΔΣ modulator

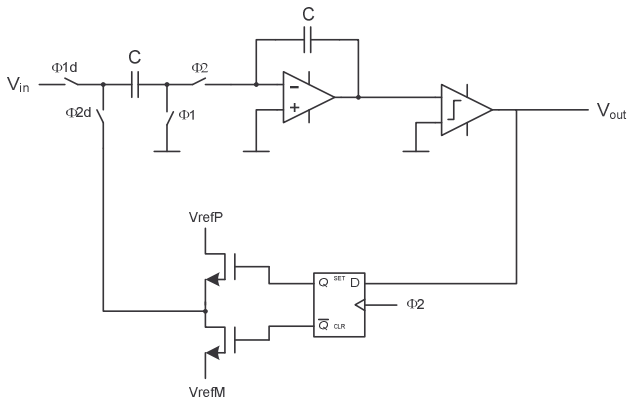

Fig. 4 Folded cascode operational amplifier

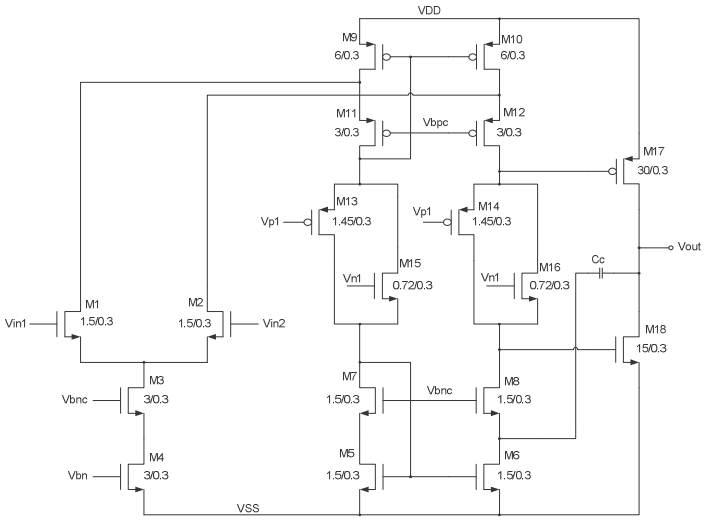

Fig. 5 Simulated relationship between timing resolution and LPF output

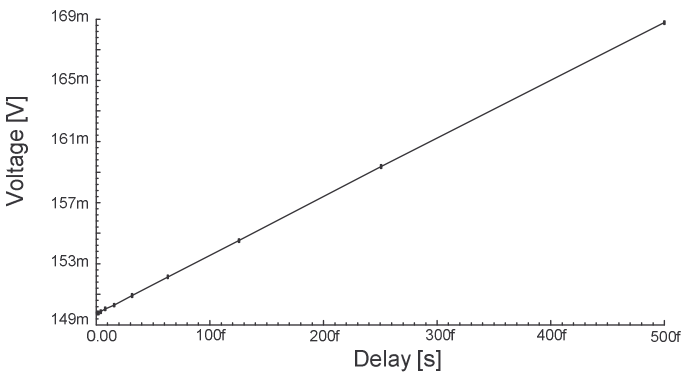

Fig. 6 Input and output waveforms of the proposed architecture