

Dynamic Voltage Scaling Aware Delay Fault Testing

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Abstract

The application of Dynamic Voltage Scaling (DVS) to reduce energy consumption may have a detrimental impact on the quality of manufacturing tests employed to detect permanent faults. This paper analyses the influence of different voltage/frequency settings on fault detection within a DVS application. In particular, the effect of supply voltage on different types of delay faults is considered. This paper presents a study of these problems with simulation results. We have demonstrated that the test application time increases as we reduce the test voltage. We have also shown that for newer technologies we do not have to go to very low voltage levels for delay fault testing. We conclude that it is necessary to test at more than one operating voltage and that the lowest operating voltage does not necessarily give the best fault cover.

1. Introduction

Power management of Systems on Chip has attracted a large body of research; among the most promising power management policies is dynamic voltage scaling (DVS). DVS exploits the fact that the clock frequency of a processor changes proportionally with the supply voltage, while the dynamic energy is proportional to the *square* of the processor's supply voltage. Running the processor at a slower speed means that the supply voltage can be lowered, yielding a quadratic reduction in the energy consumption at the expense of increased execution time. Therefore, designers can adapt the processor voltage /frequency (V/F) setting according to the requirements (often processors run faster than needed) and exploit the energy/speed trade-off. As an efficient energy reduction technique, DVS has been implemented in several contemporary embedded microprocessors such as Intel XScale [1] and Transmeta Crusoe [2], and in ARM's IEM [3] with different (V/F) settings.

During normal operation, a DVS-enabled system can run at several different V/F settings; it is therefore

necessary to ensure that the system will function correctly at each possible V/F setting. Research on very low voltage (VLV) testing [4] has shown that while some faults cannot be observed at the nominal power supply voltage, they become apparent at different operating conditions, such as lower supply voltage. This means that traditional test methodologies, assuming a fixed/nominal power supply voltage and clock frequency, may not guarantee fault-free operation for DVS-enabled systems.

2. Delay Fault Testing For DVS Systems

With decreasing feature sizes of VLSI circuits, manufacturing tests based on the stuck-at fault model are becoming less effective in detecting defects which are typically resistive opens and shorts. To achieve low defect rates, tests for delay faults are becoming essential.

Moreover, delay fault testing is significant in DVS systems because DVS adjusts the voltage and hence the frequency to exploit the slack time. The effect of a change in power supply on delay faults has been reported previously [5-7], but in these cases the voltage is changed for testing purposes, not for normal operation, as with DVS.

Chang and McCluskey reported, [5], that delay faults may not cause the circuit to malfunction under normal operating conditions. If, however, the supply voltage changes during operation, delay faults may cause problems and may result in unexpected behaviour of the circuit. The work was done for circuits that normally operate at a single voltage. In the case of DVS, there is more than one operating voltage and the significance of delay faults is potentially greater.

Experimental results in [7] show the significant effect of operating conditions and process variations on circuit delays. The variation of gate delay propagation with power supply for non-voltage-compensated circuits was demonstrated experimentally. A more recent study, [6], reported that the electrical performance is affected by environmental and physical factors, of which the power supply is one of the more

critical. Other related work on delay fault testing has shown that the most critical path for the circuit varies with voltage [8,9]. For a given voltage there is an optimal test set. As far as we know no one has studied whether the overall fault coverage can be improved by testing the circuit at multiple voltages.

2.1 Very Low Voltage Testing

Yuyun [10] and Chang [5] argued that VLV testing increases the fault coverage in CMOS pass-transistor logic. By reducing the power supply to slightly above twice the threshold voltage, the fault coverage can be increased. The disadvantages of reducing the supply voltage to these theoretical limits are that the noise margin will be reduced and the circuit delay will be increased. Chang has suggested that best trade-off between fault coverage and supply voltage is to run the test at between $2 \times V_{th}$ and $2.5 \times V_{th}$. Both papers on delay faults using VLV [5, 10] looked at non-operational delay faults – timing failures that occur when the delay is different from the designed delay but only at voltages other than those at which the circuit is designed to work. On the other hand, we are looking at operational delays, i.e. delay faults that will not give the expected output at the expected time.

The other main disadvantage of reducing the supply voltage is performance degradation [4], resulting in an increase in test application time. As the voltage is reduced, the operating frequency decreases, and hence the number of test vectors that can be applied in a given time will reduce. The scan speed is limited by three factors: the tester capability; power during scan; and the scan chain capability. With reduced supply voltage, the scan chain capability will be reduced.

To illustrate this, we have interpreted some published results for the Transmeta Crusoe 5600 processor [11]. Equation (1) gives the operating frequency.

$$f = (L_d K_6)^{-1} ((1 + K_1)V_{dd} + K_2V_{bs} - V_{th1})^\alpha \quad (1)$$

Using the constants for 0.18 μ m CMOS given in [11], the relation between the circuit supply voltage and frequency was derived. The bulk-source voltage V_{bs} , is set to zero since we are not considering the effect of body biasing in our analysis. The value of the threshold voltage, V_{th1} given as 0.359V. The normal processor operating voltage is between 1.2 to 1.6V. Figure 1 shows the relation between the supply voltage and normalised frequency. At 1.2V, the operating frequency is 70% of that at 1.6V. Tests at

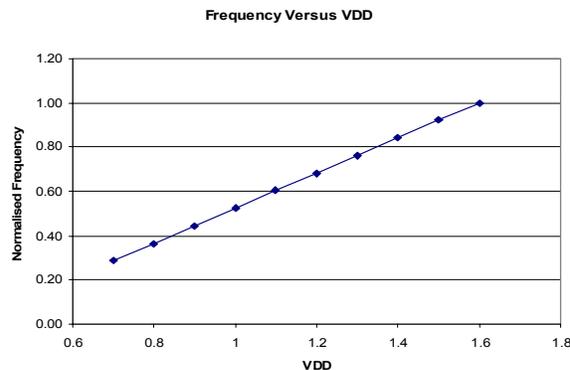


Figure 1 Supply Voltage versus frequency for Transmeta Crusoe 5600 Processor

this voltage would result in the test application time increasing by 1.4 times compared to the time taken at the highest operating voltage.

It has also been reported, [4], that VLV testing results in coverage loss. In other words, a particular range of resistive fault values is detectable at the one voltage, but not at a lower voltage. The study in [4] looked at resistive bridging faults that cause stuck faults. There have been more recent studies showing how bridging faults can cause timing failures [12, 13]. It is reported in [12] that the delay caused by bridge resistance can either increase or decrease depending on the input patterns. This claim is further supported by [16] where a basic fault coverage analysis has been done on for a CMOS bridging fault at different power supplies. The study shows that by reducing the supply voltage, the fault coverage for resistive bridging faults can be increased. However [17] has shown some examples of undetectable faults at lower supply voltages even though they are detected at a higher supply voltage.

Figure 3 shows the effects of different resistive values under different voltages. The simulations used a simple resistive short circuit, as in Figure 2, to represent a bridging fault. The outputs of five different values of resistors are shown in the waveforms. The inputs to the NAND gate are [0,0]. The maximum resistor value that is manifested as a stuck-at-fault decreases as the voltage increases. (10k Ω at 2.0V; 5k Ω at 3.3 V). Figure 3 also shows a significant increase in delay as we decrease the supply voltage.

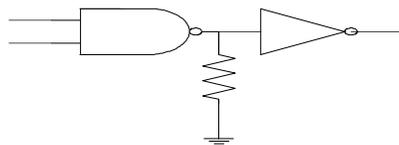


Figure 2 Simulation Circuit.

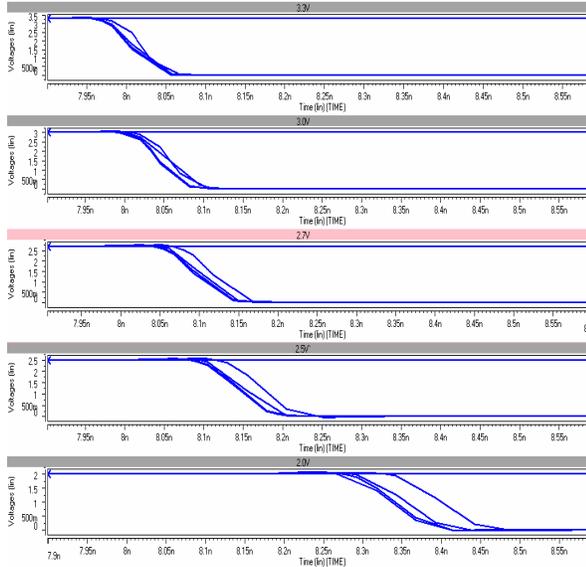


Figure 3 Change in delay for different resistive values for different power supply voltages.

3. Delay flaws

We have studied two defects that can cause timing failures. These are transmission gate opens and resistive opens. Due to space limitations we do not include the detailed results of the bridging fault study. We have chosen these defects since both will cause increases in propagation delays. It is important to note that certain faults such as NMOS gate-to-source shorts and NMOS gate-to-drain shorts will cause reductions in delay values. Transmission gate opens were thoroughly studied in [5] using 0.8 and 0.6 μm technology. In order to determine whether the fault effects become more significant with changing feature sizes, we have revisited the examples using 0.35 μm technology and voltage steps from an actual DVS processor. The voltage steps are 3.3, 3.0, 2.7, 2.5 and 2.0 Volts. These voltage ranges are consistent with the voltage range of StrongArm SA1100 DVS processors [14].

3.1 Transmission Gate Opens

Transmission gate opens were simulated using a similar setup to that in [5]. The circuit is part of a multiplier consisting of 4 levels of carry-save adders. The circuit uses two different pass transistor logic implementations for full adder cells. Figure 4 shows the interconnections between the adder's cells. Each adder has five transmission gates. If one of the transistors, either PMOS or NMOS, is stuck open, the output will be degraded. A degraded signal is defined as one in which V_{IH} is lower than the supply voltage

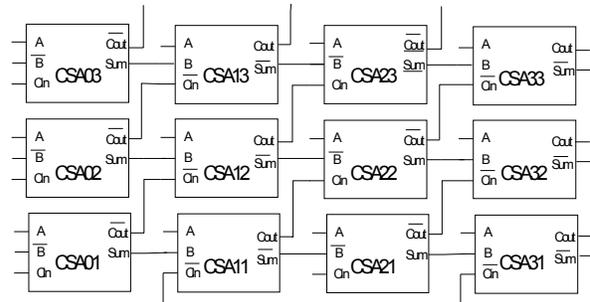


Figure 4 Interconnection between adder cells for simulation setup [4].

or V_{IL} is higher than the ground signal. Faults were injected at two different locations. Both of the faults are NMOS opens. For the 0.35 μm technology, $|V_{tp}|$ is higher than V_{tn} . This will result in NMOS transistors having a higher driving strength and an open in an NMOS gate will create a longer delay than an open in a PMOS gate. The first fault is an NMOS open at the output transmission gate of CSA11. This open will cause a degraded signal to be passed to input B of CSA21. The second fault is an open at the output transmission gate of CSA22. The resulting degraded signal will be fed to input B of CSA32. The signal paths for the faults are shown in Table 1. The faults were injected in two different types of cell to show how the supply voltages affect different fault locations. Inverters were used as buffers at all inputs and outputs of the circuit under test.

Table 1 Signal propagating path

	Fault Site	Signal Propagating Path
A	CSA11 NMOS Open	CSA01(A)-CSA11(B)-CSA21 (B)-CSA32(Cin) CSA32(Cout)
B	CSA22 NMOS Open	CSA01(A)-CSA11(B)-CSA22 (Cin)-CSA32(B)-CSA32(Cout)

3.1.1 Simulation Results

Figure 5 shows how the path delay changes for the fault-free and transmission gate fault cases, with varying supply voltage. In all three examples, the fault-free case is shown as a solid trace, while the faulty delay is shown dashed. It can be seen that the delay increases as the supply voltage falls, until at 2.5V, the fault behaves as a stuck fault, after the initial transient.

Table 2 shows the path delay ratio and gate delay ratios between the faulty circuits and the fault free circuit. The path delay ratio is measured as the ratio of the signal propagating path of the faulty circuit to the same path of the fault free circuit. The gate delay ratio is the ratio between the delay of the faulty adder cell

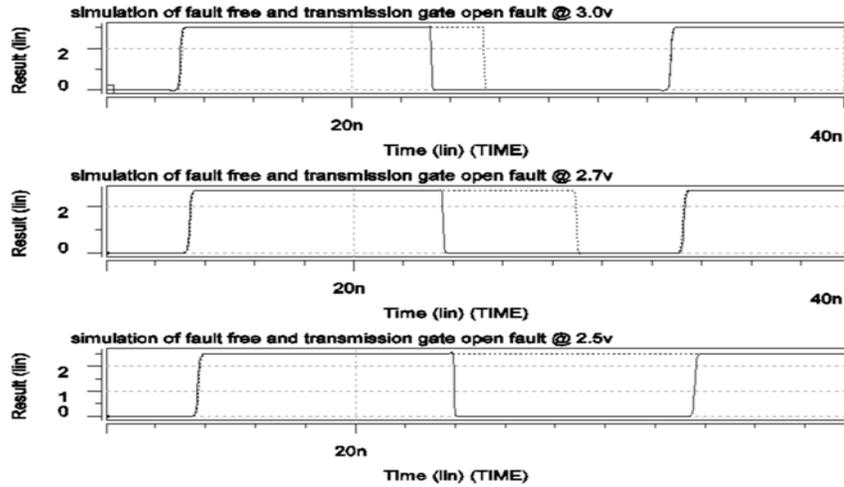


Figure 5 Changes in delays for fault free and transmission gate open fault at different supply voltages

and the fault free adder cell. The entries in Table 2 shown as “SF” mean the fault causes the circuit to show a stuck-at-fault error. In [5] Chang reported that the stuck fault happens at lower voltages for larger geometry process. Our results shows similar patterns with the delay faults manifesting themselves as stuck at fault at higher voltage. As expected, both the gate delay ratio and the path delay ratio increase as we reduce the voltage. Another important point to note is that for the path delay ratio, the highest voltage shows a minimum ratio of 36%. With the increasing accuracy of the ATE, these delay faults can be captured even at much higher voltages

Table 2 Path Delay Ratio and Gate Delay Ratio for Faults A and B

Vdd	Fault A		Fault B	
	Path Delay Ratio	Gate Delay Ratio	Path Delay Ratio	Gate Delay Ratio
3.3	1.36	1.02	1.43	1.05
3.0	1.56	1.05	1.68	1.10
2.7	2.27	1.12	2.51	1.19
2.5	SF	SF	SF	SF
2.0	SF	SF	SF	SF

3.2 Resistive Open Defects

A resistive open defect can be modelled as a resistance between two nodes. This is depicted in Figure 6. Previous research, [15], categorises open faults into strong-opens ($>10M\Omega$) and weak opens ($\leq 10M\Omega$). Strong-opens will cause stuck-at faults and

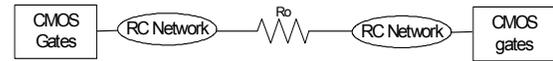


Figure 6 Resistive open fault model

can be detected using standard stuck-at patterns. Weak opens are difficult to detect because they have timing-dependent effects. This implies that the test results change with test speed. We have used 2 different circuits to evaluate the effect of the power supply on gate and path delay ratios for circuits with weak opens.

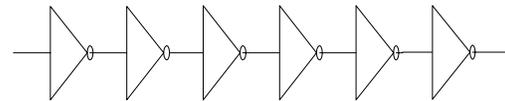


Figure 7 Buffer chain of 6 inverters

A buffer chain of 6 inverters, as shown in Figure 7, was simulated to characterise the behaviour of a circuit with weak resistive opens. The resistor open defects were injected between the second and third inverters. The path delay was measured between the input of the second inverter and output of the fifth inverter and the gate delay was measured between the same input and the output of third inverter. Table 3 and 4 list the delay ratios for the circuit. To observe the impact of resistive opens in a more complex circuit, weak resistive faults were injected into the circuit of Figure 4. The resistive open defects were injected at 2 locations in the multiplier cell. The first location (A) is between CSA22 and CSA 32. The second location (B) is between CSA11 and CSA21. Tables 5 and 6 list the delay ratios.

Table 3 Path Delay Ratio for Buffer Chain

Vdd	Ro=500Ω	Ro=10kΩ	Ro=25kΩ	Ro=250kΩ	Ro=1MΩ
3.30	1.01	1.09	1.20	3.20	9.25
3.00	1.00	1.07	1.18	3.04	8.50
2.70	1.00	1.06	1.16	2.75	7.65
2.50	1.00	1.06	1.16	2.70	7.22
2.00	1.00	1.05	1.13	2.25	5.59

Table 4 Gate Delay Ratio for Buffer Chain

Vdd	Ro=500Ω	Ro=10kΩ	Ro=25kΩ	Ro=250kΩ	Ro=1MΩ
3.30	1.01	1.15	1.40	5.38	17.46
3.00	1.01	1.15	1.36	5.01	16.01
2.70	1.01	1.11	1.32	4.48	14.20
2.50	1.01	1.11	1.32	4.36	13.36
2.00	1.00	1.09	1.24	3.38	9.91

Table 5 Path Delay Ratio for multiplier circuit for resistive open faults

Vdd	Ro=25kΩ		Ro=250kΩ		Ro=1MΩ	
	FAULT LOCATION					
	A	B	A	B	A	B
3.30	1.02	1.02	1.18	1.13	1.67	1.48
3.00	1.01	1.02	1.17	1.12	1.61	1.44
2.70	1.01	1.02	1.15	1.11	1.56	1.39
2.50	1.01	1.01	1.12	1.10	1.50	1.36
2.00	1.01	1.01	1.11	1.07	1.38	1.26

Table 6 Gate Delay Ratio for multiplier circuit for resistive open faults

Vdd	Ro=25kΩ		Ro=250kΩ		Ro=1MΩ	
	FAULT LOCATION					
	A	B	A	B	A	B
3.30	1.00	1.01	1.32	1.16	2.05	1.55
3.00	1.00	1.02	1.30	1.15	1.97	1.54
2.70	1.00	1.01	1.29	1.15	1.95	1.51
2.50	1.00	1.01	1.28	1.15	1.86	1.50
2.00	1.00	1.01	1.25	1.12	1.74	1.41

3.2.1 Simulation results

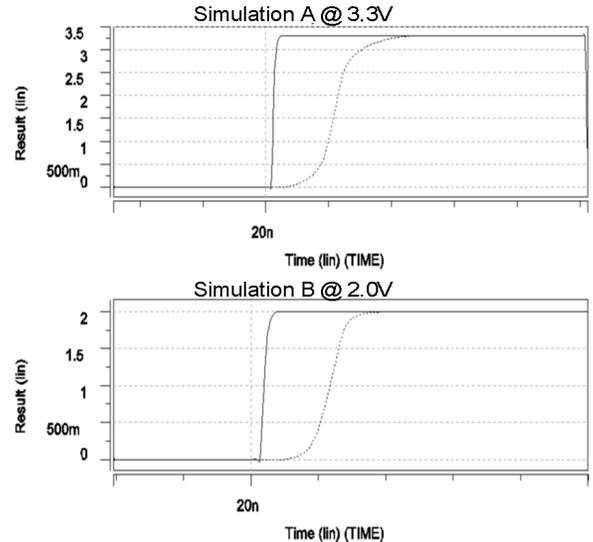
Figure 8 shows the circuit waveforms for the inverter chain under fault-free conditions (solid) and with the resistive open fault inserted (dashed), at two supply voltages. In both cases, the waveform is observed one inverter after the fault site. It can be seen that as the supply voltage falls, the *absolute* delay increases for both the fault-free and faulty cases.

However, the *relative* delay for the faulty cases *decreases* compared with the fault-free delay.

From Tables 3 and 4, it can be seen that the reduction of the delay ratios with decreasing voltage for both path and gate delays is significant. The delay ratio pattern is inverse to that for transmission gate open faults. As we reduce the supply voltage, the time taken for gate signals to settle grows. This is true for both faulty and fault free circuits. Note however, that the delay in the faulty circuit does not change proportionally to that in the fault free circuit.

Table 7 shows the absolute delay of the circuit for the fault free case and for a resistive open fault of 1MΩ. The delay almost doubles (1.83) when the supply voltage is reduced from 3.3V to 2.0V for fault free circuit. For the faulty circuit the increase in delay is only 1.04 times.

For small resistive open fault values, the increase in delay due to the fault is not significant at both ends of the voltage range. However, as the resistor value increases, the impact of the voltage reduction is marked. For the more complex circuit, the impact of the resistance is not as significant as in the smaller circuit. This is because the delayed signals get restored at the next adder cell.

**Figure 8 Fault-free (solid) and resistive open delays (dashed) at 3.3V and 2.0V.**

The statistical distribution of resistive open faults of 1MΩ to 10MΩ is similar to that in the range of 100kΩ to 1MΩ [15]. The probability of having a resistive open of 1MΩ and above is as high as having a lower value of resistance. In this scenario it is better to run the test at the highest voltage since not only will a

fault give a larger delay ratio, the test application time will be significantly reduced, as illustrated by Figure 1.

Table 7 Absolute gate delays for faulty and fault free circuit

Vdd	Gate delay for fault free circuit	Gate Delay for resistive open of 1M Ω
3.3	1.19E-10	2.07E-09
2.0	2.18E-10	2.16E-09

4 Conclusions

This paper presents a first approach to a testing strategy for delay faults in Dynamic Voltage Scaling systems. Our study shows that we do not need to use the lowest operating voltages to detect certain types of faults. From the transmission gate open simulation it is evident that low to mid-range voltages give sufficient fault coverage. In general testing at lower operating voltages is only required for certain types of faults such as transmission gate opens and bridging faults. On the other hand, weak resistive opens that cause delay faults are best tested at higher operating voltages. Simulation results both of a simple inverter chain circuit and a more complicated multiplier circuits support our conclusions. The overall conclusion is that in order to guarantee the quality of DVS systems, it will be necessary to select a number of voltage-specific delay fault tests, in addition to voltage-independent stuck-fault tests. Initial testing can be done at the highest operating voltage and this will reduce the time and cost of the test. The escaped defects can be detected at lower mid-range voltages without the need to go to the lowest voltages. Future work will aim to find an optimal set of voltage/fault test pairs.

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