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The vertical metal insulator semiconductor tunnel transistor: A proposed Fowler–Nordheim tunneling device

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Abstract

We propose a new field-effect transistor, the vertical metal insulator semiconductor tunnel transistor (VMISTT) which operates using gate modulation of the Fowler–Nordheim tunneling current through a metal insulator semiconductor (M-I-S) diode. The VMISTT has significant advantages over the metal-oxide-semiconductor field-effect transistor in device scaling. In order to allow room-temperature operation of the VMISTT, the tunnel oxide has to be optimized for the metal-to-insulator barrier height and the current–voltage characteristics. We have grown TiO₂ layers as the tunnel insulator by oxidizing 7 and 10 nm thick Ti metal films vacuum-evaporated on silicon substrates, and characterized the films by current–voltage and capacitance–voltage techniques. The quality of the oxide films showed variations, depending on the oxidation temperatures in the range of 450–550 °C. Fowler–Nordheim tunneling was observed at low temperatures at bias voltage of 2 V and above and a barrier height of approximately 0.4 eV was calculated. Leakage currents present were due Schottky-barrier emission at room-temperature, and hopping at liquid nitrogen temperature.

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1. Introduction

Progress in integrated circuit (IC) technology has been achieved by reduction in the total area

of individual transistors, resulting in an increase of speed accompanied by dramatic increase in density of device and interconnect integration. However, the metal-oxide-semiconductor field-effect transistor (MOSFET) has physical limits for size reduction due to short-channel effects [1]. In addition, the random location of dopants within the conducting channel is expected to create

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fluctuations in the threshold voltage of the individual transistors. Another consideration is the detrimental effect of source-drain, junction and gate current leakage on the performance of transistors with increasingly smaller critical dimension [2]. The introduction of metal-oxide high-k gate dielectrics and metal gates renders obsolete one of the key advantages of basic Si technology, namely the thermal growth of silicon dioxide as the gate insulator.

Many new devices that can be scaled significantly further have recently been proposed and fabricated, such as the Schottky-barrier field-effect transistor (SB FET) [3,4], the silicon stacked tunnel transistor [5] and the metal-oxide tunnel transistor (MOTT) [6]. The latter device is based on gate modulation of Fowler–Nordheim (F–N) tunneling [7] between a metal source and drain through an insulating body of approximately 10 nm thickness as shown in Fig. 1. The barrier height of the body oxide should be low enough to allow F–N tunneling and at the same time high enough to prevent thermionic emission. The source and the drain of the device are metallic and no semiconductors or silicide contacts are required in the process. This means that the source and the drain contact areas are minimized and that no short-channel effects exist. High speed operation in the ps range is expected since no minority carriers are involved and transconductance can be of the same order as for MOSFET's (1 mS/ μm). In principle, device fabrication should be considerably cheaper than of a comparable

MOSFET. Furthermore, the transistor is non-crystalline which means that it can be grown on flexible substrates and it is imaginable that three-dimensional circuits can be developed. Excellent operation with five orders of magnitude difference between on and off current has been achieved at 90 K [6,8–10]. Notwithstanding the good initial results, the MOTT has attracted little attention due to a variety of reasons: the room-temperature operation is unconvincing due to thermal leakage over the barrier, the fabrication method of the insulating oxide barrier is not scalable, and no complementary device exists. In this article we propose a MOTT-like device, which alleviates the above problems, and we present initial results on the tunneling current through the insulating body.

2. Theory, device design and simulation of VMISTT

The operation of the vertical metal insulator semiconductor tunneling transistor (VMISTT) is based upon gate modulation of F–N tunneling. Currents due to other mechanisms, such as trap assisted tunneling (TAT) [11], Schottky-barrier emission (SBE), hopping, and Poole–Frenkel (P–F) effect cannot be modulated and represent leakage currents.

The F–N tunneling current density for an applied voltage V is given by [7]

$$J = AV^2 e^{-B/V}, \quad (1)$$

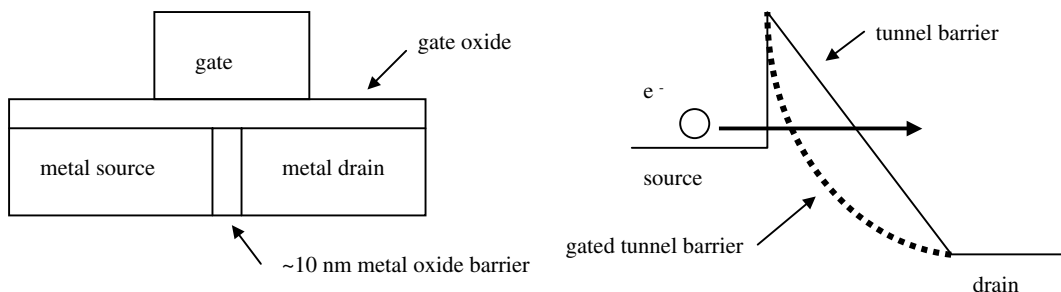


Fig. 1. Schematic and principle of a MOTT: the metal-oxide barrier allows Fowler–Nordheim tunneling when a drain voltage is applied. The source-drain Fowler–Nordheim tunneling current is modulated by the applied gate voltage at the gate oxide interface and a strong tunneling channel opens up.

where A and B are constants given by

$$A = q^2 / (8\pi\hbar d^2 \Phi), \tag{2}$$

$$B = 4\sqrt{2qm^*m_0}\Phi^{3/2}d / (3\hbar). \tag{3}$$

The symbol Φ stands for the metal/oxide barrier height in eV, m^* is the tunneling effective mass of the charge carrier in the barrier material, d is the tunnel barrier width, m_0 is the free electron rest mass, q is the magnitude of electronic charge, and \hbar is the reduced Planck's constant. Hence, the $\ln(J/V^2)$ versus $1/V$ plot is a straight line having a slope of $-B$, and is a characteristic of F–N tunneling current.

The VMISTT as shown in Fig. 2 is different in two important aspects from the MOTT. First, by replacing the source by doped (single or poly crystalline) silicon and choosing an appropriate tunnel barrier and metal drain, it is possible to make both n-type and p-type devices. In order to realize complementary operations in VMISTT it is essential to ensure that carriers tunnel only from the semiconductor to the drain electrode through the oxide channel. That is possible when metals of low (Al = 4.1 eV) and high (Pt = 5.1 eV) work functions are chosen for n- and p-type VMISTT, respectively. The band diagrams in Fig. 3 illustrate the situations. For the p-VMISTT holes tunnel from p-type Si as the tunnel barrier thins at increased negative drain bias. A high work function of the drain metal ensures that the tunnel barrier for electrons from the drain to p-type Si is large which minimizes the electron current. On the other

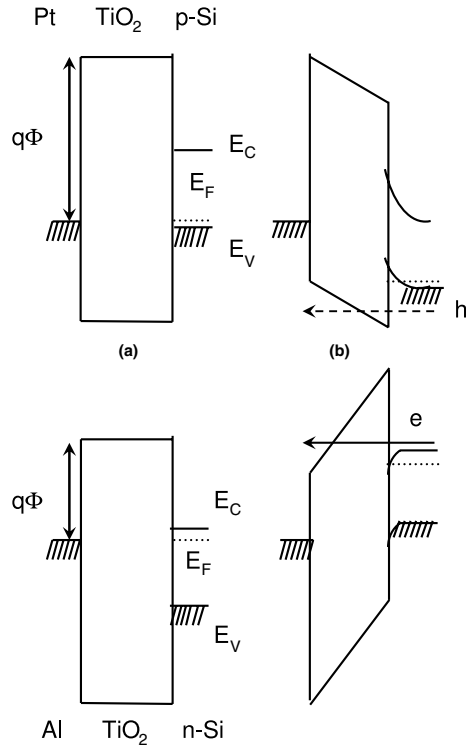


Fig. 3. Schematic energy band diagrams of a Pt/TiO₂/p-Si and an Al/TiO₂/n-Si sample for: (a) zero bias and (b) positive and negative substrate biases. Gate modulation will only enhance the Si to metal tunneling and hence allow complementary operation.

hand, for an n-type VMISTT a low value of the metal work function ensures electron tunneling from n-type Si to drain and suppresses hole current in the opposite direction.

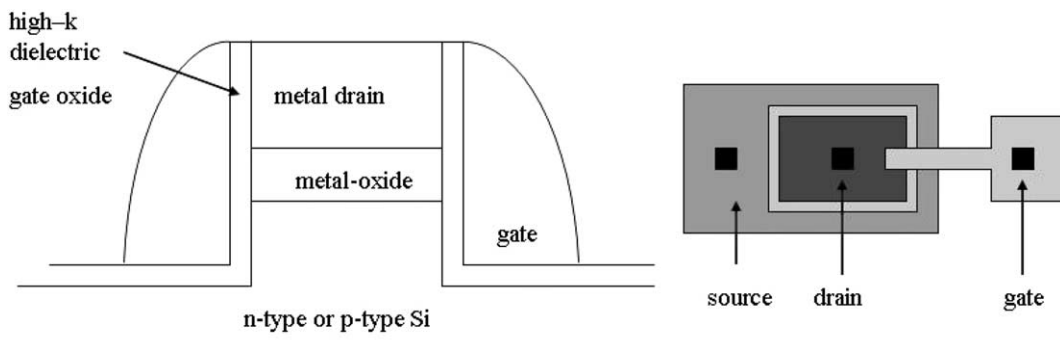


Fig. 2. Cross-sectional and top view of the schematic diagram of the proposed VMISTT.

We have simulated p- and n-type VMISTT operations using the SILVACO device simulator Atlas [12] to show efficient gate control of the proposed devices. Transfer characteristics of the VMISTT structure given in Fig. 4 show the drain current as a function of the gate voltage in the 0 to ± 3 V range. The F–N tunneling material parameters defined in Eq. (2) and (3) are the experimental data obtained in this work for titanium dioxide (TiO_2) as the tunnel oxide, being $A = 2.25 \times 10^{-6} \text{ AV}^{-2} \text{ cm}^{-2}$ and $B = 9.12 \times 10^6 \text{ Vcm}^{-1}$. A drain current swing of over six orders of magnitude is obtained for relatively low bias. The ratio of the dielectric constants of the gate dielectric and the tunnel oxide heavily influences the gate modulation as the gate field can penetrate further in the channel for a high gate dielectric value, in similar fashion as in a MOSFET. The simulation assumed negligible gate leakage which is justified if the gate dielectric energy gap and band off-set are considerably higher than those

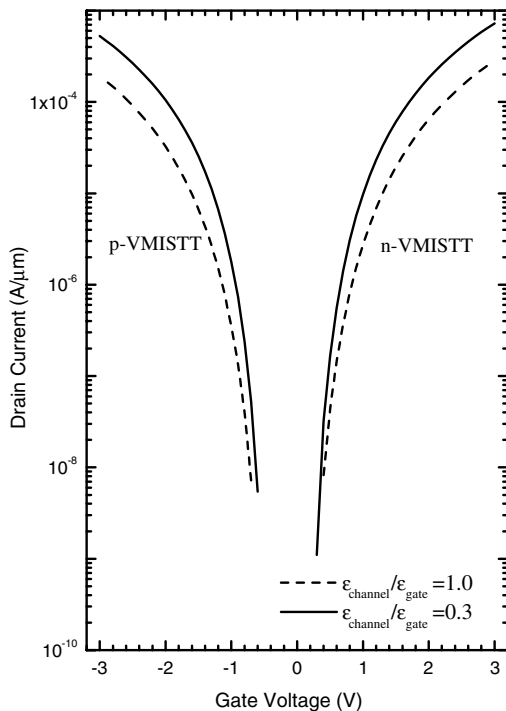


Fig. 4. SILVACO ATLAS device simulation of the transfer characteristic of a p-type and n-type VMISTT using the experimental data for the Fowler–Nordheim tunneling.

of the tunnel oxide. The device will hence only operate with a low bandgap tunnel oxide which additionally ensures low operational voltages. The off-state of the device will be dominated by the leakage currents mentioned before.

The second advantage of the VMISTT is the vertical lay-out, which allows the metallic oxide to be grown by controllable, scalable methods, such as evaporation or sputtering of a metal followed by thermal or plasma oxidation. This will lead to a much better controlled oxide layer and hence a strongly reduced leakage current as compared to the lateral MOTT. The surrounding gate structure will allow more efficient gate control than its single-gate counterparts. Subsequent processing can continue along the same lines as those for vertical MOSFETs, with the gate oxide replaced by a high-k dielectric [13–15].

TiO_2 has been used in MOTTs and is expected to be an excellent choice for the VMISTT as well, since its band off-set is around 1 eV for both electrons in the conduction band and holes in the valence band. In the present work, we chose TiO_2 as the tunnel dielectric, and optimized its growth conditions on p-type silicon (Si) as the first step towards making a VMISTT operable at room temperatures. TiO_2 has been grown by a number of techniques, like metal organic chemical vapour deposition (MOCVD) [16], sputtering [17], anodic oxidation [9], plasma oxidation of metallic Ti films [18]. As exact control of the barrier height is of paramount importance to control the tunneling current only the latter method of plasma oxidation or thermal oxidation of the metallic constituent are expected to give the required wetting and minimal surface roughness to make reproducible tunnel devices [19]. The temperature and the oxygen pressure are the prime parameters for oxidation. Oxygen deficiencies are expected in titanium oxide [20], whereas the crystallinity or lack of it will influence the currents strongly. The amorphous to crystalline phase transition is reported to be at 360 °C [21], but likely depends on the exact circumstances. The improvements in oxide properties grown at a higher temperature are often counter-balanced by an increased thermal budget and the growth of a SiO_2 layer at the TiO_2/Si interface [22,23].

This is undesirable for efficient tunneling, although a thin SiO_2 layer may be tolerated. Post oxidation anneals in oxygen or forming gas might be beneficial as well. Unlike CVD methods or sputtering of TiO_2 , the optimum oxidation conditions strongly depend on the thickness of the metallic film, and analysis of thick films bear little resemblance to the thin metal-oxides.

3. Experimental

Titanium (Ti) layers of thickness of 7 and 10 nm were deposited on RCA-cleaned and HF-treated 4 in. diameter, low-resistivity (0.01–0.02 Ωcm) p-type Si substrates by vacuum e-beam evaporation without any substrate heating. The oxide was subsequently formed by thermal oxidation at 450, 500, and 550 $^\circ\text{C}$ for 30 min. Subsequently, front contacts using shadow masks and back contacts were formed by vacuum evaporation of 1 μm thick aluminium (Al) layers. The high Si doping ensured that the back contacts were ohmic. The area of the top contact pads used in most of the measure-

ments was $270 \times 271 \mu\text{m}^2$. Ellipsometry was performed using laser light at 632.8 nm for a fixed angle of incidence of 70° to check the thicknesses of the oxide layers. Cross-sectional scanning electron microscopy (SEM) was done using a Hitachi S-4800 microscope to visualize the oxide layers grown. These confirm that the thickness of the oxidized Ti is approximately equal to the nominal thickness for TiO_2 , being 1.8 times the metallic Ti thickness. The latter values have been used in the calculations (see Figs. 5).

Current–voltage characteristics were obtained at room temperature and low temperatures using the HP4155A parametric analyzer. The bias was applied to the p-type substrate of the wafers while the top Al contact was kept at the ground potential. Positive and negative bias sweeps were started from zero. The low temperature measurements were done by mounting the samples on a liquid nitrogen cryostat, controlled by the BioRad DL4960 temperature controller. Capacitance–voltage characterization was done at room temperature at 1 MHz using the HP4280A C-meter and at variable frequency using a HP4192A impedance analyzer. The bias was either ramped from

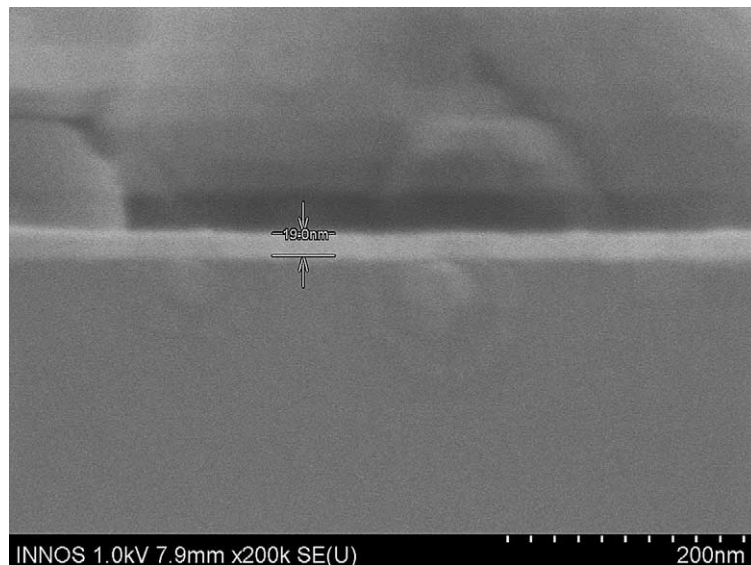


Fig. 5. Cross-sectional field emission SEM micrograph of the TiO_2 layer. The silicon substrate is below the oxide layer, which appears as a bright band.

inversion, or ramped from zero bias without noticeable difference.

4. Results and discussion

We analyzed the $I-V$ and $C-V$ data to assess the thicknesses and dielectric constants of the layers, and identify the active carrier transport mechanisms in order to maximize the F-N tunneling for VMISTT. The $I-V$ characteristics of the TiO_2 samples are shown in Figs. 6 and 7. It is clear from these figures that increased oxidation temperature results in a smaller current, although the difference between 500 and 550 °C is relatively small for the 10 nm Ti film. Reduction of leakage currents is expected with films closer to TiO_2 stoichiometry but formation of a SiO_2 interfacial layer will also reduce the current. However, a large (more than 1 nm) SiO_2 interfa-

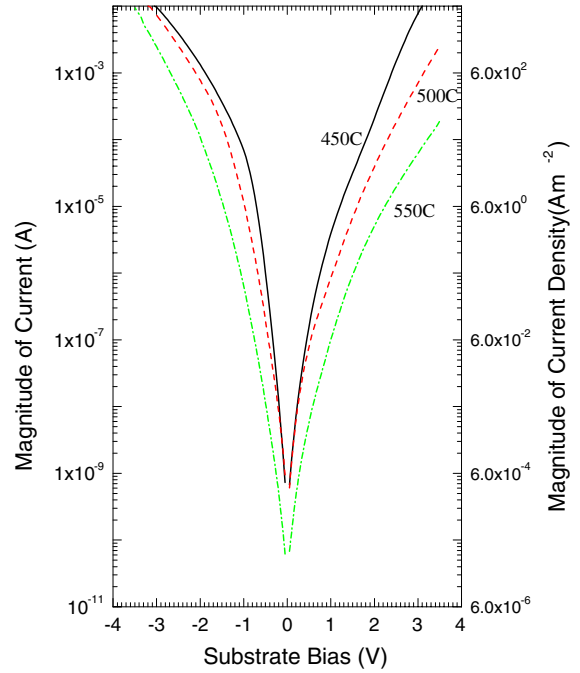


Fig. 7. $I-V$ characteristics of 12 nm TiO_2 films oxidized at three different temperatures. The current reduces strongly with increasing temperature.

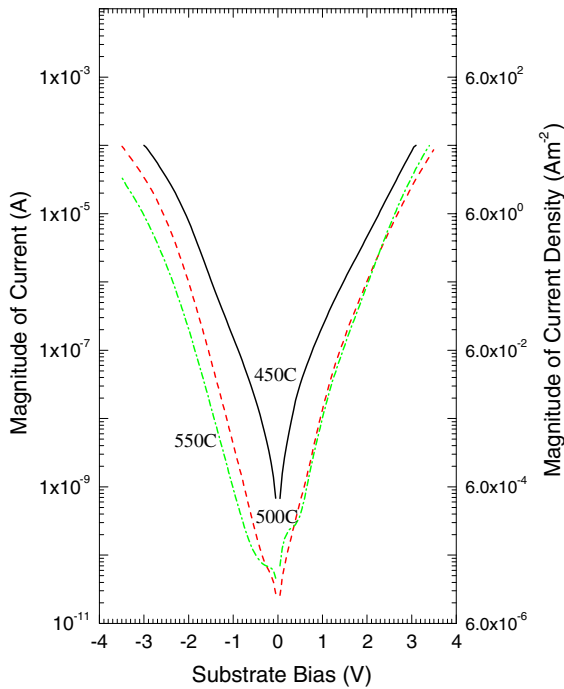


Fig. 6. $I-V$ characteristics of 18 nm TiO_2 films oxidized at three different temperatures. The current reduces strongly with increasing temperature from 450 to 500 °C. Both positive bias and negative bias give similar levels of current.

cial layer is unlikely as a TiO_2/SiO_2 double barrier structure is expected to show much stronger asymmetry between the positive and negative bias curves [24].

The results of $C-V$ measurements are shown in Figs. 8 and 9. All curves show a lack of saturation in accumulation. This is due to the very thin oxide and high dielectric constant of the oxide which makes the (quantum) width of the accumulation layer of importance [25,26]. Table 1 shows the accumulation capacitance and calculated dielectric constant assuming the nominal oxide thickness. The dielectric values of just below 30 are in good agreement with the TiO_2 films deposited by chemical vapour deposition by Campbell et al. [25]. The decreasing accumulation capacitance and dielectric constant with increasing oxidation temperature suggests an increase the interfacial oxide thickness [22,23].

Fig. 10 shows the $\ln(I/V^2)$ versus $1/V$ F-N plot for a 18 nm TiO_2 layer at 84 and 300 K for positive and negative substrate bias. The linear segment of

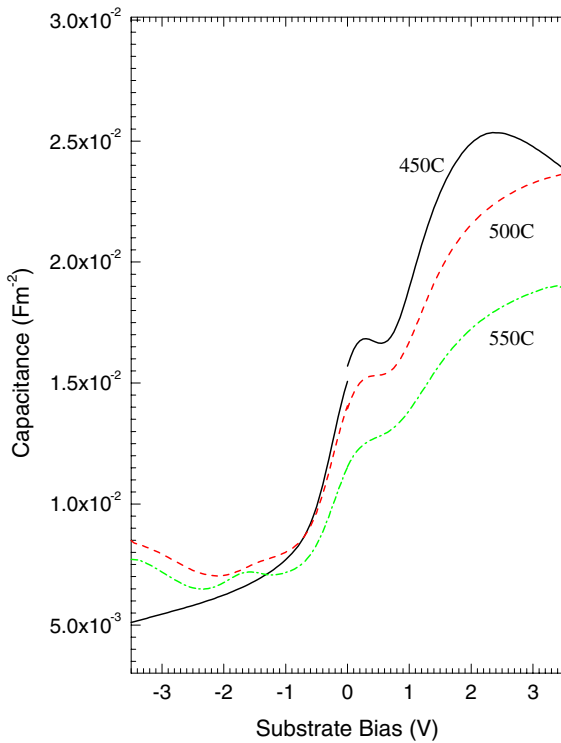


Fig. 8. C – V characteristics of the 18 nm TiO_2 layers grown. Decrease of capacitance with oxidation temperature is consistent with increasing interfacial oxide with higher oxidation temperature.

the low temperature curves in the 2–3 V positive bias range corresponds to F–N tunneling and the Al/ TiO_2 barrier height obtained from Eq. (1) is 0.3–0.4 eV, which is in good agreement with published data [16]. As shown in Table 2, The F–N plots for the 12 nm films and the films oxidized at 450 and 500 °C yield a nominal barrier height of 0.3–0.4 eV as well. For negative bias, although the general features are similar to those for positive bias, the F–N tunneling starts at a slightly lower value due to the small difference in band alignment between the Al metal and the silicon conduction band.

The flat line in the I/V^2 versus $1/V$ low temperature curve at lower bias corresponds to a linear I – V curve as shown more clearly in Fig. 11. Ohmic conduction or hopping is hence the only leakage mechanism at low temperatures. At room temperature an extra current mechanism turns up in the

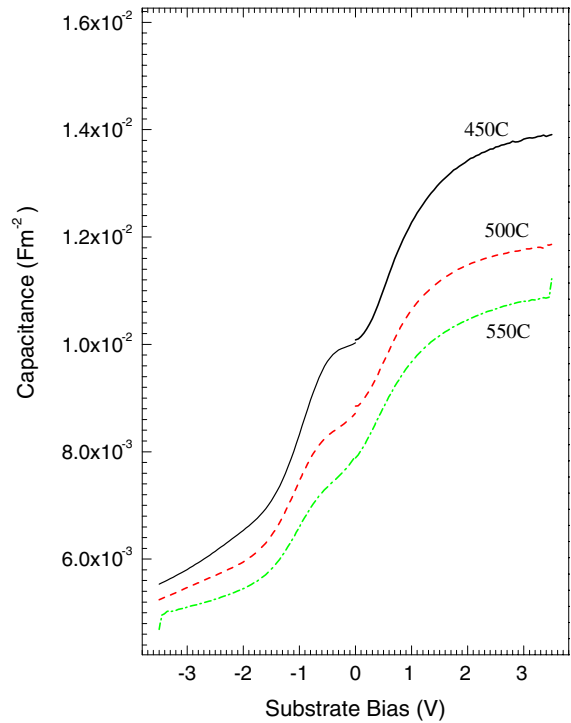


Fig. 9. C – V characteristics of the 12 nm TiO_2 layers grown. The curve for the film oxidized at 450 °C shows anomalies at high voltage due to the large current through the oxide.

Table 1

Accumulation capacitance at 3 V for all TiO_2 layers

Ti (nm)	Oxidation (C)	TiO_2 (nm)	C_{max} (Fm^{-2})	ϵ_s
7	450	12.5	2.55×10^{-2}	35.9
	500		2.36×10^{-2}	33.2
	550		1.90×10^{-2}	26.8
10	450	17.8	1.40×10^{-2}	28.2
	500		1.19×10^{-2}	23.8
	550		1.09×10^{-2}	21.9

The dielectric constant was calculated using the nominal thickness of the TiO_2 layers, being 18 and 12 nm TiO_2 for 10 and 7 nm Ti layer, respectively.

intermediate voltage range. Schottky barrier emission current is given by [1]

$$I = A^{**} T^2 e^{-q\Phi/(kT)} e^{q\sqrt{qV/(4\pi\epsilon_{\text{ox}}d_{\text{ox}})}/(kT)}, \quad (4)$$

where A^{**} is the Richardson’s constant, $q\Phi$ is the barrier energy, $\epsilon_{\text{ox}} = \kappa_{\text{ox}}\epsilon_0$, V is the applied bias and the other symbols have their usual significance.

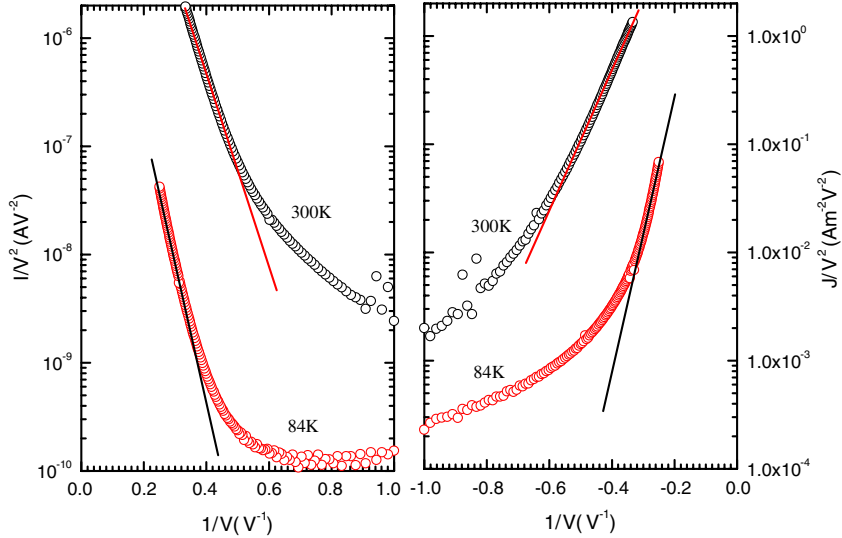


Fig. 10. Fowler–Nordheim plots for the 18 nm TiO₂ layer oxidized at 550 °C for 300 and 84 K. The parameters for straight line fits to equation (1) at 84 K are tabulated in Table 2.

Table 2
Fowler–Nordheim barrier height as derived from the slope of the F–N plots at 84 K

Ti (nm)	Oxidation (C)	TiO ₂ (nm)	F–N slope (V)	ϕ (eV)
7	450	12.5	15.48	0.32
	500		13.81	0.30
	550		–	–
10	450	17.8	26.51	0.36
	500		37.63	0.46
	550		30.83	0.40

Fig. 12 shows the $\ln(I)$ versus \sqrt{V} Schottky plot for the 18 nm TiO₂ layer at 300 K. The fit to equation (4) shows excellent agreement over a very large current range. The nature of I – V curves in Fig. 10 can hence be explained by invoking these three mechanisms. The same mechanisms have been used by Campbell et al. [16] for a TiO₂ deposited by chemical vapour deposition. Even though these authors use a Pt electrode with a higher work function and with hole tunneling as the main current for negative gate voltage, the curves are very similar. The biggest difference is that in our film the F–N tunneling starts at 2 V as compared to more than 3 V in their devices. The most likely reason for this discrepancy is that our interfacial

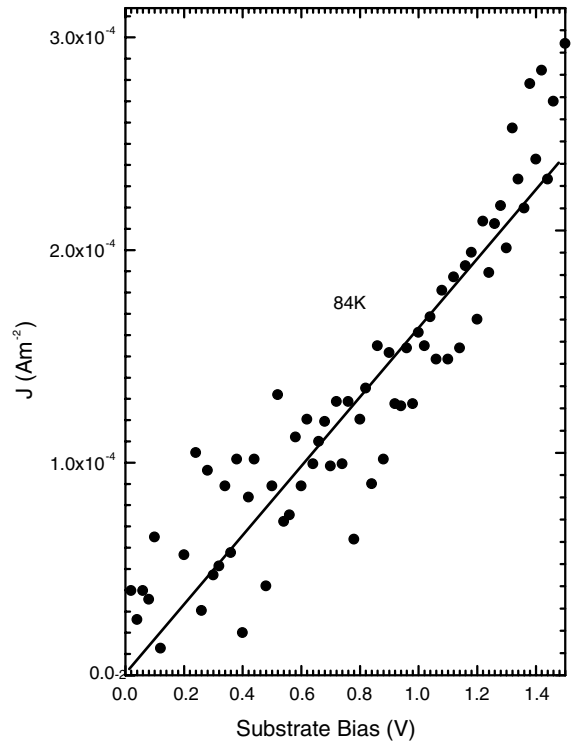


Fig. 11. I – V characteristics at 84 K for the 18 nm TiO₂ layer oxidized at 550 °C at low positive substrate bias. The straight line is indicative of Ohmic conduction or hopping.

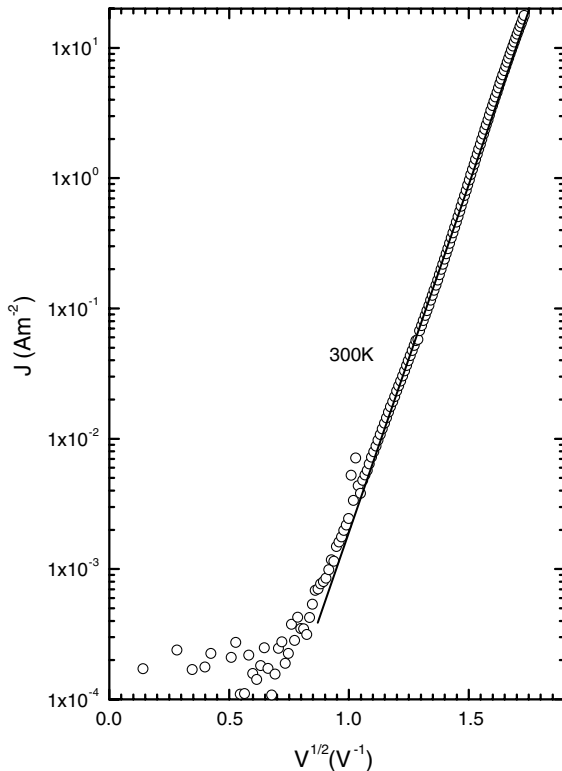


Fig. 12. The Schottky plots at 300 K for the 18 nm TiO₂ layer oxidized at 550 °C for positive substrate bias. The straight line is a fit to equation (4).

silicon dioxide layer is thinner than the 3 nm estimated by Campbell et al. since their post-deposition anneal at 750 °C in oxygen increased the interfacial layer significantly. Further reduction in Schottky current is required to have a VMISTT operating at room temperature with competitive characteristics.

5. Conclusions

We have proposed a new transistor based upon gate modulation of Fowler–Nordheim tunneling in a metal insulator semiconductor diode. The vertical metal insulating tunnel transistor (VMISTT) can be fabricated by conventional methods and complementary devices with good on/off ratio are possible. This requires controlled Fowler–Nordheim tunneling of electrons and holes from a n-type and p-type semiconductor, respectively.

The Schottky-barrier emission leakage currents should be suppressed as far as possible. We have grown p-type silicon–titanium dioxide–aluminium diodes with 7 and 10 nm Ti films thermally oxidized at 450, 500, and 550 °C. Fowler–Nordheim tunneling is shown to be the dominant current mechanism at low temperature and biases above 2 V corresponding to a barrier height of 0.4 eV. At low temperatures the only leakage current is hopping, but at room temperature considerable Schottky emission is still present.

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