Asymmetric Gate-Induced Drain Leakage and Body Leakage in Vertical MOSFETs With Reduced Parasitic Capacitance

Enrico Gili, *Member, IEEE*, V. Dominik Kunz, Takashi Uchino, *Member, IEEE*, Mohammad M. Al Hakim, C. H. de Groot, *Member, IEEE*, Peter Ashburn, *Member, IEEE*, and Stephen Hall, *Member, IEEE*

***Abstract*—Vertical MOSFETs, unlike conventional planar MOSFETs, do not have identical structures at the source and drain, but have very different gate overlaps and geometric configurations. This paper investigates the effect of the asymmetric source and drain geometries of surround-gate vertical MOSFETs on the drain leakage currents in the OFF-state region of operation. Measurements of gate-induced drain leakage (GIDL) and body leakage are carried out as a function of temperature for transistors connected in the drain-on-top and drain-on-bottom configurations. Asymmetric leakage currents are seen when the source and drain terminals are interchanged, with the GIDL being higher in the drain-on-bottom configuration and the body leakage being higher in the drain-on-top configuration. Band-to-band tunneling is identified as the dominant leakage mechanism for both the GIDL and body leakage from electrical measurements at temperatures ranging from −50 to 200 °C. The asymmetric body leakage is explained by a difference in body doping concentration at the top and bottom drain–body junctions due to the use of a p-well ion implantation. The asymmetric GIDL is explained by the difference in gate oxide thickness on the vertical ⟨110⟩ pillar sidewalls and the horizontal ⟨100⟩ wafer surface.**

***Index Terms*—Band-to-band tunneling, body leakage, fillet local oxidation (FILOX), gate-induced drain leakage (GIDL), leakage current, vertical MOSFET.**

I. Introduction

Vertical MOSFETs built on the sidewalls of vertical pillars are increasingly being studied as an alternative to standard lateral MOSFETs for the scaling of CMOS into the nanometer regime [1]–[7]. For this application, they have a number of important advantages over planar MOSFETs. First, surround-gate or double-gate structures allow more channel width and drive current per unit silicon area. Second, the gate length is controlled by nonlithographic methods, allowing devices with sub-100-nm channel length to be fabricated without the need of advanced photolithography. Third, the gate length of the devices is decoupled from the packing density; for random access memory (RAM) applications, long-channel transistors (with lower off currents) can be integrated with short-channel transistors without decreasing the number of devices per unit area. Finally, for double-gate vertical MOSFETs built on the sidewalls of thin ridges, improved short-channel effects can be obtained due to the coupling between the channels on the two sides of the ridges [6], [7].

Manuscript received June 30, 2005; revised February 2, 2006. This work was supported by the European Commission. The review of this paper was arranged by Editor J. Hutchby.

E. Gili, T. Uchino, M. M. Al Hakim, C. H. de Groot, and P. Ashburn are with the School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, U.K. (e-mail: eg02r@ecs.soton.ac.uk).

V. D. Kunz is with the AMI Semiconductors, Oudenaarde 9700, Belgium.

S. Hall is with the Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool L69 3BX, U.K.

Digital Object Identifier 10.1109/TED.2006.872361

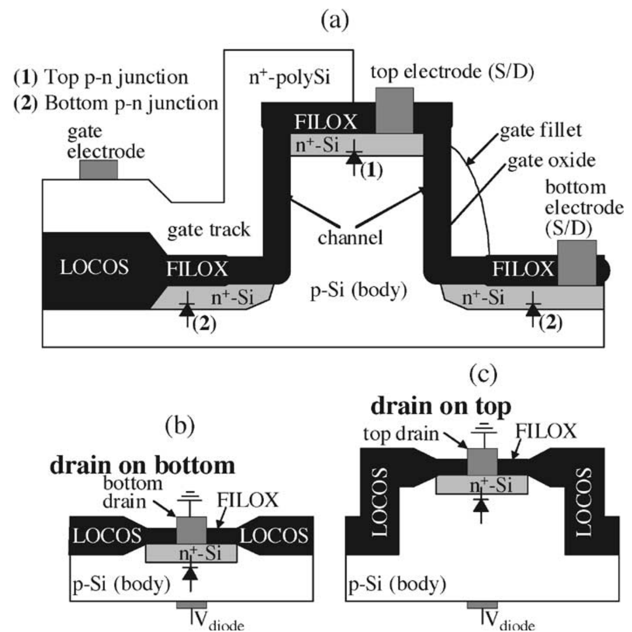

Fig. 1. (a) Schematic cross section of a surround-gate vertical MOSFET fabricated with the FILOX process [9], [10]; S/D = source−drain. Asymmetric top and bottom structures of the body–drain p-n junctions. Schematic cross section of the large-area ungated diodes with the same doping profile at the (b) bottom and (c) top body–drain junctions of the vertical MOSFETs. The large-area diodes had an area (A_{diode}) of 22 200 μm^2.

An important disadvantage of vertical MOSFETs is the increased overlap capacitance between the gate and the source–drain regions. The reduction of this capacitance has been a recurring theme in the literature [5], [8]. Recently, a new technology has been developed to reduce this overlap capacitance, which is called the fillet local oxidation (FILOX) process [9], [10]. In this process, a thicker oxide is grown at the bottom and top of the active pillar using a nitride spacer to suppress oxidation on the pillar sidewalls. This structure is illustrated schematically in Fig. 1(a), where it can be seen that the FILOX oxide reduces the overlap capacitance between the gate and the source–drain electrodes. A further potential disadvantage of

0018-9383/$20.00 © 2006 IEEE

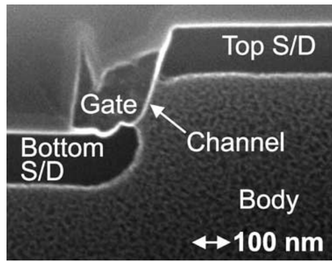

Fig. 2. SEM cross section of the active area of a surround-gate vertical MOSFET with a 130-nm channel length.

vertical MOSFETs is the inherent asymmetry of the structure in the drain-on-top and drain-on-bottom configurations, which can make it difficult to use source and drain terminals interchangeably in different circuit architectures. On the contrary, this is not an issue in planar MOSFETs, where the interchange of source and drain has no effect on the electrical characteristics. The asymmetry of vertical MOSFETs is potentially exacerbated in the FILOX process because any bird's beak arising from the FILOX will be different at the top and bottom of the pillar. Further study of the asymmetry of the electrical characteristics of vertical MOSFETs is essential to determine whether this is an issue and, if so, to identify the physical mechanisms responsible for asymmetric behavior.

In this paper, we investigate the gate-induced drain leakage (GIDL) and the body leakage of FILOX vertical MOSFETs in the drain-on-top and drain-on-bottom configurations to identify the effect of the asymmetric source–drain geometry on the OFF-state leakage. The temperature dependence of the leakage currents is also studied to identify the physical mechanisms responsible for the leakage in the two configurations, and simulations are performed to confirm the mechanisms. It is shown that both the GIDL and the body leakage of vertical MOSFETs are asymmetric when the source and drain are interchanged, with GIDL being higher in the drain-on-bottom configuration and body leakage being higher in the drain-on-top configuration.

II. Experimental Procedure

Surround-gate n-channel vertical MOSFETs with channel length ranging from 50 to 200 nm were fabricated with the FILOX process [9], [10]. The transistor fabrication began with dry etch of silicon pillars, followed by stress relief oxide growth and silicon nitride deposition. The nitride layer was then anisotropically etched to create a nitride spacer around the perimeter of the pillar, after which thermal oxidation was carried out to create the FILOX oxide layer illustrated in Fig. 1(a). After stripping of the nitride layer and stress relief oxide, a gate oxide was grown, and an *in situ* doped polysilicon layer was deposited and patterned to produce a polysilicon surround gate on the pillar sidewall. Finally, the source–drain electrodes were fabricated by ion implantation, and contacts and metal were added. Further details of the fabrication process can be found in the literature [9], [10]. A scanning electron microscopy (SEM) cross section of a completed vertical MOSFET with a 200-nm channel length is shown in Fig. 2.

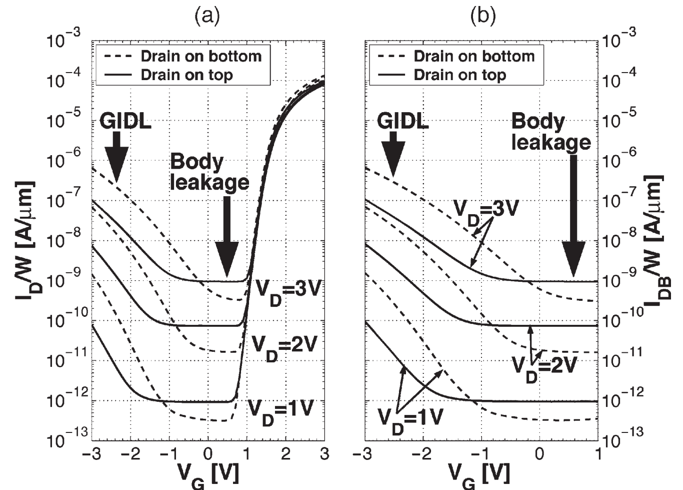

Fig. 3. (a) Measured transfer characteristics in the drain-on-top and drain-on-bottom configurations of a typical surround-gate vertical MOSFET with a 32-μm channel width (W) and a 200-nm channel length (L); V_S (source bias) $= V_B$ (body bias) $= 0$ V; $V_G =$ gate bias; $V_D =$ drain bias; $I_D =$ drain current. (b) Measured gated diode characteristics in the drain-on-top and drain-on-bottom configurations for the same device; $V_B = 0$ V; source floating; $I_{\mathrm{DB}} =$ drain−body current.

Transistor electrical characterization was performed on a temperature-controlled chuck linked to a semiconductor parameter analyzer. Initial measurements were taken at room temperature, and then, detailed measurements were made at different temperatures, ranging from −50 to 200 °C. Vertical MOSFETs with channel width W ranging between 32 and 52 μm and channel length L of 200 nm were characterized. Three types of electrical measurement were made, all in both the drain-on-top and drain-on-bottom configurations. The first measurement was of transistor transfer characteristics for positive and negative gate voltages, with the body contact grounded. The second measurement was of gated diode characteristics. This measurement was made on the transistors, with the source floating, the body grounded, and the bias applied to the gate and drain. The final measurement was of diode current–voltage characteristics, with the objective of investigating the characteristics of the top and bottom body–drain p-n junctions. These measurements were not performed directly on the transistors because the top and bottom drain–body junction areas were different [Fig. 1(a)]. Instead, the drain–body junctions were characterized on the large-area (22 200 μm^2) ungated p-n junctions with doping profile and pillar height identical to the bottom [Fig. 1(b)] and top [Fig. 1(c)] junctions of the vertical MOSFETs.

III. Results

Fig. 3(a) shows the typical measured transfer characteristics of the surround-gate vertical MOSFETs in the drain-on-top and drain-on-bottom configurations. The devices have a threshold voltage of 1.7 V in both configurations, and only a small difference in the on-state currents is observed [9]. In contrast, in the OFF-state region of operation, a large difference (about a factor of 10) in the drain leakage currents is observed when the source and drain are interchanged. Two different regions of the characteristics can be distinguished in the OFF-state region of

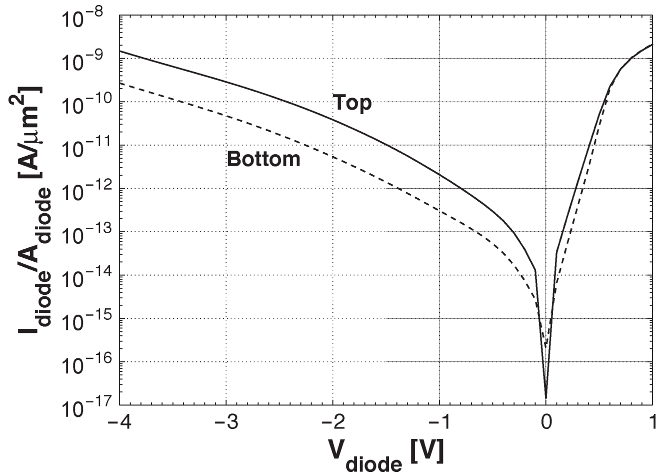

Fig. 4. Current–voltage (I_{diode}–V_{diode}) characteristics of the top and bottom body–drain p-n junctions measured on the large-area ungated diodes shown in Fig. 1(b) and (c).

operation [Fig. 3(a)]. At low gate bias V_G, the drain current is independent of V_G. This indicates a body leakage mechanism in which the current depends only on the drain–body bias. In contrast, at higher negative gate bias, the drain current is strongly dependent on V_G. This indicates the presence of GIDL, which varies with both the gate bias and the drain bias V_D. The GIDL at high negative gate bias is a factor of approximately 10 higher in the drain-on-bottom configuration than in the drain-on-top configuration. In contrast, the body leakage at low gate bias is lower in the drain-on-bottom configuration than in the drain-on-top configuration.

To further investigate the asymmetric OFF-state leakage, Fig. 3(b) shows the gated diode characteristics in which the source of the vertical MOSFET is left floating. The OFF-state leakage can be more easily distinguished in this measurement mode because both the subthreshold and the ON-state currents are suppressed. It can be seen that the values of body leakage obtained from the gated diode measurement are similar to those obtained at low gate bias in the OFF-state region of the transfer characteristic. This confirms that the gate-bias-independent current seen at low gate bias in Fig. 3(a) is due to body leakage. Furthermore, the same asymmetry in the characteristics is observed for the drain-on-bottom and drain-on-top configurations in Fig. 3(a) and (b). The body leakage is lower in the drain-on-bottom configuration, whereas the GIDL is about a decade higher.

To further confirm the asymmetry in the body leakage, Fig. 4 shows the results of measurements of the current–voltage characteristics of the large-area ungated diodes with the same drain–body doping profile as the transistors [Fig. 1(b) and (c)]. The data from the top and bottom drain–body junctions are directly comparable because the diodes have the same area. In reverse bias, the leakage current is a decade higher for the top (solid line) than for the bottom drain–body junction (dashed line). This result confirms the asymmetry in the body leakage, with the top junction giving higher values of body leakage than the bottom junction.

To investigate the leakage mechanisms, Fig. 5 shows measurements of the gated diode characteristics [Fig. 5(a)] and

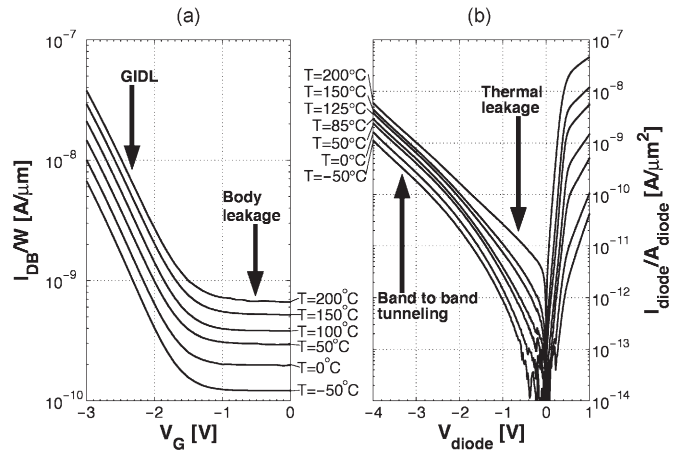

Fig. 5. (a) Measured gated diode characteristics at temperatures ranging between −50 and 200 °C, measured on surround-gate vertical MOSFETs in the drain-on-top configuration with $L = 200$ nm and $W = 52$ μm; source floating; $V_B = 0$ V; $V_D = 2$ V. (b) Measured current–voltage diode characteristics of the bottom body–drain p-n junction at temperatures ranging between −50 and 200 °C, measured on the large-area ungated diode shown in Fig. 1(b).

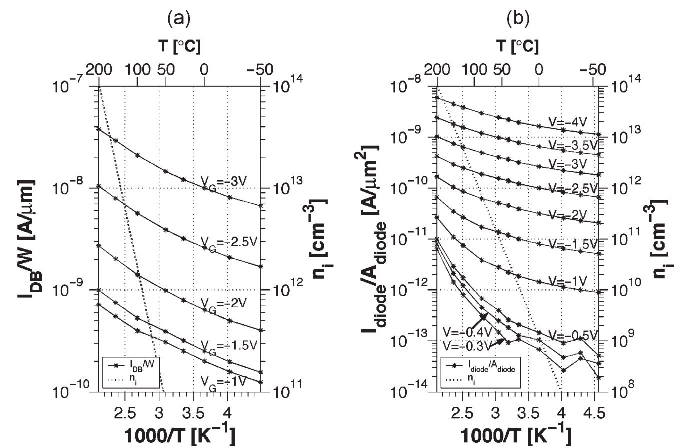

Fig. 6. (a) Reciprocal temperature dependence of the gated diode characteristics [Fig. 5(a)] for different values of gate bias. (b) Reciprocal temperature dependence of the large-area diode leakage [Fig. 5(b)] for different values of reverse bias ($V = V_{\mathrm{diode}}$). The experimental data are compared with the temperature dependence of the intrinsic carrier concentration in Si (n_i) [14].

the large-area diode current–voltage characteristics [Fig. 5(b)] at different temperatures. The gated diode characteristics were measured for the drain-on-top configuration at a drain bias of 2 V. The gated diode characteristics in Fig. 5(a) show a similar temperature dependence in the GIDL and the body leakage regions of the characteristic, indicating that a similar mechanism controls the leakage current in the two regions. The large-area diode current–voltage characteristics in Fig. 5(b) show a different temperature dependence at low reverse voltages than at high. At low reverse voltages around 0.5 V, a strong temperature dependence is seen at high temperatures ($T > 50$ °C), whereas at high reverse voltages, a weak temperature dependence is observed. This result indicates that different mechanisms dominate the characteristics at low and high reverse biases.

Fig. 6 shows measurements of the reciprocal temperature dependence of the gated diode characteristics and the large-area diode current–voltage characteristics. In Fig. 6(a), the gated

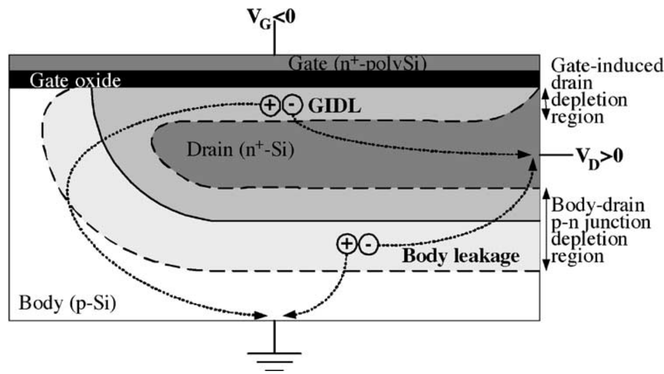

Fig. 7. Schematic cross section of the drain region of a MOSFET showing a representation of the GIDL and the body leakage.

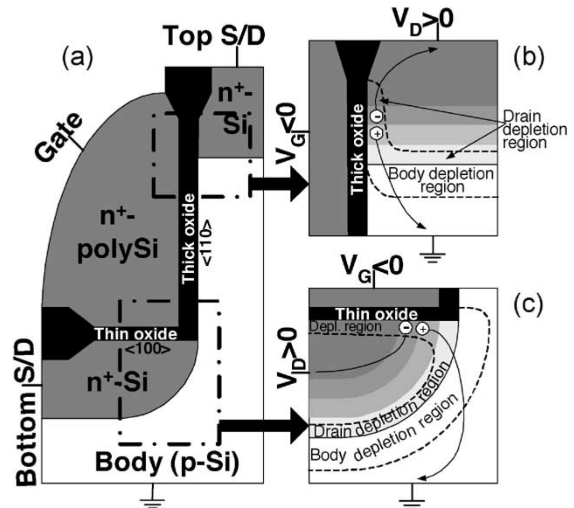

Fig. 8. (a) Schematic cross section of the pillar sidewall of a vertical MOSFET, including a representation of the GIDL mechanism (b) at the top and (c) at the bottom gate/drain overlap regions. The ⟨100⟩ horizontal surface and the ⟨110⟩ vertical sidewall are indicated. The gray scale in (b) and (c) represents the area where the arsenic doping concentration decreases rapidly. The dashed lines show the locations of the depletion regions.

diode current is plotted as a function of reciprocal temperature for different values of gate voltage. It can be seen that the gated diode current has a weak temperature dependence over the whole temperature range and for all values of gate voltage. In Fig. 6(b), the diode leakage is plotted as a function of reciprocal temperature for different values of reverse bias. At high reverse bias, the leakage has a weak temperature dependence, which suggests that the mechanism controlling the large-area diode leakage at high bias is the same as that controlling the gated diode current. However, at low reverse bias, the temperature dependence of the diode leakage current shows a stronger temperature dependence at high temperatures ($T > 50\ ^\circ\text{C}$).

IV. Discussion

A. Leakage Mechanisms

In the OFF-state region of operation of a conventional lateral MOSFET, the drain leakage current is generally due to two main contributions, namely: 1) the GIDL and 2) the body leakage [11], [12]. A schematic representation of these two leakage mechanisms is shown in Fig. 7, which is a cross section of the drain region of a MOSFET. Fig. 7 shows the depletion regions induced by a negative gate voltage and a positive drain voltage. The body–drain depletion region is due to the reverse-biased body–drain p-n junction. An additional gate-induced depletion region is formed at the surface for $V_{\rm DG} > 0$, where the gate overlaps the drain extensions of the MOSFET. The gate-induced depletion region gives rise to band bending in the drain extensions. When the band bending exceeds the silicon bandgap, electrons can tunnel into the drain from the valence to the conduction band [11]. The generated electron–hole pairs are then collected by the drain and body contacts, respectively, giving rise to GIDL. Band-to-band tunneling can also occur in the body–drain depletion region at high reverse biases, giving rise to body leakage [12]. This type of leakage is very sensitive to the body doping concentration because an increased doping gives rise to a higher electric field and an enhanced band-to-band tunneling. On the other hand, both GIDL and body leakage can arise from thermal generation of carriers in the depletion regions [12]–[14]. This mechanism is dominant in devices with low body and drain doping concentrations. It has been demonstrated that the reciprocal temperature dependence of the thermal generation current within the depletion region is the same as that of the intrinsic carrier concentration n_i [14]. However, in the short-channel vertical MOSFETs that we have analyzed here, the drain and body doping concentrations are higher to control the short-channel effects and source–drain series resistance, and hence, the main leakage mechanism is the band-to-band tunneling of electrons.

In this paper, the leakage current mechanisms can be identified from the temperature dependence of the currents shown in Figs. 5 and 6. The results in Fig. 6(a) show that the GIDL has a much weaker temperature dependence than the intrinsic carrier concentration, which is shown as a dotted line. A weak temperature dependence of this type is typical of band-to-band tunneling [13], and hence, we can infer that this mechanism is responsible for the GIDL seen in this work. For the drain-on-top configuration, this GIDL occurs where the gate spacer overlaps the n^+ drain at the top of the pillar, as shown schematically in Fig. 8(b). For the drain-on-bottom configuration, the GIDL occurs where the gate spacer overlaps the n^+ drain at the bottom corner of the pillar, as shown in Fig. 8(c). A similar weak temperature dependence is seen at high reverse bias in Fig. 6(b) for the diode reverse leakage, and hence, we can also attribute this leakage to band-to-band tunneling. At low reverse bias and high temperatures, the temperature dependence is much stronger and approaches the slope of the intrinsic carrier concentration. At these temperatures, the leakage current is dominated by thermal generation of carriers within the depletion region [14].

B. Asymmetric Body Leakage

As shown in Fig. 4, the body leakage is a factor of approximately 10 higher in the drain-on-top configuration than in the drain-on-bottom configuration. As the dominant body leakage mechanism at room temperature is band-to-band tunneling, as demonstrated in Fig. 6(b), we have to consider the body

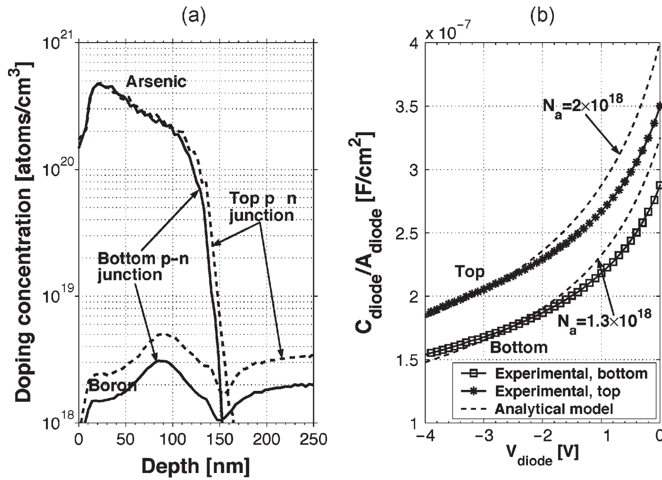

Fig. 9. (a) SIMS measurements of the doping profiles at the top and bottom body–drain p-n junctions [indicated in Fig. 1(a)] of the vertical MOSFETs. (b) Capacitance–voltage ($C_{\rm diode}$–$V_{\rm diode}$) characteristics of the top and bottom body–drain p-n junctions, measured on the large-area ungated diodes shown in Fig. 1(b) and (c); the measurement frequency was 1 MHz; $N_a =$ acceptor doping concentration. The experimental results are compared with the prediction of an analytical model for an abrupt n^+-p junction.

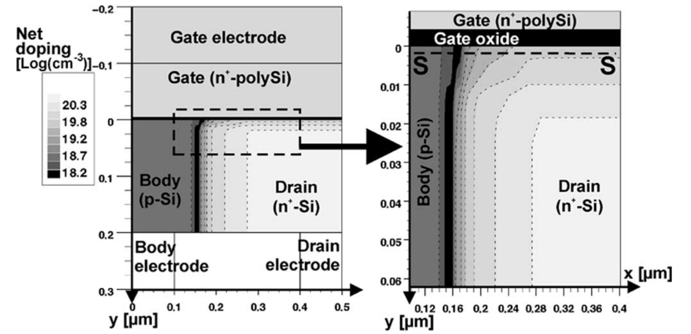

Fig. 10. Model of the gated diodes implemented for the simulation of the GIDL. The gate oxide thickness was used as a fitting parameter in the simulations.

doping as a source of the asymmetry because the band-to-band tunneling current is very sensitive to the doping concentration. A high doping enhances the band bending and the electric field across the reverse-biased body–drain junction. To investigate the role of the body doping, secondary ion mass spectroscopy (SIMS) profiles were measured for the top and bottom body–drain p-n junctions, and the results are presented in Fig. 9(a). These profiles show that the average body doping at the top p-n junction ($N_a \approx 3 \times 10^{18}$ cm^{-3}) is higher than that at the bottom p-n junction ($N_a \approx 2 \times 10^{18}$ cm^{-3}), which is consistent with the higher body leakage in the drain-on-top configuration. This interpretation is confirmed by the body–drain p-n junction capacitance–voltage plots shown in Fig. 9(b). The capacitance is lower for the bottom body–drain junction, indicating a lower body doping concentration. Using an analytical model of an abrupt one-sided n^+-p junction to fit the capacitance–voltage characteristics gives body doping concentrations of 2×10^{18} and 1.3×10^{18} cm^{-3} for the top and bottom body–drain p-n junctions, respectively. These values of body doping concentration are in reasonable agreement with the SIMS profiles given the assumption of an abrupt p-n junction and the uncertainties in the absolute values of SIMS doping concentrations.

The asymmetric doping profiles at the top and bottom of the pillar are caused by the use of a p-type well ion implantation and high-temperature drive-in to dope the body at the beginning of the fabrication process [9], [10]. After the p-well drive-in, a photoresist mask was used to define the pillar, and the exposed Si substrate was dry etched to create the vertical channel. During the pillar dry etch, boron impurities were removed from the area not covered by the pillar photoresist mask. The subsequent local oxidation of silicon (LOCOS) and FILOX high-temperature anneals gave rise to a higher body doping concentration at the top of the pillar than at the bottom, as shown in Fig. 9(a).

C. Asymmetric GIDL

As shown in Fig. 3, the GIDL is a factor of approximately 10 higher in the drain-on-bottom configuration than in the drain-on-top configuration. To investigate the origin of this asymmetry, device simulations were performed using the simplified model of the gated diodes shown in Fig. 10. Measured SIMS doping profiles [Fig. 9(a)] calibrated to measure sheet resistance values were used in the simulations to set the drain doping profile. The body doping profile was assumed, for simplicity, to be constant throughout the structure, as its effect on GIDL is negligible. To simplify the simulated structure, body and drain electrodes were placed at the back of the structure. The simulations were based on a two-dimensional (2-D) GIDL model [15], in which the band-to-band tunneling generation rate ($G_{\rm BBT}$) of hole–electron pairs is a function of the total electric field ($E_{\rm TOT} = (E_x^2 + E_y^2)^{1/2}$) in the gate-induced drain depletion region. The relation between $G_{\rm BBT}$ and $E_{\rm TOT}$ is given by

$$G_{\rm BBT} = A E_{\rm TOT}^2 \, e^{-\frac{B}{E_{\rm TOT}}} \tag{1}$$

where $A = 9.66 \times 10^{18}$ $\rm V^{-2} \cdot s^{-1} \cdot cm^{-1}$ and $B = 3 \times 10^{17}$ $\rm V \cdot cm^{-1}$. This generation mechanism is implemented into the right hand of the continuity equation [16]. The gate oxide thickness was used as a fitting parameter in the simulations.

Fig. 11 shows the simulated gated diode characteristics for the drain-on-bottom and drain-on-top configurations and also for comparison with the measured data. To separate the GIDL component of the OFF-state current, the body leakage current was subtracted from the measured data. Fig. 11 shows that a reasonable fit to the measured GIDL is obtained for a gate oxide thickness of 5 nm for the drain-on-top configuration and 4 nm for the drain-on-bottom configuration. For the drain-on-bottom configuration, the gate oxide is on the horizontal $\langle 100 \rangle$ surface (Fig. 8), and hence, the fitted value of 4 nm can be compared with a measured value of about 4 nm obtained from $\langle 100 \rangle$ test wafers. The measured and fitted values of gate oxide thickness are in excellent agreement. For the drain-on-top configuration, the gate oxide is on the vertical $\langle 110 \rangle$ sidewall (Fig. 8), and

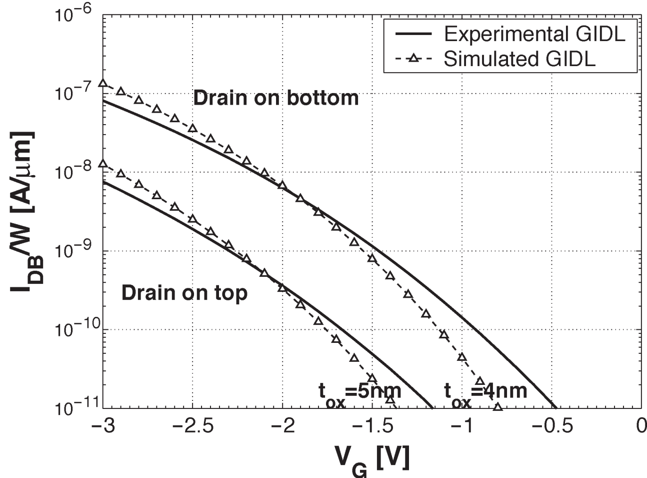

Fig. 11. Comparison between the simulated gated diode characteristics and the experimental gated diode characteristics of a surround-gate vertical MOSFET with $W = 52$ μm and $L = 200$ nm; $V_D = 2$ V; $V_B = 0$ V; source floating. The experimental GIDL curves are obtained by subtracting the body leakage component from the $I_{\mathrm{DB}}(V_G)$ experimental characteristics of the gated diode.

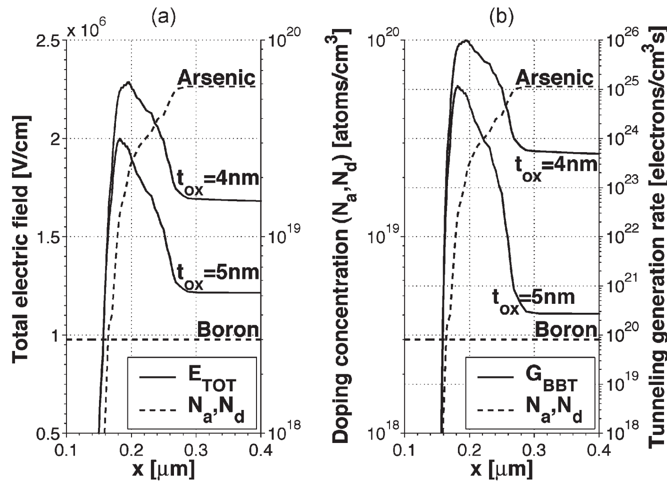

Fig. 12. (a) Simulated total electric field E_{TOT} and (b) simulated band-to-band tunneling generation rate G_{BBT} along a cross section parallel to the gate oxide in the gate-induced drain depletion region (section S–S in Fig. 10); $V_D = 2$ V, $V_G = -3$ V, $V_B = 0$ V; N_a = acceptor doping concentration; N_d = donor doping concentration. The doping profile along the cross section is shown for comparison.

the fitted gate oxide thickness is 25% higher (5 nm) than that obtained in the drain-on-bottom configuration. This 25% difference in fitted oxide thickness is compared with a measured difference of 40% between ⟨100⟩ and ⟨110⟩ surfaces reported in the literature [17]. This agreement is reasonable, given that the pillars are not completely vertical, as shown in Fig. 2.

Fig. 12 shows the simulated total electric field E_{TOT} and the band-to-band tunneling generation rate G_{BBT} on a cross section parallel to the gate oxide in the gate-induced drain depletion region (section S–S in Fig. 10). The 4-nm gate oxide yields a higher electric field [Fig. 12(a)] and, therefore, boosts the band-to-band tunneling generation rate [Fig. 12(b)] and the GIDL. The arsenic doping profiles are also plotted in Fig. 12, and it can be seen that the electric field has a maximum value in the portion of the gate-induced drain depletion region close to the drain–body junction, where the arsenic doping concentration decreases rapidly. This sharp peak in the electric field gives a similar sharp peak in the band-to-band tunneling generation rate in the same physical location. In fact, the band-to-band tunneling generation rate at this location is more than two decades higher than that at the peak of the arsenic profile. This result indicates that the GIDL is highly localized and is therefore not influenced by the area of the gate/drain overlap. The asymmetry in the gate overlaps at the top and bottom of the pillar can therefore be discounted as an explanation for the asymmetric GIDL. The presence of asymmetric bird's beaks from the FILOX process, which would give rise to further asymmetry in the gate overlaps at the top and bottom of the pillar, can also be discounted as an explanation for the asymmetry. We can therefore conclude that the asymmetric GIDL can be explained solely in terms of the different gate oxide thicknesses on the horizontal ⟨100⟩ and vertical ⟨110⟩ surfaces.

The asymmetry in the drain leakage currents of vertical MOSFETs could be used to advantage if the transistors were fabricated on ⟨110⟩ wafers instead of ⟨100⟩ wafers. For this arrangement, a thin gate oxide would be obtained on the vertical ⟨100⟩ pillar sidewall, whereas a thicker oxide would be obtained on the horizontal ⟨110⟩ surface. Both the GIDL and the body leakage would then be lower in the drain-on-bottom configuration. In this situation, vertical MOSFETs operating in the drain-on-bottom configuration would provide lower OFF-state leakage than conventional planar MOSFETs, which could prove useful in applications that require low standby power.

V. Conclusion

In this paper, we have presented experimental evidence of asymmetric leakage currents in surround-gate vertical MOSFETs with dry-etched channels and ion-implanted source and drain. The asymmetry is observed in the transfer characteristics of the devices when the source and the drain are interchanged, with GIDL being higher in the drain-on-bottom configuration and body leakage being higher in the drain-on-top configuration. The temperature dependence of the leakage currents has been analyzed, and the band-to-band tunneling of electrons from the valence band to the conduction band has been identified as the dominant leakage mechanism. The asymmetric body leakage is process induced and arises from a slightly larger body doping concentration at the top of the pillar than at the bottom due to the use of a well implant for the body doping. On the other hand, the asymmetric GIDL is explained by a thicker gate oxide on the vertical ⟨110⟩ pillar sidewall than on the horizontal ⟨100⟩ wafer surface. The thinner gate oxide at the bottom of the pillar increases the electric field and enhances the band-to-band tunneling, which is the cause of the GIDL. The good agreement between the simulated and measured leakage characteristics of the devices is a strong indication that the FILOX process has a negligible impact on the asymmetric drain leakage currents.

REFERENCES

[1] T. Schulz, W. Rosner, L. Risch, A. Korbel, and U. Langmann, "Short-channel vertical sidewall MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1783–1788, Aug. 2001.

[2] K. Mori, A. Duong, and W. F. Richardson, "Sub-100-nm vertical MOSFET with threshold voltage adjustment," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 61–66, Jan. 2002.

[3] L. Risch, W. H. Krautschneider, F. Hofmann, H. Schaefer, T. Aeugle, and W. Roesner, "Vertical MOS transistor with 70 nm channel length," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1495–1498, Sep. 1996.

[4] H. Gossner, F. Wittmann, I. Eisele, T. Grabolla, and D. Behammer, "Vertical MOS technology with sub-0.1 μm channel lengths," *Electron. Lett.*, vol. 31, no. 16, pp. 1394–1396, Aug. 1995.

[5] J. M. Hergenrother, S.-H. Oh, T. Nigam, D. Monroe, F. P. Klemens, and A. Kornblit, "The vertical replacement-gate (VRG) MOSFET," *Solid State Electron.*, vol. 46, no. 7, pp. 939–950, Jul. 2002.

[6] J. Moers, S. Trellenkamp, M. Goryll, M. Marso, A. van der Hart, and S. Hogg *et al.*, "Top contacts for vertical double-gate MOSFETs," *Microelectron. Eng.*, vol. 64, no. 1–4, pp. 465–471, Oct. 2002.

[7] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki, "Ultrathin channel vertical DG MOSFET fabricated by using ion-bombardment-retarded etching," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2078–2085, Dec. 2004.

[8] M. Jurczak, E. Josse, R. Gwoziecki, M. Paoli, and T. Skotnicki, "Investigation on the suitability of vertical MOSFET's for high speed (RF) CMOS applications," in *Proc. ESSDERC Conf.*, 1998, pp. 172–175.

[9] E. Gili, V. Kunz, C. de Groot, T. Uchino, P. Ashburn, D. Donaghy, S. Hall, Y. Wang, and P. Hemment, "Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance," *Solid State Electron.*, vol. 48, no. 4, pp. 511–519, Apr. 2004.

[10] V. Kunz, T. Uchino, C. de Groot, P. Ashburn, D. Donaghy, S. Hall, Y. Wang, and P. Hemment, "Reduction of parasitic capacitance in vertical MOSFET's by spacer local oxidation (FILOX)," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1487–1493, Jun. 2003.

[11] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.*, vol. EDL-8, no. 11, pp. 515–517, Nov. 1987.

[12] G. A. M. Hurkx, "On the modelling of tunnelling currents in reverse-biased p-n junctions," *Solid State Electron.*, vol. 32, no. 8, pp. 665–668, Aug. 1989.

[13] W. P. Noble, S. H. Voldman, and A. Bryant, "The effects of gate field on the leakage characteristics of heavily doped junctions," *IEEE Trans. Electron Devices*, vol. 36, no. 4, pp. 720–726, Apr. 1989.

[14] A. S. Grove and D. J. Fitzgerald, "Surface effects on p-n junctions characteristics of surface space-charge regions under non-equilibrium conditions," *Solid State Electron.*, vol. 9, no. 8, pp. 783–806, Aug. 1966.

[15] S. A. Parke, J. E. Moon, H. C. Wann, P. K. Ko, and C. Hu, "Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1694–1703, Jul. 1992.

[16] *Atlas User's Manual–Process Simulation Software*, Silvaco Int. Ltd., Santa Clara, CA, 2000.

[17] B. Goebel, D. Schumann, and E. Bertagnolli, "Vertical n-channel MOSFETs for extremely high density memories: The impact of interface orientation on device performance," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 897–906, May 2001.

Enrico Gili (M'05) was born in Pinerolo, Italy, in 1977. He received the M.S. degree in physics engineering from the Institut National Polytechnique, Grenoble, France, in 2001, and the M.S. degree in materials engineering from the Politecnico di Torino, Turin, Italy, in 2002.

He was with the Department of Electronics and Computer Science, University of Southampton, Southampton, working on fabrication and characterization of CMOS-compatible vertical MOSFETs with reduced parasitics. In 2005, he joined Innos Ltd., Southampton, where he is currently a Process Engineer in a research and development semiconductor fabrication facility.

V. Dominik Kunz was born in Eberbach, Germany, in 1967. He received the Dipl.Ing. degree in electrical engineering from the Technische Universitaet Berlin, Berlin, Germany, in 1995, and the Ph.D. degree from the University of Southampton, Southampton, U.K., in 2003, for work on CMOS-compatible surround-gate vertical MOSFETs with reduced parasitics.

He was with Tandberg Television, Southampton, for five years, where he was involved in the development of the first commercially available digital terrestrial television ASIC as well as in related hardware and software projects. In 2003, he joined AMI Semiconductors, Oudenaarde, Belgium, where he is currently a Project Leader.

Takashi Uchino (M'98) received the M.S. and Ph.D. degrees in materials science from Tsukuba University, Ibaraki, Japan, in 1986 and 1989, respectively.

In 1989, he joined the Central Research Laboratory, Hitachi, Ltd., Japan, where he was engaged in the development of high-speed silicon bipolar, BiCMOS, and CMOS devices and their technologies. From 1999 to 2002, he was with the Semiconductor and Integrated Circuits Group, Hitachi, Ltd., Japan. In 2002, he joined the School of Electronics and Computer Science, University of Southampton, Southampton, U.K., as a Research Staff. His present research interests include the technology and physics of novel devices and carbon nanotube devices.

Mohammad M. Al Hakim received the B.S. and M.S. degrees in electrical and electronic engineering from Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, in 1999 and 2001, respectively. He is currently working toward the Ph.D. degree in electrical and electronic engineering at the University of Southampton, Southampton, U.K.

He joined the Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, as a Lecturer. His research interests include semiconductor devices modeling, fabrication and characterization, and designing architectures for three-dimensional CMOS integration.

C. H. de Groot (M'01) received the M.S. degree in physics from the University of Groningen, Groningen, The Netherlands, in 1994, and the Ph.D. degree from the University of Amsterdam, Amsterdam, The Netherlands, in 1998, with research carried out at the Philips Research Laboratories in Eindhoven, The Netherlands. His Ph.D. dissertation was on NdFeB permanent magnets and magnetism in rare-earth intermetallic compounds.

From 1998 to 2000, he was a Research Fellow at the Francis Bitter Magnet Laboratory, Massachusetts Institute of Technology, Cambridge, where he conducted research on spin tunnel junction. Since 2000, he has been with the Department of Electronics and Computer Science, University of Southampton, Southampton, U.K., as a Research Lecturer. His research interest includes nanoelectronics with emphasis on spintronics and post-CMOS field-effect transistors.

Peter Ashburn (M'89) was born in Rotherham, U.K., in 1950. He received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from the University of Leeds, Leeds, U.K., in 1971 and 1974, respectively. His dissertation topic involved the experimental and theoretical study of radiation damage in silicon p-n junctions.

In 1974, he joined the technical staff of Philips Research Laboratories and worked initially on ion-implanted integrated circuit bipolar transistors and then on electron lithography for submicrometer integrated circuits. In 1978, he joined the academic staff of the Department of Electronics and Computer Science, University of Southampton, as a Lecturer, and is currently a Personal Chair in Microelectronics. Since taking up a post at the University of Southampton, he has worked on polysilicon emitter bipolar transistors, high-speed bipolar and BiCMOS technologies, SiGe heterojunction bipolar transistors, and vertical MOSFETs. His current research interests include diffusion suppression using fluorine, transistor in a grain, ultimate CMOS, and carbon nanotube electronics. He has authored and coauthored 200 papers in the technical literature and has authored books on the design and realization of bipolar transistors in 1988 and on silicon germanium heterojunction bipolar transistors in 2003.

Stephen Hall (M'93) received the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1987, for his research on a new form of integrated injection logic in the GaAs/AlGaAs materials system.

He is currently the Head of the Department of Electrical Engineering and Electronics, University of Southampton, Southampton, U.K., and serves on a number of U.K. national advisory groups. He took up a lecturing post and began working on silicon-on-insulator materials characterization and device physics in the separation by implanted oxygen and oxidized porous Si systems, which was in collaboration with U.K. university and industrial collaborators. Other areas of activity concerned the fabrication and electrical assessment of cobalt disilicide Schottky diodes together with silicon–germanium materials characterization and device physics for both SOI heterojunction bipolar transistor and MOSFET. His current major activities concern novel design concepts for very deep submicrometer vertical MOSFETs, high-k dielectrics and novel device, and circuit blocks for third-generation neural network application.