Reducing Power Dissipation in SRAM during Test

Dilillo Luigi[1]*, Rosinger Paul[1], Al-Hashimi Bashir M.[1] and Girard Patrick[2]

[1]Dept. of Electronics and Computer Science, Univ. of Southampton, Southampton, United Kingdom, {ld3, pmr, bmah}@usc.edu

[2] Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier – LIRMM, Montpellier, France, girard@lirmm.fr

* corresponding author: Dilillo Luigi

Address:

University of Southampton

Electronics and Computer Science (ECS) Department

Highfield, Southampton, SO17 1BJ, United Kingdom

Office : +44-(0)238-059-3119

Fax : +44 (0)238-059-2901

Email : ld3@ ecs.soton.ac.uk

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Abstract *— In this paper we analyze the power consumption of SRAM memories and demonstrate that the full functional pre-charge activity is not necessary during test because of the predictable addressing sequence. We exploit this observation in order to minimize power dissipation during test by eliminating the unnecessary power consumption associated with the pre-charge activity. This is achieved through a modified pre-charge control circuitry, exploiting the first degree of freedom of March tests, which permits to choose a specific addressing sequence. Further, the modified pre-charge logic allows also the switching between the normal functional mode and the low power test mode. We demonstrate that the modified pre-charge control circuitry has little or no effect on the memory performance. We analyze the sources of power consumption in functional and low power test mode, and we show how the power dissipation is computed for bit and word-oriented SRAMs. The efficiency of the proposed solution is validated through extensive Spice simulations for both bit-oriented and word-oriented SRAM.*

Keywords — SRAM , Low Power, Test March, Pre-charge

1 INTRODUCTION

Reducing power dissipation during testing of complex Systems-on-Chip (SoC) has been acknowledged as a major concern. Industrial research has shown that the power dissipation during test mode can be several times larger than in normal functional mode [1, 2]. We have chosen to focus our attention on memories because, as indicated by the ITRS'03 [3], by 2008 over 90% of SoC area will be employed by memories. Reducing power during test of memories is important because it can make possible to test several memories of the SoC at same time reducing significantly the test time. While numerous papers on constraining power dissipation during test exist [4-9], only few publications address the problem of reducing test power in memories. In fact, only two papers have been published in this field [10-11]. However, the authors outline techniques that mainly reduce power during functional mode and they indicate how their technique can be employed during test or error correction.

In this paper, we propose a new method that minimizes test power in SRAM memories by exploiting the predictability of the addressing sequence. In [12], we have proposed a preliminary version of this study that we complete and generalize with this paper. It is shown in [13-14] that the pre-charge circuits are the main contributors to power dissipation in SRAM. These circuits have the role of pre-charging and equalizing the long and high capacitive bit lines. This action is essential to ensure correct memory operation. In this work we have developed a technique that reduces the pre-charge activity during test. This technique is based on the fact that in functional mode the cells are selected in random sequence, and therefore all pre-charge circuits need to be always active, while during the test mode the access sequence is known, and consequently, only the columns that are to be selected need to be pre-charged. We implemented this low power test mode by using a modified pre-charge control circuitry.

The rest of the paper is organized as follows. In Section 2, we describe the SRAM pre-charge operation in functional mode. In Section 3, we present the new method that allows reducing the pre-charge activity during test mode, and its implementation in Section 4. Experimental validation of the proposed low power technique for bit-oriented and word-oriented SRAM is presented in Section 5. Final future work is discussed in section 6. Conclusions are given in Section 7.

2 BACKGROUND: SRAM FUNCTIONAL MODE

In random access memories during functional mode, the addressing sequence is unpredictable. Consequently, all bit lines need to be pre-charged (to VDD) in order to have all the array columns ready for a new operation. When a cell is selected for a read/write operation, the corresponding pre-charge circuit is normally turned off during the time required for the operation. For the columns that are not involved in the operation, the pre-charge circuit is commonly left ON and the corresponding cells undergo a stress called RES (Read Equivalent Stress), as it has been demonstrated in [15]. For example, in an 8kx32 bit-oriented SRAM, organized as an array of 512 rows x 512 column, when a read/write operation is performed on a cell, the other 511 cells of the same row undergo RESs. This is illustrated in Figure 1. When the cell $C_{i,0}$ is selected for a read/write operation, the word line selection signal WLi is activated and all the cells of the i^{th} row are selected, and thus connected with their bit lines.

The actual operation is performed on cell $C_{i,0}$, while all the other cells in the row undergo RESs. With the pre-charge circuits (Pr_j) active and the word line command being high on the unselected columns, the cells fight against the pre-charge circuits, that pull-up the voltage level at VDD. In Figure 2, we show the operational diagrams of a pre-charge circuit of a selected and an unselected column. In the following, we will identify the two main sources of power consumption in the unselected columns related to the pre-charge activity. Firstly, the cells in the unselected columns

consume power due to the RES. Secondly, there is power dissipation in the pre-charge circuits of these columns because they are always *ON*. In the normal operation mode of a random access memory, this pre-charge activity is essential and the RES is tolerated, because at the end of each operation all the columns of the array, including the current selected column, need to be ready for the next operation, whose location is unpredictable.

During the memory test mode, however, the addressing order to access the cells (and the columns) is known. Consequently the power dissipation due to pre-charge and RESs could be significantly reduced by pre-charging only the necessary columns as it will be shown in the following section. In Section 3, we will consider bit-oriented SRAM to explain the proposed low power test method, then we will show how the method can be extended to word-oriented memories in Section 5.

3 REDUCING TEST POWER

Memories are mainly tested with fault-oriented algorithms, such as March tests [16]. All March tests are characterized by six Degrees Of Freedom (DOF) and the first one states: any arbitrary address sequence can be defined as an $\Uparrow$ sequence, as long as all addresses occur exactly once ($\Downarrow$ is the reverse of $\Uparrow$). The fault detection properties are independent of the utilized address sequence [17-18]. This means that we can choose the addressing sequence of a March test without changing its capability to cover the target faults, for most March algorithms. We exploit this property of March tests in order to minimize power dissipation during test by eliminating the unnecessary pre-charge activity.

For this purpose, we have chosen the addressing sequence ‘word line after word line'. For example, let us consider an SRAM organized as an array of *n* rows and *m* columns. The read and write operations of each March element need to be acted first on all the *m* cells of the first word line, then on the m cells of the second word line, and so on, as shown in Figure 3. The BIST structure that can

produce this addressing sequence can be easily implemented by two counters that we call counter A and counter B. The first counter A should increment at each March element operation. This counter gives the part of address useful to select a column in the array. The terminal count (overflow) signal of this first counter A can be used as clock signal of the second counter B, which gives the address useful to select a row in the array. In practice, the counter B starst with 00…00 selecting the first row of the array and holds on this selection during the time that the counter A produces all the addresses of the cells in the row in the order from 0 to m-1, where *m* is the number of columns. When counter A reaches the number *m-1* the terminal count (overflow) signal is high enabling the counter B to increase of one unit. This means that the second row is now selected and counter A produces again all the addresses of the cells in the row. The process goes on until all rows and all the columns of the array are selected and it is repeated for all the elements of the March test to be run.

With this particular addressing sequence, word line after word line, when one March element is operated on a certain cell, and thus in a certain column of the array, the following cell to be selected is placed in the column that immediately follows. This means that, for a bit-oriented SRAM, the pre-charge action is required only in two columns of the entire memory array:

- The selected column, because the bit line restoration is needed for each following operation of the current March element.
- The column that immediately follows, because the next cell to be accessed is placed there.

Considering the scenario of a 512x512 SRAM array configuration, we have:

- In the selected column: pre-charge is *OFF* during the first half of the cycle. Pre-charge is *ON* during the second half of the clock cycle, see Figure 2a and 2b.
- In next column to be selected, the pre-charge is *ON* during the entire clock cycle, see Figure 2c and 2d.
- In all the other 510 columns the pre-charge circuit can be turned OFF, because the cells of these columns are not involved in the immediately following operation. This leads to a significant saving in cell array power consumption, as it will be shown in the experimental section.

Figure 4 shows the proposed “low power test” scenario when the memory array column ‘0’ is selected. For the 510 columns where the pre-charge circuit is inactive, the cells are still selected by the common word line selection signal. This implies that these cells are still interacting with their corresponding bit lines. These bit lines behave like floating capacitors, which are not driven any longer by the pre-charge circuits, but by the cells. We have studied this interaction with Spice simulations using the following parameters: technology: 0.13µm; clock cycle: 3ns; voltage supply: 1.6 V. The scheme used in the simulation is depicted in Figure 5, while the results are shown in Figure 6. The scheme in Figure 5 shows two cells $C_{i,j}$ and $C_{i+1,j}$ placed in the same column. Cell $C_{i,j}$ stores ’0’ (node S at ‘0’and node SB at ‘1’) and $C_{i+1,j}$ stores the opposite value ’1’ (node S at ‘1’and node SB at ‘0’). In the first part of the simulation, cell $C_{i\,j}$ is selected (WL_i at VDD) and interacts with the bit lines. After a certain delay, cell $C_{i,j}$ is deselected (WL_i at ‘0’), and cell $C_{i+1,j}$ selected (WL_{i+1} at VDD). The waveforms in Figure 6a and 6b show that the contact between node SB of cell $C_{i,j}$ and bit line BLB has no effect on the voltage levels of BLB and node SB, because both of them are at VDD. On the other hand, the contact between cell node S active at ‘0’ and bit line BL floating at VDD produces the progressive discharge of BL to 0V (logic value ‘0’) in nearly nine clock cycles. This implies that, after a short time, in all the unselected columns, the cells are not stressed anymore by the bit lines. The consequence is that in the unselected cells there is no more power consumption associated with RES, as shown in Figure 6b.

Although the proposed scenario greatly reduces the test power consumption, it should be pointed out that the transition from the current array row *i* to *i+1* may lead to a problem as shown in Figure 7. In this figure we analyze the case in which two cells $C_{i,j}$ and $C_{i+1,j}$ are placed in the same column j and in consecutive rows i and i+1; These cells stores opposite values and are indirectly accessed, *i.e.* other cells of their row are accessed. The cell $C_{i,j}$, stores a ‘0’ and during its indirect accesses has driven its bit lines BL and BLB respectively at ‘0’ and ‘1’. The cell $C_{i+1,j}$ stores a ‘1’, an opposite

value with respect to the value stored in $C_{i,j}$. With the transition from the i^{th} row to the $(i+1)^{th}$ row, these bit lines of column j, with BLB at VDD and BL driven to '0' by cell $C_{i,j}$, are connected to $C_{i+1,j}$ which is indirectly accessed due to the operation in the first cell of row i+1. As the bit lines drive the value of the cell $C_{i+1,}$ (their equivalent capacitances are much larger than the cell nodes capacitances), this event causes the faulty swap of cell $C_{i+1,j}$. The occurrence of this faulty swap is shown in Figure 6c. The solution that we propose for this problem is: in the last operation on the last cell on the current row, the bit line level of all columns is restored at VDD by activating their pre-charge circuits for only this clock cycle (Figure 7). The advantage of this solution is that it preserves the data background independency, which means that any value can be stored in the cells. Note that when both bit lines are at VDD the indirect access of a cell can not cause its faulty swap.

4 PRE-CHARGE CONTROL CIRCUITRY MODIFICATION

According to the proposed low power test technique the SRAM memory can operate in two different modes: a functional mode in which the memory acts normally and a low power test mode in which the addressing sequence is fixed to 'word line after word line' and the pre-charge activity is restricted to two columns for each clock cycle (in bit oriented SRAM): the selected column and the following one. During the final operation on the last cell of each row, the memory returns to functional mode for only one clock cycle to restore the voltage level of all the bit line at VDD. This is necessary in order to prepare the operations in the next row.

We propose a practical implementation of this method consisting in a modification of the pre-charge control circuitry. The modified pre-charge control logic contains an additional element for each column (Figure 8). This element consists of one multiplexer (two transmission gates and one inverter) and one NAND gate. The additional cost of the added logic is ten transistors. The signal LPtest allows the selection between the functional mode and low power test mode. The signal Pr_j is

the original pre-charge signal, while NPrj is the modified pre-charge signal and $\overline{CS_j}$ is the complementary of the column selection signal. The multiplexer performs the mode selection, while the NAND gate forces the functional mode for the column when it is selected for a read/write operation. When LPtest is ON (LPtest = 1), the signal $\overline{CS_j}$ of a selected column j drives the pre-charge of the next column j+1. Note that the pre-charge is active with the input signal NPrj at '0'. The $\overline{CS}$ signal of the last column is not connected to the first column pre-charge control, because it is not necessary. As stated above, for the transition from a row to the next one, the functional mode is restored for one clock cycle, making the first column ready to be accessed for a read/write operation, and avoiding faulty cell swaps in the other columns.

We have studied the effect of the modified pre-charge logic and we have found that it has little or no effect on the memory performance during normal operation. The switching between the functional mode and the low power test mode is achieved by a multiplexer implemented by two transmission gates (Figure 8). When the functional mode is selected, one of the transmissions gates (on the right of the pre-charge control element, Figure 8) allows signal Pr_j to drive the pre-charge circuit. We have chosen to use transmission gates (two transistors), instead of a single pass transistor, in order to ensure the minimum delay in the transitions ($0\rightarrow1$ and $1\rightarrow0$) of the Pr_j signal during the normal functional mode, as well as the CS_{j-1} signal during low power test mode.

The proposed method assumes 'word line after word line' addressing sequence. It should be noted that there are algorithms that require different addressing sequence or that rely on normal operation power consumption [15, 17, 19, 20]. In order to run properly these algorithm, the normal function mode can be selected and all the normal condition of the memory are restored, in particular the normal power consumption and the possibility to use any possible addressing sequence.

5 EXPERIMENTAL RESULTS

We first analyze (Subsection 5.1) the sources of power consumption in the normal (without the test power awareness) and proposed test scenario. Next, based on this analysis we show how the power dissipation is computed for bit-oriented (Subsection 5.2) and word-oriented (Subsection 5.3) SRAM memories.

5.1 Power analysis

Our analysis shows that there are five main sources of power dissipation during test:

1. Pre-charge circuits. Apart from the selected columns, all pre-charge circuits are ON in the functional mode (Figure 1), while in low power test mode the number of pre-charge circuits that are ON is equal to the number of selected columns (only one in the case of bit-oriented memories, Figure 4).

2. Array row transition. The activation of the normal mode, for one clock cycle at the row transition, involves significant power dissipation, due to the restoration at VDD voltage level of 50% of all the bit lines in the unselected columns of the array. This is because in the unselected columns one of the two bit lines is driven to '0' by the indirectly selected cells (Figure 6a). Even though this event involves significant power dissipation, its impact on the average power per clock cycle is reduced because of its infrequent occurrence. This line is charged and discharged only once for each row transition, thus its frequency is very low:

$$F(\text{Row transition}) = \frac{1}{(\#\text{March element operations}) \cdot (\#\text{memory columns})}$$

Considering a bit-oriented memory with a structure of 512 columns, where we perform a March element, composed by one operation, there is a row transition once for each 512 (=512*1) clock cycles. For a four operations element there is one row transition every 2048 (=512*4) clock cycles. Due to its low occurrence the average power increment per clock cycle can be neglected.

3. Driver of signal LPtest (Figure 8). The line that carries this signal has the same equivalent capacitance of a word line, because it has the same length and it drives the same number of MOS transistors. This line is charged and discharged only once for each row transition, thus its frequency is very low (see point 2) and therefore its contribution to the average power per clock cycle that it brings can be neglected.

4. Read Equivalent Stress consumption. In functional mode, all the cells on the row of the selected cells are indirectly selected and undergo RESs. In low power test mode, the number of cells undergoing a RES is equal to the number of selected columns (one in the case of bit-oriented memories). These cells are placed in the columns immediately after the selected ones. We have performed Spice simulations indicating that the cell power dissipation during a RES is approximately three orders of magnitude smaller than the pre-charge power dissipation during the

RES. Consequently the cell power dissipation can be neglected in the computation of the overall power dissipation.

5. Modified pre-charge control logic. The gates used to realize this logic are designed with minimal dimensions because their output load is very low. The capacities driven by these gates are about three orders of magnitude smaller than a single bit line capacitance. Moreover, there is only one control element switching for each column changing. For these reasons, the contribution of the new control elements to the overall power dissipation can be considered negligible.

Based on the previous analysis, it can be concluded that the power dissipation reduction depends on the memory array organization (#row and #col) and on the March algorithm that is being run (#elements and # operations per element). Also the number of read (#read) and write (#write) operations of the algorithm is important in the computing, because the power dissipation of a read action is lower than that of a write action. The power reduction per operation given by the method is independent on the type of performed operation (read or write).

5.2 Bit-oriented SRAM

The power dissipation during functional and low power test mode in the case of bit-oriented memories is computed. The average power dissipations per clock cycle during functional mode and low power test mode (respectively $P_{F, BO}$ and $P_{LPT, BO}$) are:

$$P_{F,BO} = \frac{\#\text{read} \cdot P_r + \#\text{write} \cdot P_w}{\#\text{operations}}$$

$$P_{LPT,BO} = P_{F,BO} - \left((\#\text{col} - 2) \cdot P_A - \frac{\#\text{row} \cdot (\#\text{col} - 1) \cdot \#\text{elements}}{\#\text{row} \cdot \#\text{col} \cdot \#\text{operations}} \cdot P_B - \frac{\#\text{row} \cdot \#\text{elements}}{\#\text{row} \cdot \#\text{col} \cdot \#\text{operations}} P_C \right)$$

where P_r denotes the memory power consumption during a read operation. P_w is the memory power consumption during a write operation. P_A is the power consumption of one pre-charge circuit for a single column restoration, $V_{BL} = V_{BLB} = VDD$. This parameter is proportional to the length of the bit lines, *i.e.* with the number of cells per column. P_B is the power consumption of a column restoration during the row transition, $V_{BLi} = V_{BLBi} = VDD \ \forall i \in \{0, 1, 2, \ldots, m-1\}$. This parameter is proportional

to length of the column and the number of columns per row. P_C is the power consumption of the LPtest signal driver.

The second equation can be simplified as follows:

$$P_{LPT,BO} = P_{F,BO} - \left((\#col - 2) \cdot P_A - \frac{\#elements}{\#operations} \cdot P_B \right)$$

because $P_C << P_B$ and it is multiplied by a coefficient hundreds times lower than P_B. We define the Power Reduction Ratio (PRR_{BO}) as

$$PRR_{BO} = 1 - \frac{P_{LPT,BO}}{P_{F,BO}}$$

To give insight into the test power reduction, we have run a set of well-known March tests in the functional and low power test modes, on a 512x512 0.13µm SRAM. We have chosen these algorithms, because they consist of different number of elements and operations. The Spice simulation results, with the following operational parameters (3ns clock cycle and 1.6V voltage supply), are shown in Table 1. The experimental results show that this method leads to a significant reduction in terms of overall power consumption (~50%) for the considered SRAM memory.

5.3 Word-oriented SRAM

The proposed method can be employed in word-oriented SRAM memories. The modified control logic (Figure 8) is the same as for bit-oriented memories, but due to the multiple cells selection the structure of the memory is different. Consequently also the power reduction that the method ensures is different. To compute the power dissipation during functional and test mode in the case of word-oriented SRAM, it is necessary to take into account other parameters. In word-oriented memories, the columns that are selected for the read/write operation are more than one. Normally, embedded word-

oriented memories are programmed to operate with different word lengths. One structure that allows this flexibility is characterized by a memory arrays divided in blocks. We propose as an example a four-block SRAM (Figure 9), with four columns for each block. Each row (word line) includes four 4-bits words. The column selection is operated by pre-decoders and multiplexers. The read operation is made by a sense amplifier (*SA* in Figure 9) and the write operation is made by Write Driver (*Wr Dr* in Figure 9). When a read or write operation is performed, a word line is activated and one cell for each block is selected, *e.g.* the cell in the first column of each block. At block level, the column selection is done by multiplexers. Most of embedded SRAMs are organized in standard rectangular arrays, whose number of rows and columns is fixed while the number of bits of the word can be chosen in relation with the application and the compatibility with the devices connected to the memory. This flexibility is allowed in memory composed by blocks. The number of bits of the word can be set by fixing the number of levels of multiplexers for the column selection. Consider a 8kx32 SRAM, organized as an array of 512 rows x 512 column, ordered in 128 blocks, with four columns per block. This memory can be programmed to work with maximum word length of 128 bits (four words per row). The memory can be programmed to work with shorter word length and in this case more levels of multiplexers are needed for the column selection. Irrespectively of the word length, the read operation is always performed in 128 columns, *i.e.* the number of blocks. The selection is similar in case of write operation.

For the application of the method, while for bit-oriented SRAMs only a column at a time is selected, and only one column needs to be pre-charged for the next operation, in word-oriented memories with block organization one column is selected for each block, and one column per block needs to be pre-charged for the next operation. This means that the number of columns where the pre-charge circuit can be switched off during test mode is smaller than in bit-oriented memories. The power dissipations per clock cycle during functional mode and low power test mode (respectively $P_{F,}$

$_{WO}$ and $P_{LPT, WO}$) are:

$$P_{F, WO} = \frac{\#\,read \cdot P_r + \#\,write \cdot P_w}{\#\,operations}$$

and

$$P_{LPT, WO} = P_{F, WO} - \left((\#\,col - 2 \cdot \#\,blocks) \cdot P_A - \frac{(\#\,col - 2 \cdot \#\,blocks) \cdot \#\,elements \cdot \#\,w\_bits}{\#\,operations \cdot \#\,col} \cdot P_B \right)$$

where #w_bits is the number of bit of one word; #blocks is the number of block in the memory array; P_r, $P_{w,}$ P_A and P_B have been described in the previous sub-section. Note that we have presented the above equation already simplified.

The equation to calculate the Power Reduction Ration (PRR_{WO}) for word-oriented memories is:

$$PRR_{WO} = 1 - \frac{P_{LPT, WO}}{P_{F, WO}}$$

To give insight into the PRR_{WO} in the case of word-oriented SRAM, we have run a set of well-known March tests in the functional and low power test modes, on a 8kx32 0.13µm SRAM, 512 rows x 512 columns, with array organized in 128 blocks, 64 blocks and with word length of 16 bits and 8 bits. These configurations are the most suitable for this kind of embedded memory. The Spice simulation results, using the same operational parameters described above (3ns clock cycle and 1.6V voltage supply), are shown in Table II. The first column of the table provides the different March tests run in the simulations. Columns two and three give the number of elements and operation of each algorithm. In the remaining columns the values of the PRR_{WO} for the different memory configurations are presented: 128 and 64 blocks, with 16 and 8 bits words. To facilitate the interpretation of the results, the experimental data of Table II are shown in the histogram of Figure 10.

The analysis of the experimental data for word-oriented memories shows that the test power reduction is inversely proportional to the number of blocks. This is because of the fact that for each block there is always one column active, independently of the length of the word. A higher number of active columns involves a higher number of columns that need to be prepared for the next operation, leaving a reduced number of columns where the pre-charge circuit can be turned off. The test power reduction is also inversely proportional to the number of bits in a word. This is because the larger the word length is, the more frequent the row transitions are, leading to high power consuming global bit line restorations.

To summarize the main results of the proposed test technique, we can observe a significant reduction in terms of overall power consumption for both bit-oriented (~50%) and word-oriented (22% up to 35%) SRAMs. The test power reduction in bit-oriented memories is higher than in word-oriented memories. For each operation in word-oriented memories, different locations (cells/columns) are selected a time, consequently the number of columns where the pre-charge circuits can be turned off is reduced, and thus power reduction is lowered. The reduced performance of the application in word-oriented memories is compensated by the fact that in these devices the quantity of data in input/output is a multiple of that of a bit-oriented one. We have validated our technique with extensive simulations on 8kx32 0.13µm SRAMs. We believe that this technique can be applied to other SRAMs achieving good results, because it always ensures a high reduction of the pre-charge dissipation, which, irrespectively of the structure, represents up to 70%-80% of the overall power consumption of SRAM memories, as demonstrated in [13].

6 FUTURE WORK

In our future work we aim to address the two points. As mentioned in Section 3, the row transition is a sensitive moment of the application of the method. In order to prevent faulty swap of the cells in

the next selected row, we have proposed to activate the functional mode for a clock cycle, in order to charge all the bit lines at VDD. This solution presents the limitation of a high drain of current in a short time and it may provoke side phenomena. The second point concerns the fact that during the test time most of bit lines are floating because the pre-charge circuits are OFF. In this condition, the bit lines may be more prone to crosstalk effects and remotely influence the contents of the cells that are indirectly selected. The authors intend to complete this study by investigating the points given above and to extend the proposed method to DRAMs and other types of memories.

7 CONCLUSION

In this work we have presented a method that minimizes the test power in SRAM memories by reducing the pre-charge activity. This was achieved by exploiting the fact that the addressing sequence during test is predictable, and hence only two columns need to be pre-charged in each clock cycle. We have implemented this low power test mode by using a modified pre-charge control logic. Spice simulations used to validate the proposed method show significant power reduction during test for bit-oriented and word-oriented SRAM memories. It has been shown that the effect of the modified pre-charge logic on the normal functional mode is negligible.

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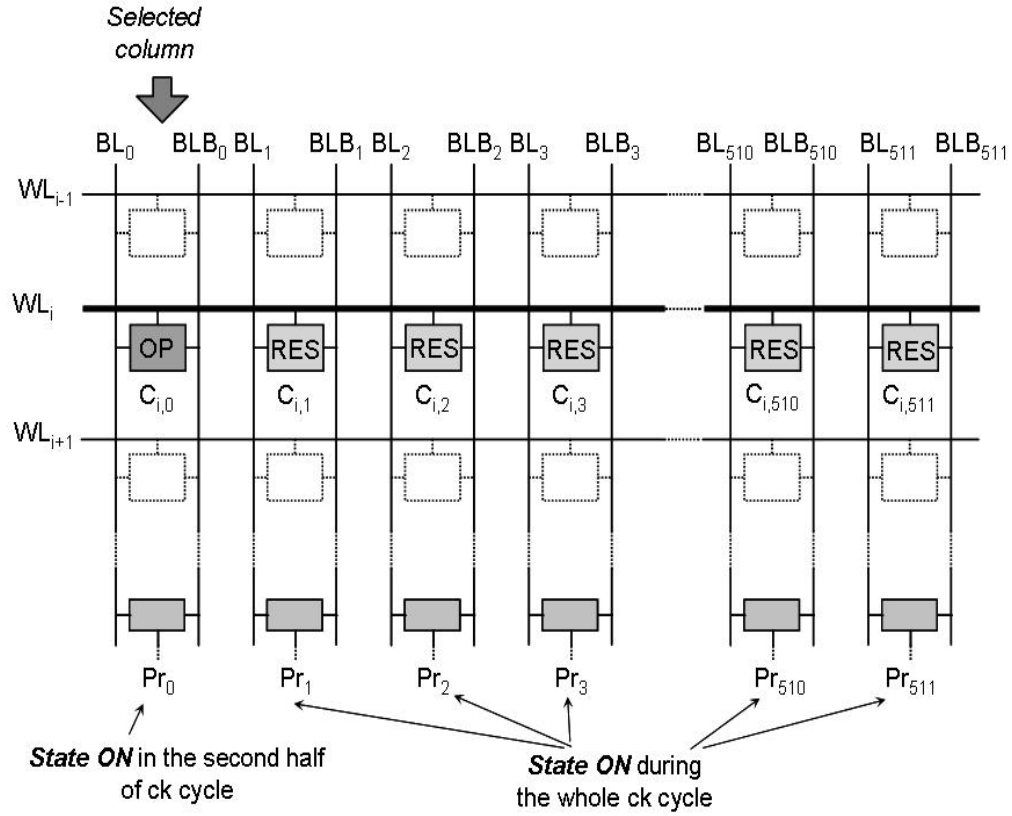

Figure 1. Functional mode of an SRAM array

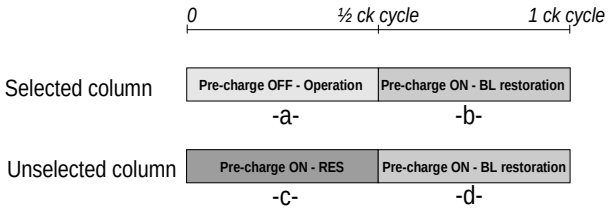

Figure 2. Pre-charge action for a selected and an unselected column

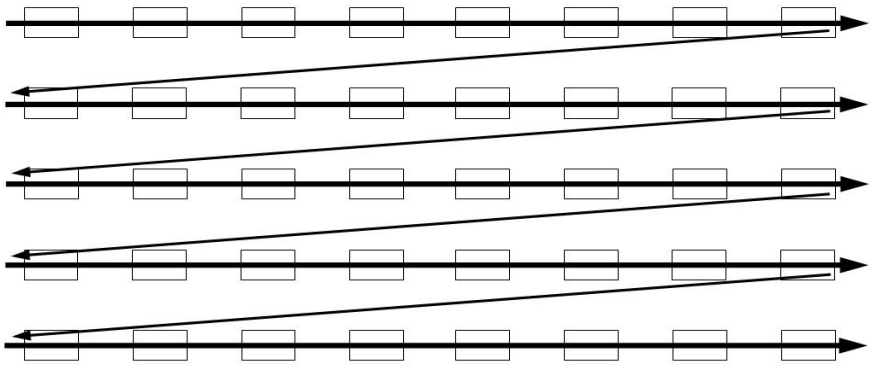

Figure 3. Access order "word line after word line"

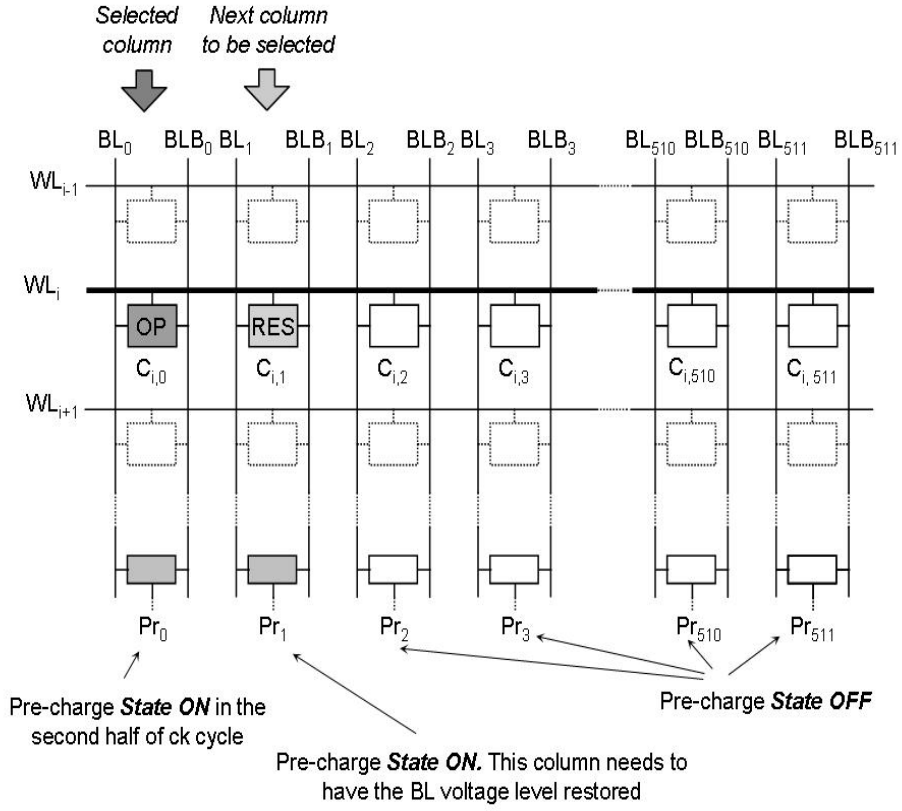

Figure 4. Proposed pre-charge activation

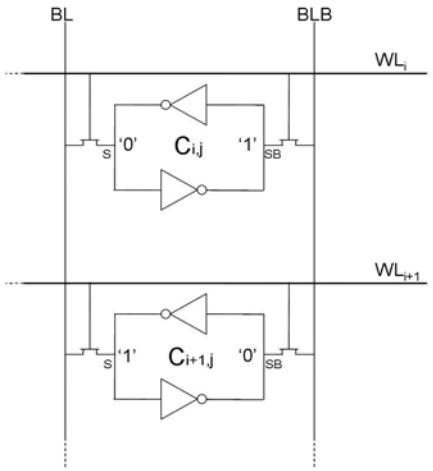

Figure 5. Scheme of interaction between unselected cells and bit lines

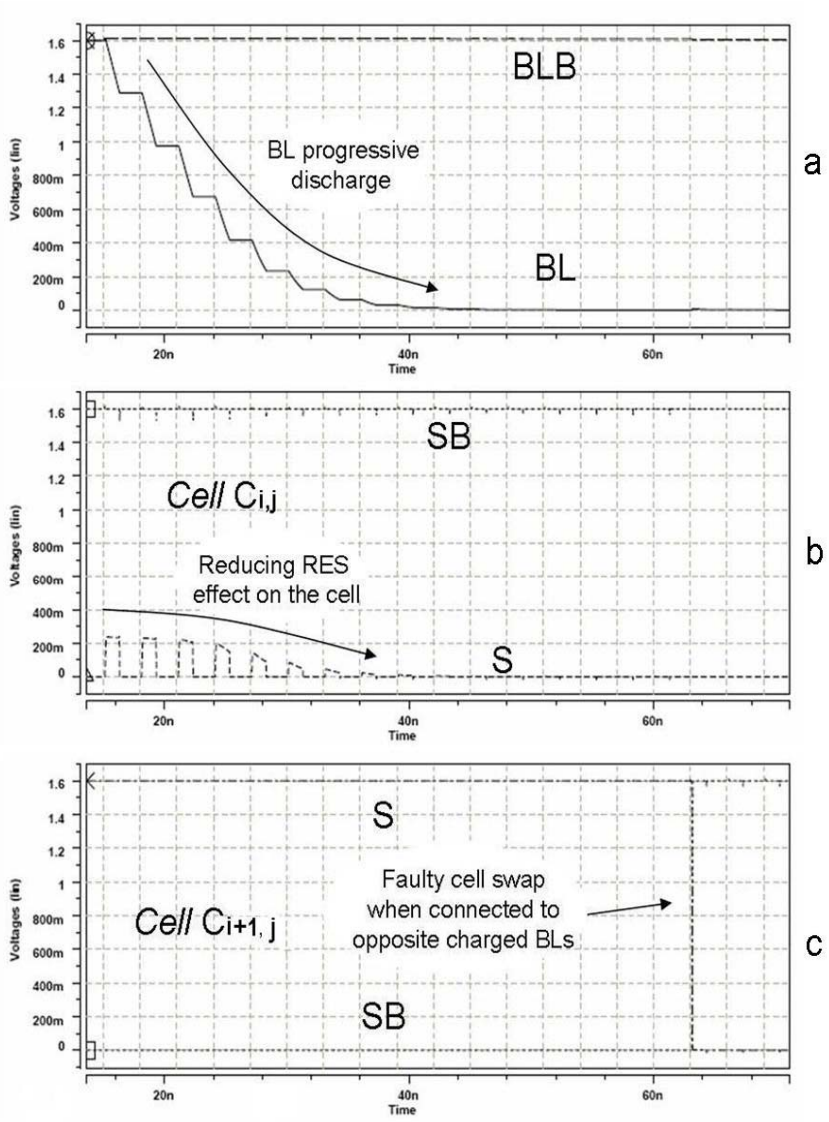

Figure 6. Spice simulations of the interaction between unselected cells and bit lines

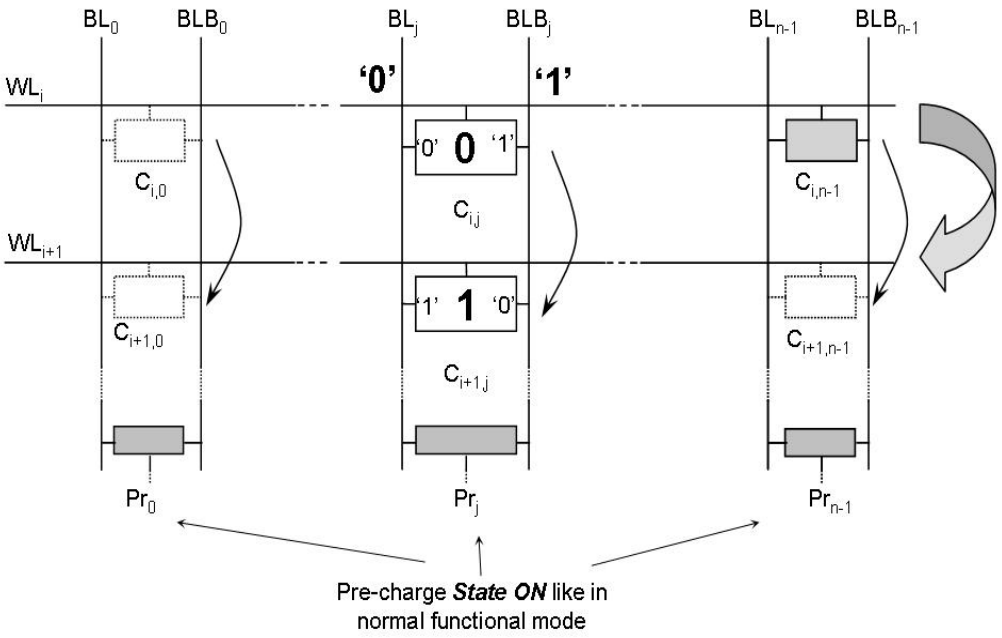

Figure 7. Preserving faulty cell swap during row transition

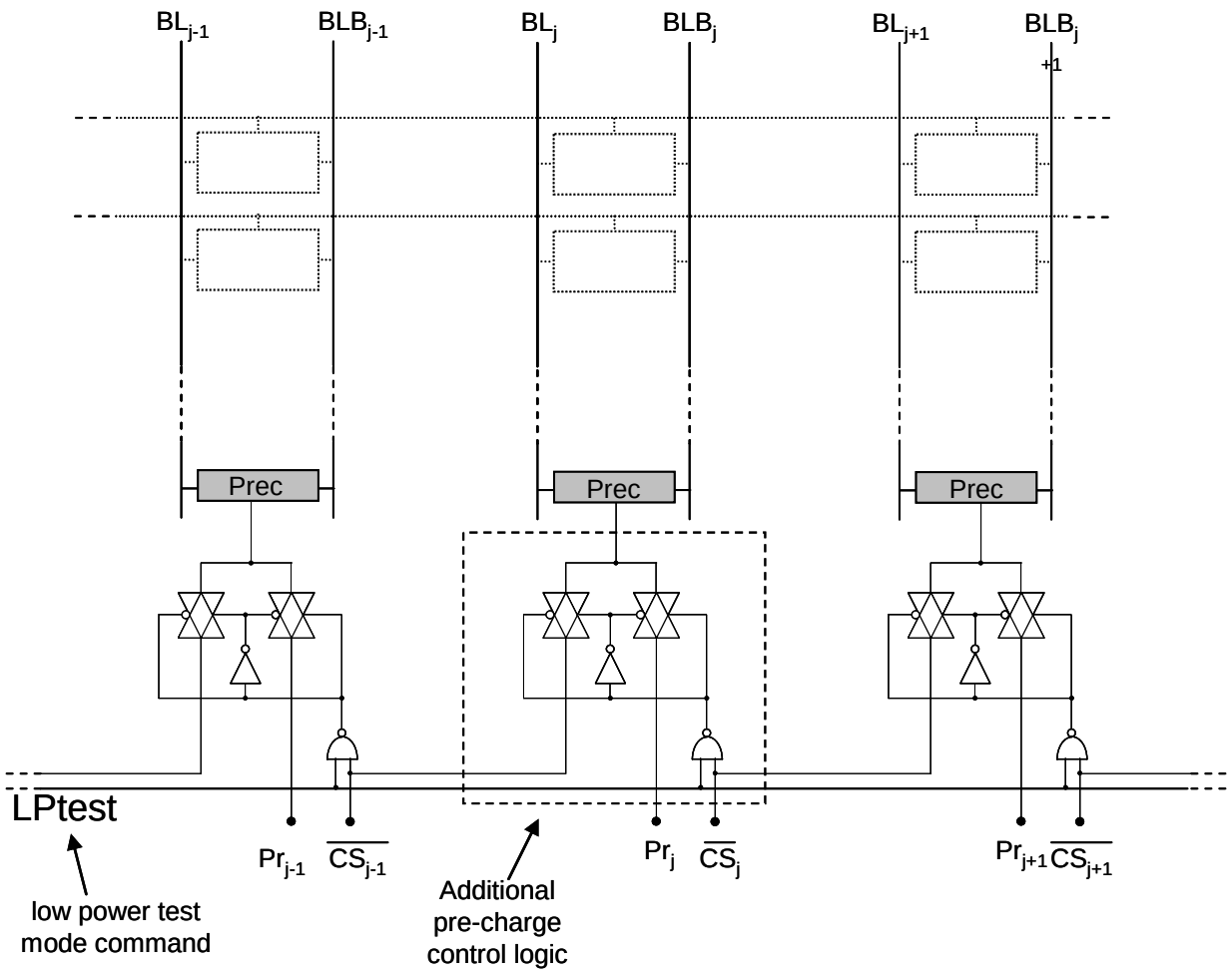

Figure 8. The modified pre-charge control logic

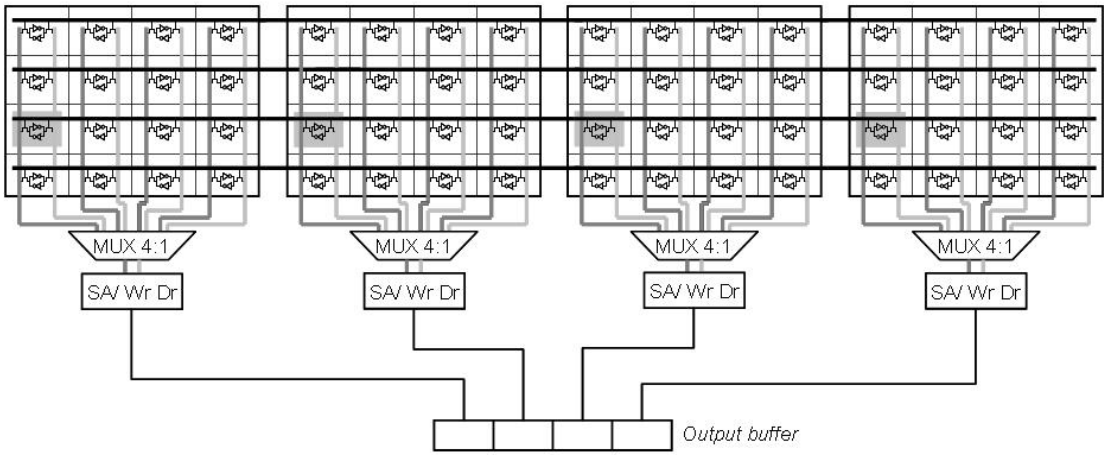

Figure 9. Example of four blocks configuration SRAM

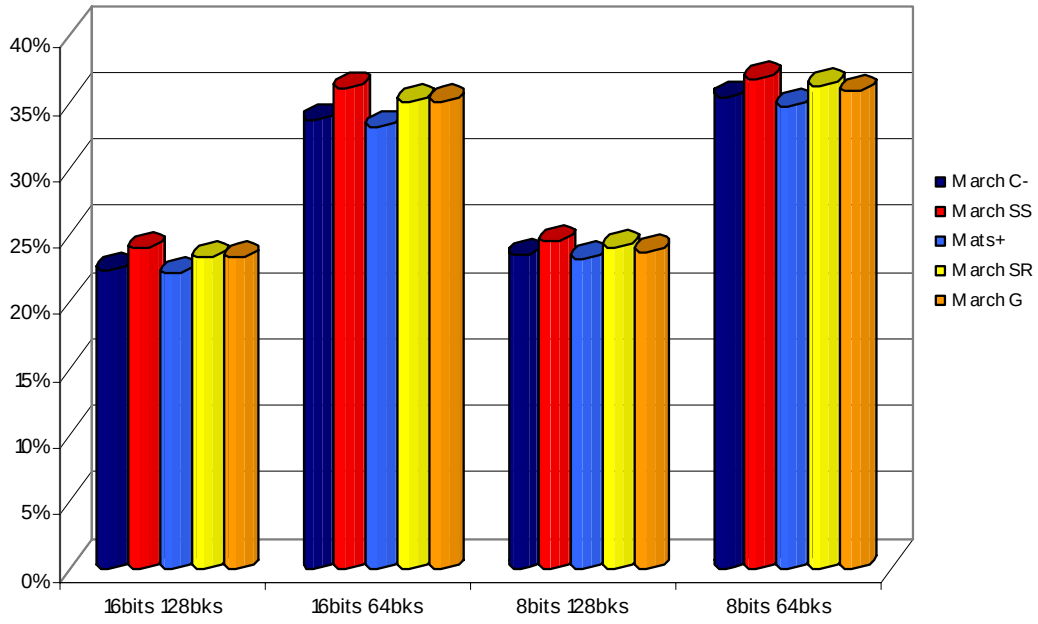

Figure 10. PRR for different algorithms and different configurations of 8kx32 SRAM

TABLE I
BIT-ORIENTED SRAM: PRR FOR DIFFERENT MARCH ALGORITHMS

Algorithm	# elm	# oper	# read	# write	PRR_{BO}
March C-	6	10	5	5	47.3 %
March SS	6	22	13	9	50.0 %
Mats+	3	5	2	3	48.1 %
March SR	6	14	8	6	49.5 %
March G	7	23	10	13	50.5 %

TABLE II
WORD-ORIENTED SRAM: PRR FOR DIFFERENT ALGORITHMS AND DIFFERENT CONFIGURATIONS OF 8KX32 SRAM

Algorithm	#elem	#oper	#read	#write	PRR 16 bits WO 128 blocks	PRR 16 bits WO 64 blocks	PRR 8 bits WO 128 blocks	PRR 8 bits WO 64 blocks
March C-	6	10	5	5	22.4%	33.6%	23.5%	35.3%
March SS	6	22	13	9	24.0%	36.0%	24.5%	36.7%
Mats+	3	5	2	3	22.1%	33.1%	23.2%	34.7%
March SR	6	14	8	6	23.3%	35.0%	24.1%	36.2%
March G	7	23	10	13	23.3%	35.0%	23.8%	35.8%

BIOGRAPHIES

Luigi Dilillo

Luigi Dilillo received his degree in Electrical Engineering in 2001 from Politecnico di Torino (Italy) and the PhD from in Microelectronics from the Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM) in France. He is postdoctoral research-fellow at University of Southampton. His researches include MEMS, digital circuits and test. At this moment he is working on memory testing with thermal and power constraints.

Paul Rosinger

Paul Rosinger received the B.Sc. in Computer Science from the Technical University of Timisoara, Romania, in 1999, and the Ph.D. in Electronics and Computer Science from the University of Southampton, United Kingdom, in 2003. He is now a postdoctoral research-fellow at Southampton University. His current research interests include testing of digital systems, low power embedded systems and reconfigurable architectures.

Bashir M. Al-Hashimi

Bashir M. Al-Hashimi is a Professor of Computer Engineering at the School of Electronics and Computer Science, University of Southampton, UK. He is the Editor-in-Chief of the IEE Proceedings: Computers and Digital Techniques. He is a Fellow of the IEE. Professor Al-Hashimi is the General Chair of the 11th IEEE European Test Symposium (Southampton 2006), and the General Chair of DATE Friday Workshops (2005 and 2006). He was the co-author of the James Beausang Best Paper Award at the 2000 IEEE International Test Conference relating to low power BIST for RTL data paths.

Patrick Girard