Multilevel generalised low-density parity-check codes

R.Y.S. Tee, F.C. Kuo and L. Hanzo

Multilevel coding invoking generalised low-density parity-check component codes is proposed, which is capable of outperforming the classic low-density parity check component codes at a reduced decoding latency.

Introduction: Multilevel coding (MLC) was proposed by Imai and Hirawaki [1] as a bandwidth-efficient coded modulation scheme designed for protecting each bit of a non-binary symbol with the aid of binary codes, while maintaining different target bit error rates (BERs). Parallel independent decoding (PID) [2] is employed as an efficient decoding strategy with reduced decoding delay, where there is no information exchange across the different protection classes.

MLC schemes may be constructed using different component codes. Recently, classic low-density parity-check (LDPC) codes [3] have been commonly used as component codes [4] owing to their flexible code rates and good BER performance. Belief propagation (BP) [3] may be used for iterative soft decoding at each different BER protection level. Against this background, we propose a novel MLC design using generalised LDPC (GLDPC) codes rather than classic LDPC codes [5] as component codes, which has the benefit of an improved BER performance and an implementationally attractive shorter parallel decoding structure.

As a benefit of their block-based nature and random generator matrix construction, no channel interleaver is required for LDPC or GLDPC component codes. For our GLDPC codes, instead of using Gallager's single-error detecting parity-check code [3], we employ binary BCH error-correcting codes [6] as the constituent codes. Simple iterative soft-input soft-output (SISO) decoders [6] are used for each constituent BCH code of the MLC scheme. We invoke both inner iterations within the LDPC/GLDPC component codes and outer iterations exchanging information between the LDPC/GLDPC block codes and the demapper, as shown in Figs. 1 and 2. Gray mapping (GM) of the bits to modulated symbols is used for non-iterative decoding, while set partitioning (SP) based mapping is used for iterative decoding, because it provides improved iteration gains.

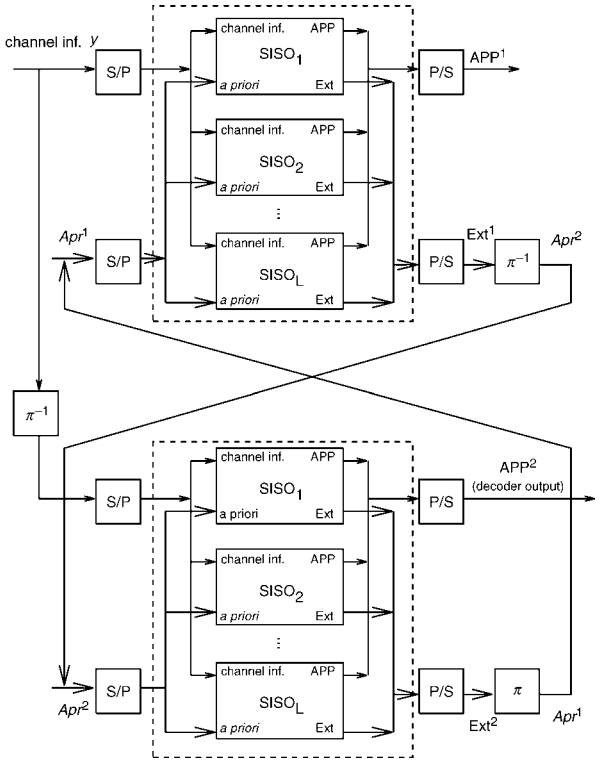

Fig. 1 *SISO BCH decoder of GLDPC component code*

Multilevel GLDPC: We propose an MLC invoking GLDPC component codes [5] having a parity-check matrix (PCM) with binary BCH codes $C_0(n, k)$ as the constituent codes. The PCM was constructed with the aid of J GLDPC superblocks. We opted for using $J=2$, since it results in a high minimum distance [5], despite its low decoding complexity. The $J=2$ superblocks are defined by two PCMs, which satisfy $H^2=\pi H^1$, where H^1 and H^2 denote the matrices of the first and second superblock, respectively, while π represents a pseudorandom permutation. This code construction requires $L=N/n$ constituent codes, where N denotes the total coded block length.

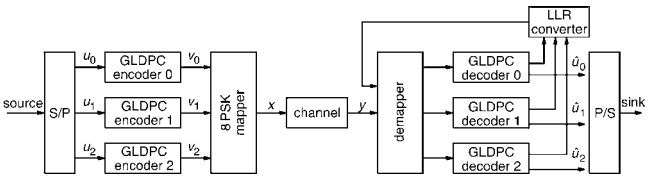

Fig. 2 *System model of MLC/PID using iteratively detected GLDPC inner codes as well as outer iterations, where u_i denotes source bit i and v_i denotes coded bits i*

Decoded output bits represented by $\hat{u}_i$
Iterative GLDPC decoder is seen in Fig. 1

Each BCH constituent code of the first GLDPC superblock shown in the upper half of Fig. 1 has an associated SISO decoder and the BCH constituent codes are decoded in parallel, before the resultant extrinsic information is fed into the second interleaved GLDPC superblock portrayed at the bottom of Fig. 1. The substantial implementational benefit of this is that a number of cost-efficient, low-speed parallel SISO decoders may be used instead of a single high-speed decoder. The reduced processing block length of a constituent BCH SISO decoder is equivalent to N/n, as opposed to N in an LDPC or turbo constituent decoder.

Fig. 1 shows the L number of SISO decoders of the L constituent BCH codes. Since we have $J=2$ GLDPC superblocks, the channel's output information y is fed directly into the L number of parallel BCH SISO decoders of the first GLDPC superblock, while deinterleaving the block π^{-1} into the second GLDPC superblock of Fig. 1. The extrinsic outputs Ext^1 of the first superblock's SISO decoders are deinterleaved and used as *a priori* information Apr^2 for each of the BCH constituent decoders of the second GLDPC superblock in Fig. 1. During the next inner iteration, the extrinsic information Ext^2 arriving from the second superblock is used as the *a priori* information Apr^1 for the BCH constituent decoders of the first GLDPC superblock of Fig. 1, as in classic turbo detectors [6].

Modulation and demodulation: Fig. 2 shows the MLC/PID system model, employing the iterative GLDPC scheme of Fig. 1 for each MLC protection class and having an additional outer decoding loop. A 3 bit/symbol encoded data is transmitted using 8-PSK modulation. Both an iterative and a non-iterative scheme are studied and Gray mapping is employed in the non-iterative scheme, where the parallel decoding of the three bits is implemented without outer iterations. However, for the sake of achieving an outer iteration gain in the decoder of our scheme, we also propose an iterative scheme employing SP based mapping [6].

Since the *a priori* information $\hat{\boldsymbol{u}}$ fed to the demapper of Fig. 2 is not equiprobable after the first outer iteration, the achievable iteration gains may be expected to increase by efficiently exploiting the *a priori* probabilities, provided that an appropriate mapping scheme is used. The extrinsic probability expression P_e of the MLC demapper of Fig. 2 providing new information for enhancing our confidence in y was given by [7].

With the aid of the so-called equivalent capacity rule [2], we obtain the desired code rate of each component for 8-PSK modulation using Gray mapping, yielding $R_0/R_1/R_2=0.510/0.745/0.745$. Given that the total number of uncoded input bits is k_i and the total number of channel coded output bits is n_i for the GLDPC encoder at the ith MLC protection level, the coding rate of the ith GLDPC component code is $R_i=1-J(1-k_i/n_i)$ [5]. The overall effective throughput of the system is therefore 2 bits/symbol. The BCH constituent codes employed in our scheme are $C_0(20,15)$, $C_1(48,42)$ and $C_2(48,42)$.

Simulation results: The proposed MLC/PID GLDPC scheme using 8-PSK modulation was investigated, when communicating over both AWGN and uncorrelated Rayleigh fading channels. We employed ten

GLDPC-BCH inner iterations, a single outer iteration using Gray demapping and six outer iterations employing SP mapping in our scheme. Fig. 3 shows that at BER $= 10^{-5}$, the proposed scheme demonstrates an E_b/N_0 improvement of around 0.5 dB in AWGN channels compared to our MLC-LDPC benchmarker system. More explicitly, we used the following rate 0.51, 0.745 and 0.745 LDPC codes as the GLDPC component codes: LDPC(1800,918), LDPC(1800,918) and LDPC(1800,1341), respectively. Both codes were decoded by the same PID scheme and again the proposed MLC-GLDPC code was constructed from the short, and hence implementationally more convenient, BCH constituent codes $C_0(20,15)$, $C_1(48,42)$ and $C_2(48,42)$, respectively. When employing SP based mapping and six outer iterations over AWGN channels, both systems achieve a further 2–2.5 dB performance improvement and the proposed MLC-GLDPC scheme retains its performance advantage. When communicating over uncorrelated Rayleigh fading channels, our MLC-GLDPC scheme outperforms the MLC-LDPC benchmarker by about 1 dB in both the single outer iteration Gray mapping and the six outer iteration aided SP based scenarios at BER $= 10^{-5}$. This might appear to be a modest gain, but it is achieved with the aid of a more convenient parallel architecture.

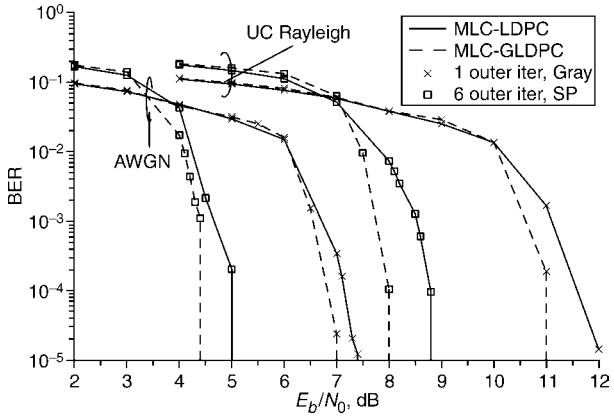

Fig. 3 *BER of both MLC-GLDPC and MLC-LDPC over AWGN channel and uncorrelated (UC) Rayleigh fading channel invoking $I_{outer} = 1$ or 6 outer and $I_{inner} = 10$ inner iterations*

Effective throughput 2 bits/symbol and BCH codes (20,15), (48,42) and (48,42) schemes, respectively

We now extend these investigations to the uncorrelated Rayleigh fading channel where both schemes invoke the same number of $I_{outer} = 6$ outer iterations. The MLC-GLDPC scheme achieves a coding advantage of 2 dB compared to the MLC-LDPC scheme at BER $= 10^{-5}$, when invoking $I_{inner} = 5$ inner iterations, as shown in Fig. 4. This coding advantage is reduced to about 1 dB when $I_{inner} = 8$ inner iterations are employed.

Conclusions: MLC GLDPC schemes are proposed. Our simulations results suggest that the attainable SNR improvement compared to a random LDPC component code based MLC benchmarker ranged between 0.5 and 2 dB, which was achieved using the same number of iterations and an implementationally beneficial parallel architecture. Multilevel Gray mapping combined with parallel decoding and dispensing with turbo/channel interleavers is attractive in low-latency real-time services, such as lip-synchronous wireless video telephony, where employing low complexity parallel decoding in the context of short BCH block constituent codes may become paramount.

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