

Combined Serially Concatenated Codes and MMSE Equalization: an EXIT Chart Aided Perspective

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Abstract—Iterative Minimum Mean Square Error (MMSE) equalization and channel decoding is appealing, since it exhibits a lower complexity than maximum *a posteriori* (MAP) turbo equalization. However, the MMSE equalizer's attainable performance is upper-bounded by that recorded for transmission over the coded AWGN channel, a phenomenon usually referred to as "error shoulder". In order to circumvent this performance limitation, we propose a three-stage concatenated transceiver constituted by inner and outer coding as well as MMSE equalization, which achieves significant iteration gains, despite using low-complexity serially concatenated memory-1 convolutional codes. It is demonstrated that this three-stage scheme outperforms the traditional two-stage MMSE turbo equalization scheme above a certain E_b/N_0 threshold. Furthermore, the convergence behavior of the proposed scheme is analyzed with the aid of 3D EXtrinsic Information Transfer (EXIT) charts and their 2D projections, leading to a number of practical iterative receiver design guidelines.

I. MOTIVATION

Turbo equalization [1] is an effective means of eliminating the channel-induced Inter-Symbol Interference (ISI) imposed on the received signal, hence the achievable performance may approach that recorded over the non-dispersive AWGN channel. When a simple rate-1 precoder is applied before the modulator, which renders the channel to appear recursive to the receiver, the attainable performance may be further improved [2], [3].

The soft-in/soft-out (SISO) Minimum Mean Square Error (MMSE) equalizer [4], which is capable of utilizing *a priori* information from other SISO modules such as a SISO channel decoder and generating *extrinsic* information, forms an attractive design alternative to the maximum *a posteriori* (MAP) equalizer owing to its lower computational complexity. This is particularly so for channels having long Channel Impulse Responses (CIRs) [4], [5]. The precoder can be readily integrated into the shift register model of the ISI channel [3], and may be modelled by combining its trellis with the trellis of a MAP/Soft Output Viterbi Algorithm (SOVA) based equalizer. However, the precoder's trellis-description cannot be directly combined with the model of an MMSE equalizer. Hence, the achievable performance of MMSE turbo equalization is potentially limited [4], [5].

EXtrinsic Information Transfer (EXIT) [6] charts have been proposed for analyzing the convergence behavior of iterative decoding schemes, which indicate that an infinitesimally low Bit-Error Rate (BER) may only be achieved by an iterative receiver, if an open tunnel exists between the EXIT curves of the two SISO components. Recently, both the convergence analysis and the best activation order of the component codes has been studied in the context of

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multiple-stage concatenated codes [7], [8], which generally require the employment of three-dimensional (3D) EXIT charts. For the sake of simplifying the associated analysis, a 3D to 2D EXIT chart projection technique was proposed in [7], [8]. It has been shown [5] that the EXIT curve of an MMSE equalizer intersects with that of the channel decoder, before reaching the decoding convergence point of (1,1), hence residual errors persist after turbo equalization. However, it is natural to conjecture that there might exist an open tunnel leading to the convergence point in the 3-D EXIT chart of a well-designed three-stage SISO system.

Against this backdrop, in this paper we propose a combined serially concatenated channel coding and MMSE equalization scheme, which is capable of achieving a precoding-aided convergence-acceleration effect for a MAP/SOVA equalizer. Moreover, the convergence behavior of the proposed scheme is investigated with the aid of the 3D to 2D EXIT chart projection technique developed in [7], [8], and further design guidelines are derived from an EXIT-chart perspective. For illustration and comparison purpose, let us start with the traditional two-stage turbo equalization schemes.

II. TURBO EQUALIZATION USING MAP/MMSE EQUALIZERS

A. System model

Fig. 1 shows the system model of a classic turbo equalization scheme. At the transmitter, a block of length L information data bits u_1 is encoded by a channel encoder first. After channel coding, the coded bits c_1 are interleaved yielding the data bits u_2 and are either directly fed to the bit-to-modulated-symbol mapper or they are first fed through a rate-1 precoder and encoded for producing the coded bits c_2 , as seen in Fig. 1. After mapping, the modulated signal x is transmitted over a dispersive channel contaminated by AWGN n . At the receiver of Fig. 1, an iterative detection/decoding structure is employed, where extrinsic information is exchanged between the channel equalizer and the channel decoder in a number of consecutive iterations. To be specific, the channel equalizer processes two inputs, namely the received signal y and the *a priori* information $A(u_2)$ fed back by the channel decoder. Then the channel equalizer of Fig. 1 generates the *extrinsic* information $E(u_2)$, which is deinterleaved and forwarded as the *a priori* information to the channel decoder. Furthermore, the channel decoder capitalizes on the *a priori* information $A(c_1)$ provided by the channel equalizer and generates the *extrinsic* information $E(c_1)$, which is interleaved and fed back to the channel equalizer as the *a priori* information. Following the last iteration, the estimates \hat{u}_1 of the original bits are generated by the channel decoder, as seen in Fig. 1.

In our forthcoming EXIT chart analysis and Monte Carlo simulations, we assume that the channel is time-invariant and that the CIR

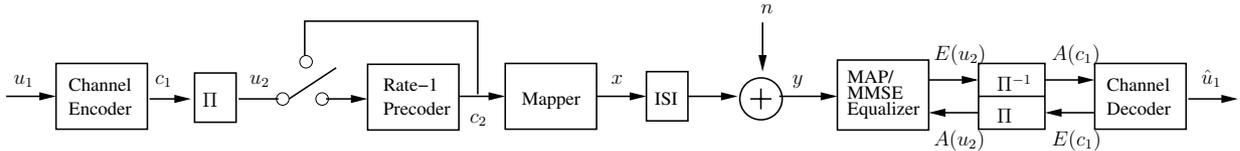


Fig. 1. Turbo equalization system using MAP/MMSE equalizer both with and without precoding. The system parameters are summarized in Table I.

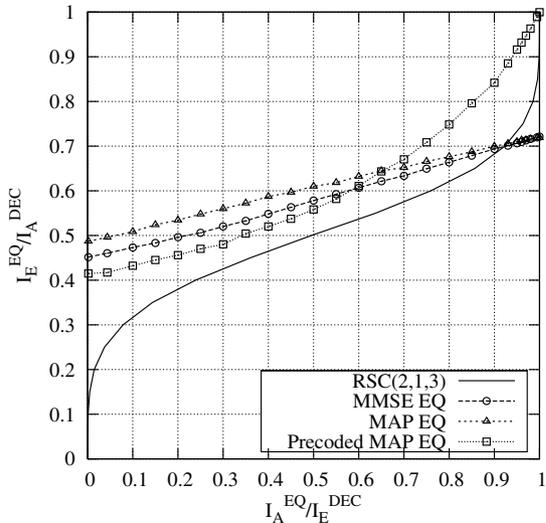


Fig. 2. EXIT charts for the iterative receiver using either an MMSE equalizer or a MAP equalizer, where the latter is investigated for both a non-precoded and a precoded channel at $E_b/N_0 = 3$ dB

is known at the receiver. To be specific, the three-path CIR of [9] described by

$$h[n] = 0.407\delta[n] + 0.815\delta[n-1] + 0.407\delta[n-2] \quad (1)$$

is used. We employ a constraint-length 3, half-rate Recursive Systematic Convolutional (RSC) code RSC(2,1,3) having the octally represented generator polynomials of (5/7), where 7 is the feedback polynomial and 5 is the feed forward polynomial. Then we use a simple rate-1 precoder described by the generator polynomials of $1/(1+D)$. Either MAP or MMSE equalization is invoked, but precoding is only combined with the MAP equalizer. For the sake of simplicity, BPSK modulation is used. Our system parameters are summarized in Table I.

TABLE I
SYSTEM PARAMETERS

Channel Encoder	RSC(2,1,3) Generator Polynomials (5/7)
Precoder	Generator Polynomials $1/(1+D)$
Modulation	BPSK
CIR	$[0.407 \ 0.815 \ 0.407]^T$
Block Length	$L = 4096$ bits

B. EXIT chart analysis

Fig. 2 depicts the EXIT functions of both the MAP/MMSE equalizers and the outer convolutional decoder. It is clear that the EXIT

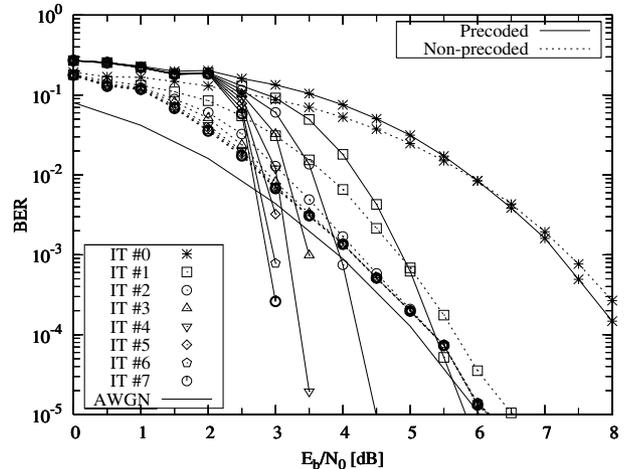


Fig. 3. BER performance of the iterative receiver using the MAP equalizer both with and without precoding

curves of both the MMSE equalizer and the MAP equalizer (without precoding) intersect with that of the outer RSC(2,1,3) decoder, before reaching the convergence point of $(I_A^{EQ} = 1, I_E^{EQ} = 1)$. Hence residual errors may persist, regardless of both the number of iterations used and the size of the interleaver. Furthermore, the MMSE equalizer generally outputs less extrinsic information than the MAP equalizer, resulting in a poorer performance. On the other hand, with the advent of precoding, the EXIT curve of the MAP equalizer becomes capable of reaching the convergence point, as seen in Fig. 2. We note however that there is a crossover between the EXIT curves of the precoded and non-precoded MAP equalizer, which implies that the non-precoded MAP equalizer would perform better in the low-SNR region, while the precoded MAP equalizer is capable of achieving an near error-free performance, provided that a sufficiently high number of iterations is performed. The convergence threshold of the precoded MAP equalizer is about 2.3 dB.

C. Simulation results

In order to verify the convergence prediction of the EXIT chart analysis outlined in Section II-B, Monte Carlo simulations were also performed and the corresponding BER results are depicted in Fig. 3. It can be seen that the BER performance of the precoded system becomes better than that of the non-precoded system at an E_b/N_0 of about 2.7 dB.

III. THREE-STAGE SERIALLY CONCATENATED CODING AND MMSE EQUALIZATION

A. System model

Simply incorporating an interleaver between the precoder and the signal mapper in the transmitter of Fig. 1 enables the receiver to

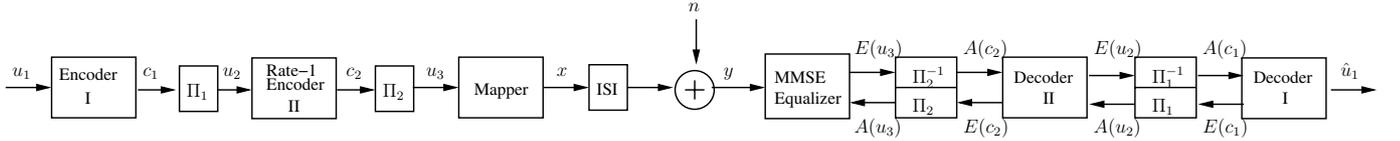


Fig. 4. System diagram of two serially concatenated code and MMSE equalization

perform iterative equalization/decoding by exchanging extrinsic information between three SISO modules, namely the MMSE equalizer, Decoder II and Decoder I of Fig. 4. Here, we would prefer not to refer to Encoder II as a precoder, since it cannot be directly combined with the equalizer at the receiver as in Fig. 1. The same three-path channel of Eq. (1) is used as in Section II. The length of the noncausal and the causal part of the MMSE filter are $N_1 = 5$ and $N_2 = 3$, respectively, resulting in an overall filter length of $N = N_1 + N_2 + 1 = 9$.

B. EXIT chart analysis

In the following, we will carry out the EXIT chart analysis of the three-stage system of Fig. 4. Similar to the two-stage system, the convergence SNR threshold of the three-stage system can be determined. At the same time, the outer code is optimized to give the lowest convergence SNR threshold. Finally, the activation order of the three SISO modules is optimized.

1) *Determination of the Convergence Threshold:* As seen in Fig. 4, Decoder II exploits two *a priori* inputs, namely, $A(c_2)$ and $A(u_2)$. At the same time, it generates two *extrinsic* outputs, i.e., $E(c_2)$ and $E(u_2)$. Hence, in order to describe the EXIT characteristics of Decoder II, we need the following two 2D EXIT functions [6], [7]:

$$I_{E(u_2)} = T_{u_2}(I_{A(u_2)}, I_{A(c_2)}), \quad (2)$$

$$I_{E(c_2)} = T_{c_2}(I_{A(u_2)}, I_{A(c_2)}). \quad (3)$$

By contrast, for the MMSE equalizer and Decoder I, only one *a priori* input is available in Fig. 4 and the corresponding EXIT functions are:

$$I_{E(u_3)} = T_{u_3}(I_{A(u_3)}, E_b/N_0) \quad (4)$$

for the equalizer and

$$I_{E(c_1)} = T_{c_1}(I_{A(c_1)}) \quad (5)$$

for Decoder I, where the second parameter of E_b/N_0 in Eq. (4) indicates that the extrinsic information also depends on the channel SNR. Hence two 3D EXIT charts are required for plotting all the EXIT functions, namely one for the EXIT functions of both Eq. (3) and Eq. (4) as shown in Fig. 5(a), and another for the EXIT functions of both Eq. (2) and Eq. (5) as shown in Fig. 5(b). Note that $I_{E(u_3)}$ of Eq. (4) is independent of $I_{A(u_2)}$, hence the MMSE equalizer's EXIT surface seen in Fig. 5(a) is generated by sliding its EXIT curve in the 2D EXIT chart of Fig. 2 along the $I_{A(u_2)}$ axis. The EXIT surface of Decoder I was generated similarly, as shown in Fig. 5(b), where $I_{E(c_1)}$ of Eq. (5) is independent of $I_{A(c_2)}$.

Let us first consider the extrinsic information exchange between the MMSE equalizer and Decoder II. Let l be the time index. Only one SISO module is invoked each time. Note that we have $I_A^{(l)}(c_2) = I_E^{(l-1)}(u_3)$, $I_A^{(l)}(u_3) = I_E^{(l-1)}(c_2)$. Considering Eq. (2), (3) and (4), for a given *a priori* information $I_A(u_2)$, we have

$$I_A^{(l)}(c_2) = T_{u_3}(T_{c_2}(I_A(u_2), I_A^{l-2}(c_2)), E_b/N_0), \quad (6)$$

with $I_A^{(0)}(c_2) = 0$ and

$$I_E^{(l)}(u_2) = T_{u_2}(I_A(u_2), I_A^{(l)}(c_2)). \quad (7)$$

The recursive equation of (6) actually represents an iteration, including the activation of both Decoder II and the MMSE equalizer. After a sufficiently high number of iterations, $I_A^{(l)}(c_2)$ and $I_E^{(l)}(u_2)$ will converge to a value between 0 and 1, which depends on the channel SNR and on the *a priori* input $I_A(u_2)$ only, i.e., we have

$$I_A(c_2) = \lim_{l \rightarrow \infty} I_A^{(l)}(c_2), \quad (8)$$

$$\begin{aligned} I_E(u_2) &= \lim_{l \rightarrow \infty} I_E^{(l)}(u_2) \\ &= T_{u_2}(I_A(u_2), \lim_{l \rightarrow \infty} I_A^{(l)}(c_2)). \end{aligned} \quad (9)$$

Hence the overall EXIT function of the combined module of the MMSE equalizer and Decoder II is a function of $I_A(u_2)$ and E_b/N_0 , which can be expressed as

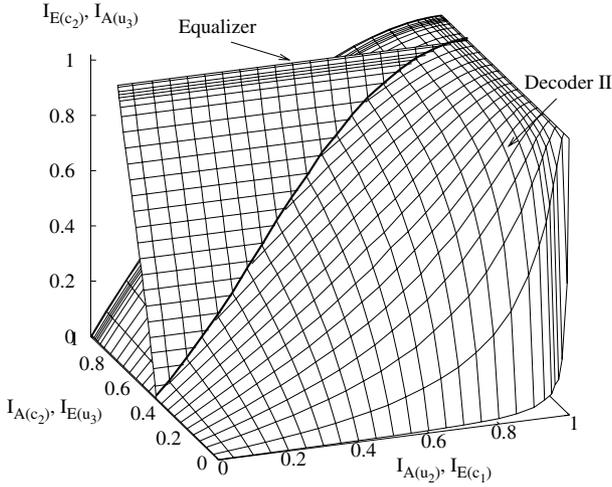
$$I_E(u_2) = T'_{u_2}(I_A(u_2), E_b/N_0). \quad (10)$$

The extreme values of $I_A(c_2)$ in Eq. (8), which corresponds to different $I_A(u_2)$ values can be visualized as the intersection of the two EXIT surfaces seen in Fig. 5(a), which is shown as a thick solid line. Furthermore, the EXIT function of Eq. (9) corresponding to the extreme values of $I_A(c_2)$ is shown as a solid line in Fig. 5(b). Finally, the EXIT function of Eq. (10) plotted for the combined module is shown in a 2D EXIT chart in Fig. 5(c).

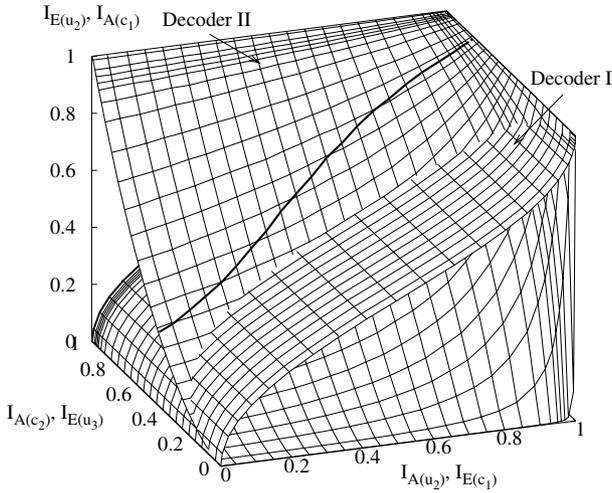
From the 2D EXIT chart of Fig. 5(c), the convergence threshold of the three-stage system can be readily determined. When using a RSC(2,1,3) having octal generator polynomials of 5/7 as the outer code, the EXIT curve of the outer code intersects with the combined EXIT curve of the equalizer and Decoder II at $E_b/N_0 = 4$ dB. Hence the convergence threshold of this system is around 4.1 dB. Note that it has been shown in [7] that the convergence point of a multiple-stage concatenated system is independent of the activation order of the component decoders. Hence, the convergence threshold determined in this way is the true convergence threshold, regardless of the activation order.

2) *Optimization of the Outer Code:* After obtaining the EXIT function of the combined module of the equalizer and Decoder II, we can optimize the outer code to provide an open tunnel between the EXIT curve of the outer code and that of the combined module at the lowest possible SNR, and hence approach the channel capacity. We carried out a code search for different generator polynomials having constraint lengths up to 5. Interestingly, we found that the relatively weak code, RSC(2,1,2) having generator polynomials of 2/3, yields the lowest convergence threshold of about 2.8 dB. The EXIT function of this code and that of the combined module at $E_b/N_0 = 2.8$ dB are also shown in Fig. 5(c)

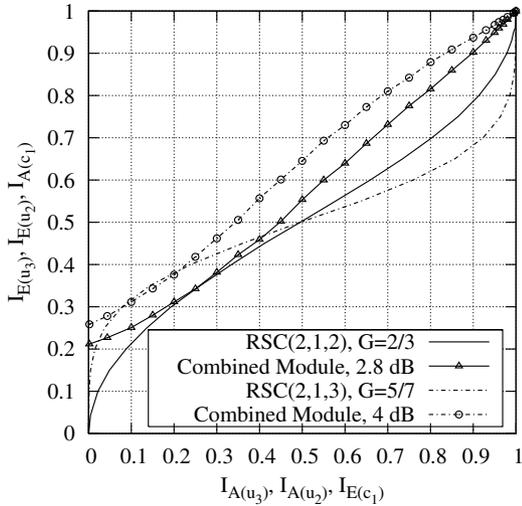
3) *Optimization of the Activation Order:* Unlike the two-stage system, the activation order of the decoders in the three-stage system is an important issue. Although different activation orders will not affect the final convergence point [7], they incur different decoding complexities and delays. A trellis-based search algorithm is proposed



(a) Decoder II and the equalizer at $E_b/N_0 = 4\text{dB}$



(b) Decoder II and Decoder I



(c) 2D EXIT chart for Decoder I and the combined module of the equalizer and Decoder II

Fig. 5. EXIT charts for the three-stage SISO system.

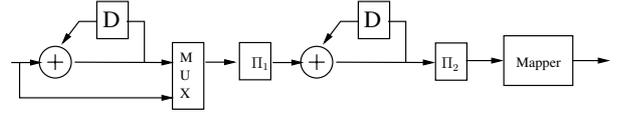


Fig. 6. A specific manifestation of the generic transmitter schematic seen in Fig. 4

in [7] to find the optimal activation order of multiple concatenated codes according to certain criteria, such as for example minimizing the decoding complexity. However, for the simple case of the three-stage system, we resorted to a heuristic search by invoking the EXIT functions of the three SISO modules according to different activation orders. The exchange of mutual information is between EXIT functions, hence this procedure is of very low complexity. In general, we found that by invoking more iterations between Decoder II and Decoder I while activating the MMSE equalizer from time to time, the three-stage system converges at a lower number of activations. This is not unexpected, since the error-correction capability is mainly provided by the serial concatenation of Decoder II and Decoder I. Furthermore, the MMSE equalizer is of the highest computational complexity among the three SISO modules, hence the less the MMSE equalizer is activated, the lower the total decoding complexity.

C. Simulation results

In our BER investigations, the RSC(2,1,2) code having the octal generator polynomials of (2/3) was invoked in Encoder/Decoder I. For the rate-1 Encoder II, again, the generator polynomial of $1/(1+D)$ was used. Fig. 6 shows a more specific manifestation of the generic schematic of the transmitter seen in Fig. 4. The block length is $L = 10^5$ bits.

Our BER results are depicted in Fig. 7. In addition to the three-stage SISO system, the BER performance of the two-stage SISO system of Fig. 1 using an MMSE equalizer is also shown. Observe in Fig. 7 that the two-stage SISO system performs better in the low-SNR region, while the three-stage SISO system has the edge in the medium to high SNR region, achieving an infinitesimally low BER for E_b/N_0 values above 3 dB. Although the two-stage scheme is of lower decoding complexity, it cannot "break" the AWGN BER bound, regardless of the number of iterations. To achieve a near-zero BER in the medium SNR range, the three-stage scheme has to be used.

Note that for the three-stage SISO system, the term "iteration" has different meaning in comparison to that used in the two-stage SISO system. In our simulations, the three SISO modules of the iterative receiver are activated periodically according to a certain order. For example, in the simulations of Fig. 7, the activation order of the three SISO modules is [3 2 1 2 1 2], where the integers represent the Index (I) of the various SISO modules. Specifically, $I = 3$ denotes the MMSE equalizer, $I = 2$ represents Decoder II and $I = 1$ denotes Decoder I. Finally, the above mentioned activation order of the three components is repeated twelve times.

The decoding trajectory of the three-stage SISO system recorded at $E_b/N_0 = 4\text{dB}$ is depicted in Fig. 8. This trajectory was obtained by recording the *a priori* input, $I_{A(c_1)}$, and the *extrinsic* output, $I_{E(c_1)}$, of Decoder I (which are also the *extrinsic* output, $I_{E(u_2)}$, and the *a priori* input, $I_{A(c_2)}$, of Decoder II) during the consecutive iterations. The vertical segments of the trajectory represent the activation of the equalizer and Decoder II at a certain number of times, while

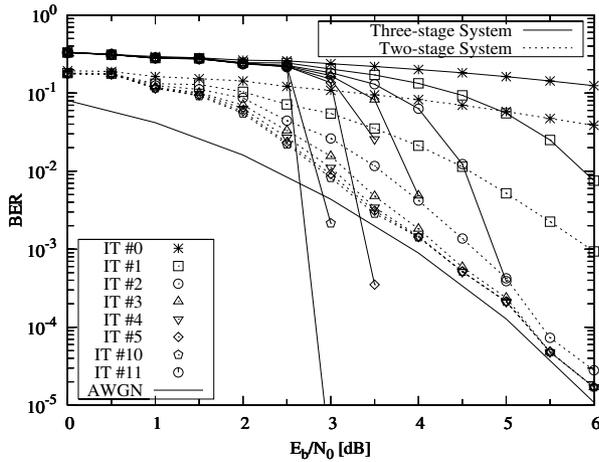


Fig. 7. BER performance of the three-stage SISO system of Fig. 4 and the two-stage SISO system of Fig. 1 using an MMSE equalizer.

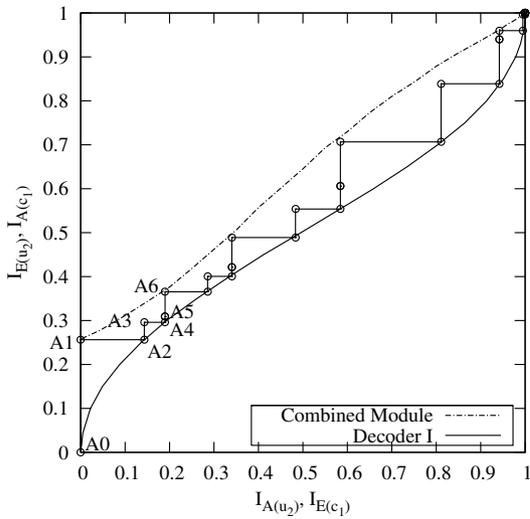


Fig. 8. EXIT charts and decoding trajectory for the three-stage SISO system at $E_b/N_0 = 4$ dB.

the horizontal segments represent a single activation of Decoder I. For example, in the simulations, we used an activation schedule of [3 2 1 2 1 2 ...]. At the beginning of iterations, the equalizer was activated, but neither the value of $I_{E(u_2)}$ nor the value of $I_{A(c_1)}$ was changed, so the trajectory stays at the A0 point. Then Decoder II was activated, resulting in an increased value of $I_{E(u_2)}$, hence the trajectory reaches the A1 point. Subsequently, Decoder I was activated, which increased the value of $I_{E(c_1)}$, hence the trajectory converges to the A2 point. Similarly, the segment between A2 and A3 represents the activation of Decoder II, the segment between A3 and A4 denotes the activation of Decoder I, and the segment between A4 and A5 denotes the activation of Decoder II. The segment between A5 and A6 represents the beginning of a new iteration associated with similar decoding activations. In conclusion, we surmise that the convergence behavior of a three-stage SISO system can be adequately visualized using a 2D EXIT chart.

IV. CONCLUSIONS AND FUTURE WORK

A three-stage serially concatenated turbo scheme using an MMSE equalizer was proposed for eliminating the residual errors encountered in more traditional two-stage turbo equalization schemes. The serially concatenated channel coding scheme consists of two low-complexity memory-1 codes, which nonetheless result in a significant iteration gain. The convergence behavior of this three-stage SISO system is accurately predicted by means of 3D EXIT charts as well as by its 2D projection.

The intermediate encoding stage, namely Encoder II was chosen to be recursive and to have unity rate for the sake of optimal decoding convergence, as suggested in [8]. The generator polynomials of the outer code of Encoder I were also optimized using EXIT chart analysis. For severely ISI-contaminated channels having diverse EXIT characteristics, irregular codes [10], [11] may be used as the outermost code for the sake of achieving early convergence, a topic, which constitutes our future research. Furthermore, the design method used here can be applied in the context of diverse iterative receivers, employing multiple SISO modules, such as the jointly designed source coding and space-time coded modulation schemes of [12].

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