Impact of strain on the design of low-power high-speed circuits

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Abstract - **In this article, we explore the impact of strain on circuit performance when strained silicon (s-Si) devices are used for designing low-power high-speed circuits. Emphasis has been given on the evaluation of noise characteristics and low-power performance along with the delay characteristics under different channel straining conditions. An inverter circuit has been used for performance evaluation through simulation where the device simulator is calibrated with experimental device data. The result shows a great promise for s-Si technology in digital applications which require high throughput and low power.**

I. INTRODUCTION

Power consumption of digital circuits is one of the main concerns of the present design community, particularly, with the market dominance of mobile and portable systems and lack of advancement of battery technology. Over the years, supply voltage scaling has emerged as the preferable technique for power reduction owing to the quadratic relationship between the supply voltage and active power dissipation [1]. However, the associated penalty comes in the form of drastic increase in circuit delay and degradation of noise margin [2]. The state of the art circuit design techniques are struggling extremely hard to satisfy the projection of International Technology Roadmap for Semiconductors (ITRS) [3] for their operations in sub-volt supply range with maintaining high-speed.

In recent years, s-Si CMOS technology has attracted much attention due to its compatibility with the existing Si process and improved device performance because of band gap engineering. It has already been exploited due to its higher carrier mobility than conventional Si to fabricate high-speed devices [4]. Accordingly, s-Si is now included in the ITRS roadmap [3]. However, the device level performance of s-Si has not yet been fully exploited by the design community. This requires research with closer integration of devices and circuits.

In this paper, we present an in-depth study of the impact of strain on speed and power performance in s-Si based circuits. The entire work reported in this paper is done by studying the static and dynamic characteristics of CMOS inverter circuits subjected to different operating conditions and different band-engineered devices. The work also addresses the impact of voltage scaling and band gap engineering on leakage, speed and noise margin at different ambient temperatures, since they are crucial in any digital design space. The rest of the paper is structured as follows: Section II describes the simulation environment and simulator calibration, in Section III the performance of s-Si inverters is studied under different straining conditions in terms of noise and power with scaling of supply voltage and conclusions are drawn in Section IV.

II. SIMULATION AND CALIBRATION

For the calibration, the device dimensions and other physical parameters are taken to be similar as those of the previously published experimental data [5]. Details of the device fabrication and electrical characterisation of data used for calibration can be found in [5, 6]. The simulation is performed using MEDICI, a commercial simulation package from Synopsys [7]. A uniform doping concentration for the channel and substrate is taken to be 1.5×10^{17} cm^{-3}.

Straining of the channel material in a CMOS device can be attained either in the wafer level by epitaxially growing a thin film of Si over silicon germanium (SiGe) alloy or in the process level by depositing SiN_3 on top of the device structures [8]. Strain itself can be of two types: bi-axial and uni-axial with either compressive or tensile in nature [8]. While compressive strain is required to enhance the mobility for holes, tensile strain can enhance mobility for both electrons and holes. In this work, we consider the devices with high performance achieved by bi-axial tensile strain. No matter how the strain is induced (whether bi-axially or uni-axially), the enhancement of carrier mobility depends on the amount of strain induced which will in turn improve the overall performance of the device [9]. The parameters for s-Si material system are taken from the literature [6]. A junction depth of 40nm has been considered. The dimensions of these devices are taken as W/L=2μm/0.13μm. Conventional Si CMOS devices of similar dimensions and doping concentrations are also simulated for a comparative study of the performance of s-Si devices. The simulator is calibrated with our experimental output characteristics for both Si and s-Si

CMOS devices. It is worth mentioning that the simulator is calibrated, to check the models and parameters chosen in the simulation for accuracy.

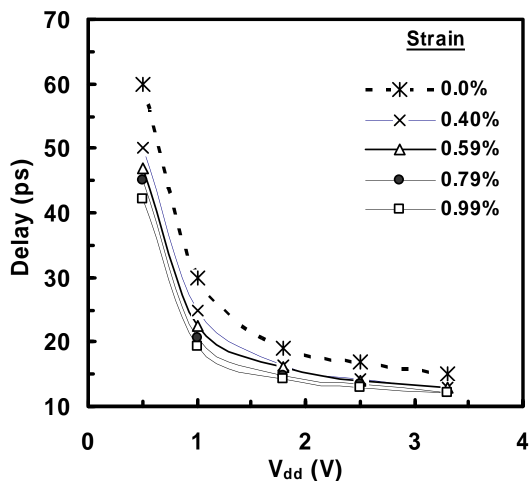

Fig. 1 The plots of propagation delay vs supply voltage for a single stage inverter made from the s-Si and conventional Si CMOS devices.

The simulated s-Si and conventional Si n- and p-MOSFETs are connected for the design of CMOS inverters using the mixed mode simulator available in MEDICI. The simulations are performed to evaluate both the propagation delay and DC transfer characteristics for the inverters. Because of the fact that the mobility enhancement of electrons and holes is asymmetric for the same amount of strain [8], the symmetric DC characteristics can only be attained by using different n- and p- geometry ratios. Here, the widths of both the pull-up and pull-down transistors are considered equal for both s-Si and Si inverters.

III. PERFORMANCE ANALYSIS

Simulations of the s-Si and Si based inverters mentioned in Section II are performed at different supply voltages ranging from 0.5V to 3.3V. The variation of propagation delay for Si and s-Si inverters against varying supply voltages are plotted in Figure 1. Figure 1 also shows the propagation delays for s-Si inverters with different amount of strain in the channel. It is interesting to note that the propagation delay of s-Si inverter with 0.99% strain in the channel consistently shows a lower delay (faster device) at all supply voltages. The smaller delay exhibited by s-Si device accounts to the fact that mobility of the carriers is enhanced by a certain amount depending on the amount of strain induced in the channel [9]. Compared to the s-Si inverter with 0.99% strain in the channel, delay for the Si inverter is seen to be higher (slower device) by 33%. It can be seen from Figure 1 that the propagation delay of s-Si inverter with a strain of 0.99% operated at a supply voltage of 1V is similar to that of the Si CMOS inverter operated at 1.8V. Thus similar speed performance can be obtained for s-Si devices compared to the Si one at much lower supply voltage, resulting in significant reduction of dynamic power dissipation. Reducing the supply voltage for achieving low power will degrade the noise margins. Therefore, it is important to study the noise characteristics for different supply voltages applied to inverters with varying amount of strain.

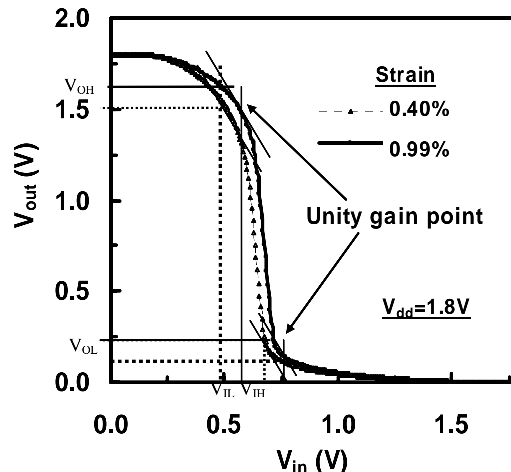

Fig. 2 The DC transfer characteristics @ V_{dd} = 1.8V for the s-Si inverters with different amount of bi-axial strain in the channel.

DC transfer characteristics of s-Si inverters with 0.40% and 0.99% strain in the channel are plotted in Figure 2. A voltage of 1.8V is supplied to the inverters. It should be noted from the figure that the output high to low and low to high transition unity gain points of s-Si with 0.99% strain is different from that of s-Si inverter having a 0.40% strain. The difference between lower (V_{IL}) and higher input voltage (V_{IH}) where the transfer characteristic is '-1' is calculated. It is lower for s-Si inverter with 0.99% strain than the inverter with 0.40% strain. This shows that for a 0.99% strained device a small change in input voltage (V_{IL} to V_{IH}) produces a large change in output voltage resulting in greater attenuation of noise at the input of gate compared with inverter with lower amount of strain. It can be concluded that when the amount of strain increases the noise immunity increases.

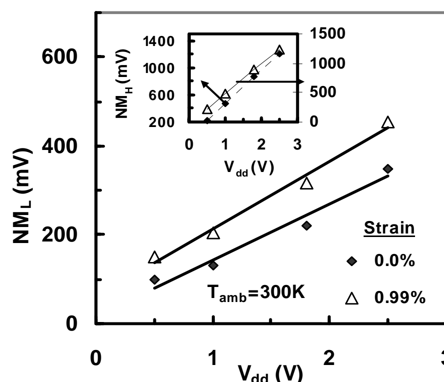

Fig. 3 The plots of variation of NM_L and NM_H with supply voltage scaling.

Figure 3 shows the variation of low noise margin (NM_L) (high noise margin (NM_H) shown in the inset of figure) of a s-Si inverter with 0.99% strain in the channel in comparison to Si inverter against supply voltage scaling. NM_L and NM_H are seen to degrade with supply voltage scaling which is expected, since the threshold

voltage and 'input and output transition points' are scaled with the supply voltage. It should be noted that still the NM_L and NM_H are higher for s-Si inverter due to the inherent property of lower threshold voltage and higher on-current for s-Si devices compared to Si devices.

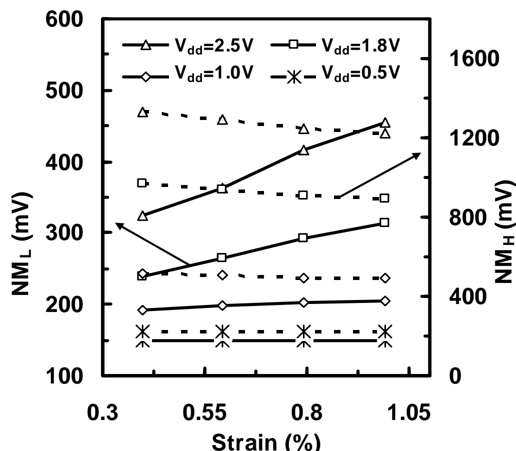

Fig. 4 The plots of variation of NM_L (*solid lines*) and NM_H (*dotted lines*) with the amount of induced strain in the device channel at different supply voltages.

Figure 4 shows the variation of NM_L and NM_H for s-Si inverters with different amount of stain. It should be noted that NM_L is increasing whereas NM_H is decreasing with increase in the amount of strain in the channel. With the increase of amount of strain, the mobility of the carriers in the channel are increased which will increase the process transconductance (K) which will in turn increase the device transconductance (β). With the increase in the amount of strain, the mobility enhancement for electrons and holes are not similar (it is higher for holes at higher amount of stain) and hence the transconductance ratio ($\beta n/\beta p$) decreases for same n- and p- geometry ratio and the voltage transfer curve (VTC) shifts towards right (Figure 2) which explains why NM_L is increasing with increasing amount of strain while NM_H decreases. Hence bi-axial strain can be optimised for symmetrical VTC's depending on the mobility enhancement.

Another interesting fact is that as the supply voltage is lowered below 1 V (which is typical operating condition for the deep sub-micron circuits) the NM_L and NM_H show very little dependence on strain although at higher supply they show significant dependence on the strain. From this result, it seems that when sub-1V supply is applied, the amount of strain present in the channel matters very little as far as the noise immunity is concerned. Thus, for sub-volt operation the optimization of strain should be more focussed on optimizing speed and power only.

The inverter circuit is simulated for diffferent ambient temperatures and the plots of noise margins are shown in Figure 5. The decrease of noise margins in the figure is attributed to the reduction of current gain (I_{on}/I_{off} ratio) for the degraded threshold voltages and sub-threshold slopes at elevated temperatures.

It is apparent from the above simulated results that the degradation of noise margins exhibited by s-Si circuits is not worse than Si circuits when the supply voltage is scaled to achieve low power performance. On the contrary, s-Si based circuits show significantly better noise margin compared to Si based circuits under the similar operating conditions.

Although s-Si based circuits show better speed and noise performance compared to Si based circuits and it is possible to optimize dynamic power dissipation for s-Si circuit by engineering the strain, its overall advantage hinges upon one fact: the leakage power dissipation.

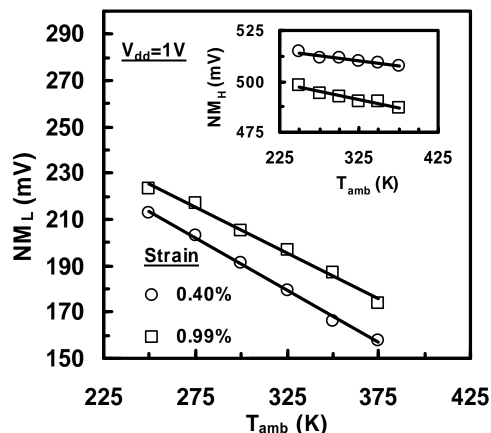

Fig. 5 The variation of NM_L and NM_H with the ambient temperature @ V_{dd} = 1V for different amount of strain along the device channel.

Figure. 6 shows the decrease of leakage current flowing through the s-Si and Si transistors when the drain/source voltage is scaled down. When the amount of strain applied in the channel increases the leakage current is found to increase by a marginal amount. From Figure 6, it is seen that the leakage current of s-Si device is higher than that of Si by almost an order of magnitude. For the continuously operated circuits, the increased leakage current due to reduction in threshold voltages is not significant.

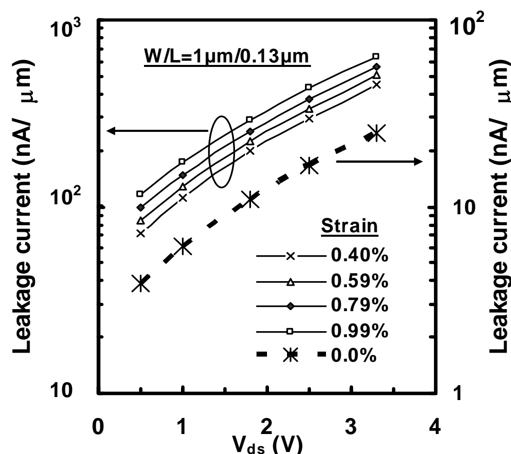

Fig. 6 The plots of leakage current vs drain source voltage for different amount of strain along the device channel.

However, circuit components which are idle during the operation of a circuit suffer from leakage currents. Hence it would be ideal to analyse the effect of leakage

current in combinatin with the change of amount of bi-axial strain at different operating conditions.

Figure 7 shows the plot of energy efficiency for the effect of delay and supply voltage scaling. Minimum energy point (MEP) (shown in the inset of figure 7) is defined where the active energy and leakage energy cross each other. It is apparent from the plot that the MEP shifts towards right with increasing induced strain in the channel. MEP is found to vary from 0.57V to 0.7V depending on the amount of induced strain. The MEP for Si inverters for the same output load will fall below its threshold voltage and hence, these will not be functional at these supply voltage regions. This is due to the fact that the leakage current for a Si device at similar drain to source voltage is approximately an order lower than that of a s-Si device, as shown in Figure 6.

If the s-Si inverters with 0.99% strain in the channel are operated at a V_{dd} of 0.7V (which is the MEP for 0.99% strain, as shown in Figure 7) then the delay is found to be 32ps. However, it is found to be 40ps for the inverters with 0.40% strain in the channel at the same V_{dd}. This implies an improvement in speed of 20% for the inverter with 0.99% strain compared to those having 0.40% strain in the channel. If the operation of the inverters is considered from the perspective of minimum energy point (MEP) for 0.40% strain in the channel, then the delays of 47ps and 37ps are observed for the inverters with 0.40% and 0.99% of strain, respectively. This implies a 21% increase in speed for the inverters with 0.99% strain compared to the inverters with 0.40% strain in the channel. However, this speed improvement will compromise the minimum energy criteria of 0.99% strain.

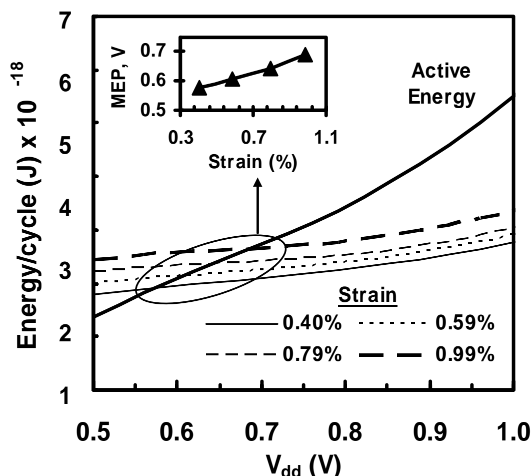

Fig. 7 The variation of Energy/Cycle with supply voltage for s-Si inverters with varying amount of strain in the device channel. Si is not operational as its MEP falls below its threshold voltage.

The important point here is that depending on the circuit requirement (whether faster operation or lower power) strain can be engineered to satisfy the required criteria. Although the natural tendency is to increase speed by using more strain, when all the performance parameters like noise immunity, power dissipation and speed are considered, the result shows that 0.99% (more leakage) strain or 0.40% (slower operation) strain could hardly be an optimal solution. The optimal strain can be be chosen following the need of a desired set of circuit performance parameters. This added flexibillity of s-Si process is very much beneficial as circuits with different properties can be obtained under the same fabrication process.

IV. CONCLUSIONS

In this work, the applicability of s-Si technology for low-power circuits without sacrificing the delay has been explored. Although the supply voltage scaling adversly affects the noise margins for s-Si inverter, it is still better compared to that of the conventional Si inverters. However in the sub-1V supply region, the noise performance is relatively independent of the amount of induced strain. The MEP of s-Si also proves its ability to operate at supply voltages near to its threshold voltage without inflicting much leakage while at the same time reducing dynamic power significantly. The additional advantage of the s-Si based circuits is that the strain can be engineered to satisfy different types of circuit requirements under the same process flow. These facts make s-Si circuits an ideal candidate for futuristic ultra low power digital circuit design.

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