Exploration of Potential of Strained-Si CMOS for Ultra Low-Power Circuit Design

H. K. Ramakrishnan[1], S. Chattopadhyay[1], K. Maharatna[2], S. Shedable[1], and A. Yakovlev[1]

[1]**Newcastle University, Merz Court, NE1 7RU, Newcastle upon Tyne, UK**
[2]**University of Southampton, Highfield, SO17 1BJ, Southampton, UK**

Abstract

This article investigates the possibility of using strained-Si (s-Si) for the design of future generation low-power digital circuits. The well known property of high current-drive of s-Si makes it very attractive for circuit applications. Here, we simulate the s-Si based inverter circuits to explore its applicability for low power high performance circuits. The simulation parameters are calibrated with experimental devices. The work shows great promise for s-Si in future digital circuit applications, particularly when low-power and high-performance are the dominating factors for design.

1. Introduction

Power dissipation in the conventional Si based complementary metal oxide semiconductor (CMOS) digital circuit design is becoming a key design criterion to meet the ever increasing demand for mobile computing with high data rate and the lack of significant advancement of battery technology. Over the years, supply voltage scaling has emerged as the preferable technique for power reduction owing to the quadratic relationship between the supply voltage and active power dissipation [1]. However, the associated compromise comes in the form of drastic increase in circuit delay. In applications requiring high performance, supply voltage scaling poses serious limitation in terms of speed [2]. The International Technology Roadmap for Semiconductors (ITRS) [3] projects sub-1V and 0.5V nominal supply at 90nm and 22nm technology nodes, respectively, for low operating power. Current circuit design research with Si-based CMOS is seriously challenged by these criteria to maintain high-speed operation.

Another path that could be adopted is to use materials having high carrier mobility instead of Si and trading off their speed for power through supply voltage scaling. In the recent years, much attention has been paid to evaluate the potential of s-Si devices in comparison to Si devices due to its compatibility with the existing Si process technology. The inherent superior mobility of s-Si has already been exploited to fabricate high-speed low-threshold devices that can be used for the design and fabrication of high-speed circuits [4-7]. Accordingly, the use of s-Si is now included in ITRS roadmap [3]. However, the device level performance improvement of s-Si has not yet been exploited by the design community barring some experimental discrete RF circuits, which takes the advantage of high-speed operation of s-Si transistors.

The present work is the first of its kind which explores the possibility of performance enhancement in terms of power and speed using s-Si devices for digital circuit design. Although, in this work, we present studies on general behaviour of digital CMOS circuits using s-Si as the base material, emphasis is given on noise performance analysis. This stems out from the fact that if trade-off between speed and supply voltage is made to reduce active power, the most likely parameter that gets affected is the noise margin. In this work, the experimental device data has been used for our circuit simulation. The entire work is done by studying the static CMOS inverter circuit characteristics subjected to different operating conditions and device dimensions. The choice of inverter is obvious since this is one of the basic logic gates. Our work shows that under the scaled supply voltage condition, s-Si based inverter shows highly superior performance compared to Si based inverters. Comparison of delay and DC transfer characteristics between s-Si and Si-based inverters is performed in section 3. Section 4 addresses the impact of voltage scaling, and device dimensions on noise margin.

2. Simulation of s-Si CMOS devices

The simulator has been calibrated to check the accuracy of the models used and the parameters chosen in the simulation. Details of the device fabrication and electrical characterisation results used for calibration can be found elsewhere [3-5]. The device dimensions and other physical parameters are taken to be similar as that of the

previously published experimental data [4-7, 9]. In this work, we consider the s-Si devices with high performance achieved by bi-axial tensile strain. No matter how the strain is induced (whether bi-axially or uni-axially), the enhancement of carrier mobility depends on the amount of induced strain which in turn will improve the overall performance of the device [5, 6]. In the present work, devices with 0.99% (~25% Ge composition) strain are considered.

3. Inverter characteristics and power performance enhancement

The simulated s-Si and conventional Si n- and p-MOSFETs are connected for the design of CMOS inverters using mixed mode, available in the MEDICI device simulator [10]. The simulations are performed to evaluate both the propagation delay and DC transfer characteristics for the inverters. The symmetric DC characteristics can only be attained by using different n- and p-geometry ratios since the mobility enhancement of the electrons and holes is asymmetric for the same amount of strain [4].

For all the simulations, the width of the device is considered to be 1μm. The gate length for the CMOS devices investigated is 90nm. Simulations are performed at supply voltages ranging from 0.3V to 1V. The comparative analysis of s-Si and Si CMOS inverters in Figure 1 shows that the increase of delay with supply voltage scaling is more severe in Si inverters. This is attributed to the fundamental difference of Si and s-Si. The latter inherently has lower threshold voltage compared to that of the former due to the presence of strain and smaller band gap. Thus, during voltage scaling, the supply voltage approaches the threshold voltage of Si devices much faster than that of the s-Si devices and consequently, the delay of Si inverter is more than 45% higher compared to s-Si inverters at 0.5 V. This particular property of s-Si circuits make them more attractive for ultra low-voltage (and consequently, ultra low-power) operation and thus, s-Si circuits have greater potential than the Si-based circuits to meet the ITRS roadmap, leading to ultra-low supply voltage era. At ultra-low supply voltage, the Si-based circuits exhibit low-power performance compromising its speed while the s-Si based circuits attain higher speed without compromising its power, even though the supply voltage scaling continues.

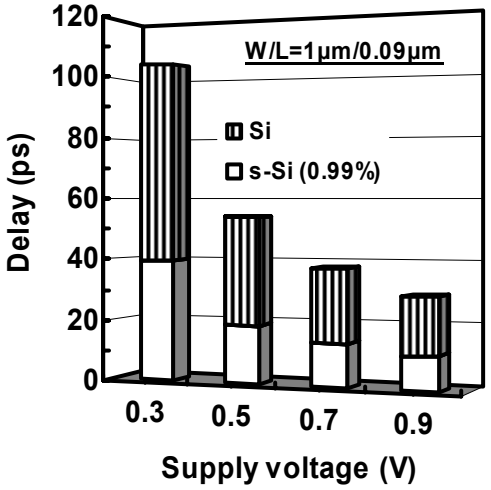

Fig. 1. Variation of delay of s-Si and Si inverters against supply voltage scaling.

It is apparent from the above results that the s-Si inverters have almost 2x speed advantage over its Si counterpart and therefore can be exploited to reduce power dissipation by scaling the supply voltage for a comparable speed performance. It has also been observed from our previous studies that the scaled s-Si based inverters consistently showed smaller delay compared to its Si counterpart [8].

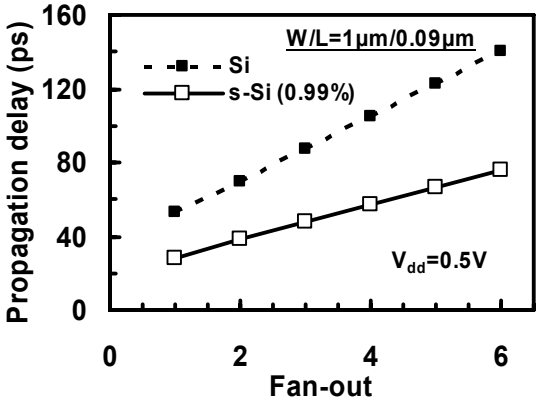

Fig. 2. Propagation delay for s-Si and Si inverters for different fan-outs.

A more interesting case is to see the delay characteristics under different fan-out conditions. This is simulated for devices with a channel length of 90nm and the resulting characteristics are shown in Figure 2. It can be seen from the plot that as the fan-out increases, the propagation delay of s-Si inverters increases much less rapidly than the Si-based counterpart reaching to a delay difference of almost 100% at a fan-out stage of 6. It is also evident that even for a less fan-out number, such as 4, the difference of delay is quite significant. These results indicate that the s-Si based inverters are

capable of exhibiting higher speed performance in comparison to the Si-based inverters under actual operating condition.

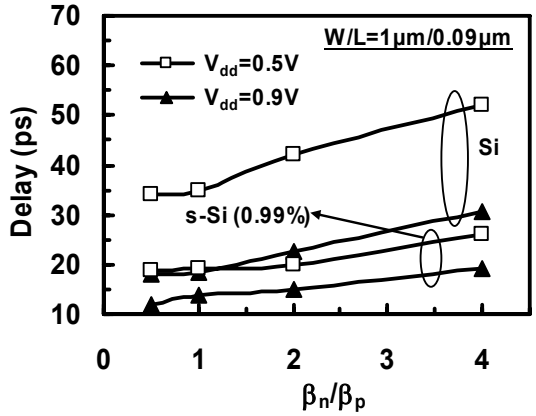

Fig. 3. Variation of delay for different supply voltages against β_n/β_p values.

It is also important to study the behaviour of transfer characteristics with respect to β_n/β_p (where β is the process gain factor for a transistor) for the s-Si inverters. Figure 3 shows delay characteristics at supply voltages of 0.5V and 0.9V for different values of β_n/β_p. Interestingly, as the supply voltage is lowered from 0.9V to 0.5V, the difference of delay is increased from 12ps to 18ps for s-Si whereas it is 18ps to 34ps for Si at β_n/β_p= 0.5. At β_n/β_p=1, these variations are from 14ps to 19ps and 18.5ps to 35ps for s-Si and Si, respectively at the same supply voltage conditions. The trend suggests that for a fixed β_n/β_p, the s-Si circuits give better speed performance than the Si- based circuits at all supply conditions. This fact once again is attributed to the inherently low threshold voltage achievable for s-Si CMOS devices. Therefore, the most important point to note from this observation and from the voltage-delay characteristic of Figure 1 is that, irrespective of the design criterion, s-Si based circuits always allow supply voltage scaling by at least 2x resulting in 4x power saving.

4. Noise margin analysis

It has been already established in previous sections that the s-Si based circuit offers several advantages, especially for power dissipation at a nominal delay compromise compared to the Si-based circuits and is highly suitable for ultra-low supply voltage. However, the reduction in supply voltage immediately poses the challenge of reducing noise margin since the noise performance becomes worse with scaling of supply.

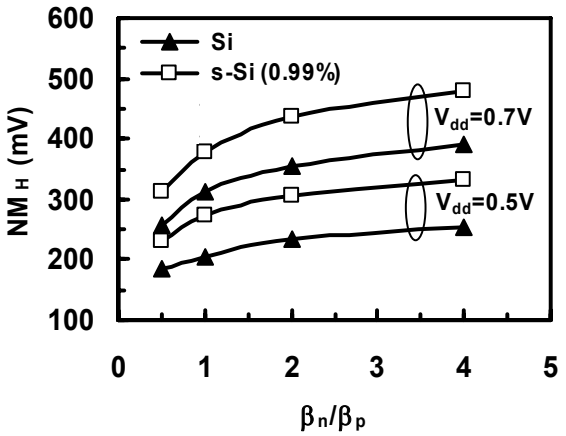

Fig. 4. Variation of NM_H for different supply voltages with different β_n/β_p values.

To study the noise performance, both the inverters are simulated under different supply voltages and NM_H (high noise margin) and NM_L (low noise margin) with respect to different β_n/β_p values are evaluated and are shown in Figure 4 and Figure 5, respectively. The point to be noted here is that, the value of NM_H (Figure 4) for s-Si inverters is always greater than that of Si inverters at all β_n/β_p values and it increases with increasing β_n/β_p ratio at the lower supply voltages.

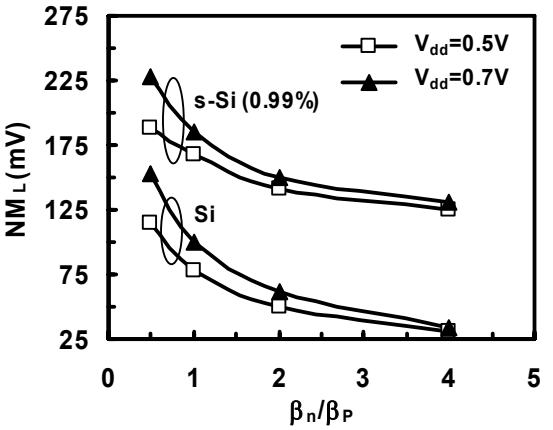

Fig. 5. Variation of NM_L for different supply voltages with different β_n/β_p.

The difference in NM_H of s-Si and Si CMOS inverters ranges from nearly 54mV at β_n/β_p=0.5 to about 87mV at β_n/β_p=4 for a supply voltage of 0.7V. However, at a supply voltage of 0.5V, the difference between s-Si and Si NM_H decreases, even though the s-Si NM_H remains higher. On the other hand, the value of NM_L for s-Si and Si inverters becomes closer with the increase of β_n/β_p value as the supply voltage is lowered as is shown in Figure 5. In each case, s-Si inverters show a

higher value compared to the Si inverters. It is apparent from the results that with the supply voltage scaling from 0.7V to 0.5V the worst-case degradation for NM_L for s-Si and Si inverter are almost 17% and 24%, respectively. Similarly, the relative degradation of NM_H are seen to be 26% and 27%, respectively.

It is to be noted from Figure 5 that the NM_L for s-Si inverters always remains higher than Si. These results show an overall better noise performance compared to the Si inverters. Another particular parameter of interest in this study is the range of logically undefined region at the input of the inverters, which is defined as the difference between lowest input-high and largest input-low voltage.

A smaller undefined region is deemed to be profitable from the noise margin and input metastability point of view. It was observed from our previous analysis [7] that Si based inverters show much higher undefined region compared to its s-Si counterpart for a similar channel length. In addition, it has been noted that there is a very little dependence of logical undefined region on channel length in s-Si inverters unlike Si inverters. This property, in essence, provides an extra degree of freedom to the designers to engineer required noise margin by adjusting the width of the devices only. The advantage with the s-Si devices is that the DC transfer characteristics can move right or left with the same W_n/W_p ratio, by changing the amount of strain in n- or p-MOSFET since the mobility enhancement of both the MOSFETs for different strain is different. This will provide enough flexibility to the digital circuit designers to adjust noise margins to save from metastability and for the signal processing engineers for better data coupling.

5. Conclusion

In this paper, we have explored the potential of s-Si CMOS devices for low-power circuit design by simulation. Experimental device data are used for calibrating the simulator. This work shows that it is possible to achieve significantly better low-power performance from s-Si based circuits than Si, since it allows significant window of voltage scaling without sacrificing for delay significantly. This is attributed to its inherently low threshold voltage and higher carrier mobility. This voltage scaling window is at least two (2x) – three (3x) times higher than that available from Si-based circuits. Thus, under the same performance specification, the s-Si based circuits can achieve at least 4x more power reduction compared to its Si-based counterpart. However, voltage scaling affects noise margin performance adversely both for Si and s-Si based circuits. But the noise margin performance for s-Si always remains superior than Si based circuits under similar operating conditions. This fact coupled with the availability of higher supply voltage reduction makes s-Si an ideal candidate for futuristic ultra low-power digital circuit design.

6. References

[1] A. P. Chandrakasan, S. Shend and R. Brodersen, "Low-power CMOS VLSI design", *IEEE J. Solid-State Cir.*, **27**, pp. 473 – 484, Apr. 1992.

[2] L. Nazhandali et al., "Energy optimization of subthreshold-voltage sensor network processors", in *Proc.ISCA'05,* pp. 197 – 207, 2005.

[3] International Technology Roadmap for Semiconductors, *http://public.itrs.net*, 2005.

[4] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, and E. A. Fitzgerald, "Carrier mobilities and process stability of strained-Si n and p-MOSFETs on SiGe virtual substrates," *J. Vac. Sci. Technol.B, Microelectron. Process. Phenom.*, **19**, pp. 2268–2279, Nov. 2001.

[5] S. Chattopadhyay, L. S. Driscoll, K. S. K. Kwa, S. H. Olsen, and A. G. O'Neill, "Strained-Si MOSFETs on relaxed SiGe platforms: Performance and challenges," *Solid State Electron.*, **48**, pp. 1407–1416, Aug. 2004.

[6] K. Rim, J. L. Hoyt, and J. F. Gibbons, "Fabrication and analysis of deep submicron s-Si n-MOSFET's", *IEEE Trans. Electron Devices.,* **47**, no. 7, pp. 1406-1415, Jul. 2000.

[7] H. Ramakrishnan, S. Chattopadhyay, A.Yakovlev, S. S. Dlay, and A.G. O'Neill, "Design of s-Silicon inverters for future VLSI applications", *Int. Conf. on Materials and Advanced Technologies (ICMAT 2005),* Jul. 2005.

[8] H. Ramakrishnan, K. Maharatna, S. Chattopadhyay, A. Yakovlev and A. G. O'Neill, "Impact of strain on the design of low-power high-speed circuits," *ISCAS 2007*, New Orleans, May 2007 (Accepted for publication).

[9] L. Yang, J. R. Watling, R. C. W. Wilkins, M. Borici, J. R. Barker, A. Asenov, and S. Roy., "Si/SiGe heterostructure parameters for device simulations", *Semicond. Sci. Technol.,* **19**, pp.1174–1182, Aug. 2004.

[10] MEDICI user's manual: Two-Dimensional Device simulation program, Sunnyvale, CA: Synopsys, Inc., 2000.