CORDIC BASED ARRAY ARCHITECTURE FOR AFFINE TRANSFORMATION OF IMAGES

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Abstract

In this paper a multiplierless array architecture of Affine transformation is proposed. The array architecture utilizes CoOrdinate Rotation DIgital Computer (CORDIC) arithmetic unit as the basic Processing Element (PE). To construct the architecture two types of CORDIC units viz. the circular and linear are used. The architecture is flexible and can be configured according to the specification of the user. Due to its multiplierless organization the array architecture is expected to consume less silicon area and power compared to that of the multiplier-based designs.

Introduction

Affine transformation is a powerful tool for carrying out the geometrical transformation of the images. In different image processing, graphics and CAD applications the object or the image are normally described and characterized numerically in some co-ordinate system, most often in the Cartesian co-ordinate system. But since depending upon the applications, the user requires more than one co-ordinate system for having a detailed view of it, the object under question is often mapped to a new co-ordinate system by invoking a sequence of mathematical operations like rotation, shearing, scaling and translation. All these four operations can be clubbed into a common term, the Affine transformation [1].

The computational intensiveness of the Affine transformation can be readily appreciated by observing the fact that it performs a series of mathematical operations like, trigonometric and arithmetic multiplication, addition and subtraction on every points of the image data. To perform this huge data computation at sufficiently fast rate, typically in real time, dedicated hardware support is much sought.

In conventional raster scan graphics systems, the Affine transformation is carried out using 4×4 matrix multiplier unit. However, for computing trigonometric multiplication, where the value of target angles are not known, the conventional multiplier requires a large storage ROM (to store the precomputed values of the trigonometric functions) and is not a flexible solution. The CORDIC algorithm [2] is an alternative to the conventional multipliers especially when the trigonometric multiplication is to be computed. While using the circular mode of CORDIC operation it is possible to carry out trigonometric multiplication in an elegant manner, its linear mode of operation can be utilized for carrying out the arithmetic multiplication operation with less hardware cost.

In this article, the authors have proposed array architecture for computing the Affine transformation of images using CORDIC as the basic PE. In the proposed architecture two types of CORDIC units *viz*., circular and linear, have been used. The architecture is completely multiplierless and can be configured according to the user's specification. The paper is structured as follows: in Section 2 the newly developed circular and linear CORDIC units are described and Section 3 describes the Affine transformation architecture using these units. In Section 4 the conclusions are drawn.

2. The CORDIC processors

2.1 The circular CORDIC processor

As has been mentioned earlier, the circular CORDIC processor can be utilized to compute the trigonometric multiplication operation in a much

more flexible and elegant way compared to the conventional multipliers. However, it has two major limitations *viz*., the requirement of post-processing circuitry to compensate the scaling factor and its limited range of angular convergence. To overcome these difficulties, the circular CORDIC algorithm is reformulated in the following way:

In our formulation, the elementary rotational angle for circular CORDIC operation is expressed as,

$\sin\alpha_i = \alpha_i = 2^{-i}$ (1)

With this consideration the CORDIC rotation of a vector $[x \quad y]^T$ through an arbitrary target angle can be defined as

$$\begin{bmatrix} x1 \\ y1 \end{bmatrix} = \prod_{i=p}^{b-1} \begin{bmatrix} 1-2^{-(2i+1)} & 2^{-i} \\ -2^{-i} & 1-2^{-(2i+1)} \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \quad (2)$$

where, $i \geq \lceil (b-2.585)/3 \rceil = p$, b is the wordlength of the processor. The above expression is derived considering a 16-bit implementation. It can be seen from equation (2) that this formulation rules out the scale factor compensation step while preserving the property of the CORDIC that the complete operation can be carried out using a series of only shift-and-add method.

To enhance the angle convergence range, we divide the entire co-ordinate space in four quadrants and express the effect of rotation at different quadrant with the result of rotation in the first quadrant. The processor can adaptively select appropriate iteration step (i) to converge the target angle at fast rate. The resulting structure is shown in Figure 1 [3].

2.2 The linear CORDIC processor

In terms of linear CORDIC operation the multiplication of two numbers M (multiplier) and N (multiplicand) can be expressed as follows:

$$\begin{bmatrix} M \\ MN \end{bmatrix} = \prod_{i=0}^{b-1} \begin{bmatrix} 1 & 0 \\ -2^{-i} & 1 \end{bmatrix} \begin{bmatrix} M \\ 0 \end{bmatrix} \quad (3)$$

We developed a linear CORDIC processor that works according to the equation (3) with the added capability to select the appropriate iteration index (i) adaptively. This enables the processor to converge to the final target value at fast rate. The structure of the adaptive linear CORDIC unit is shown in Figure 2 [3].

Both processors are provided with a signal 'PC' that indicates the completion of the operation. This signal can be viewed as handshaking signal that facilitates inter processor asynchronous data transfer.

3. The Affine transform architecture

The Affine transform unit is developed in a hierarchical manner. The complete Affine transform architecture comprises of four modules, *viz*., rotation (R), shearing (SH), scaling (SC) and translation modules (TR) as shown in Figure 3. The rotation, shearing and the scaling modules communicate with each other through a set multiplexers. The multiplexers are controlled in accordance with the user's specified operation sequence. The outputs of each of these modules are connected to another set of output multiplexers. The translation vector are added/subtracted to this output in order to generate the final desired output. This operation is carried out using an adder/subtractor unit.

The rotation module consists of a pipelined linear array of three circular CORDIC elements. On the other hand, the shearing module consists of three linear arrays arranged in parallel, each of which is composed of two linear CORDIC units connected in pipelined fashion. To carry out the functionality of the scaling unit, only three linear CORDIC units arranged in parallel are required. Each of the CORDIC units in these modules can be activated selectively according to the user's specification (1-D, 2-D or 3-D operation). For each module the data transaction between the respective PEs is carried out asynchronously using the PC signal generated by the circular and linear CORDIC element.

For internal control of the Affine transformation architecture, 12 control bits are generated from possible operation sequences that can be defined by the user. The logic states of these bits are used to control the operations of the modules (and their internal CORDIC elements) of the Affine transformation architecture. Apart from these 12 control bits, 3 additional single bit signals, *viz*., R, Sh and Sc are also generated from the user defined operation sequence which act as the enable signal for the rotation, shearing and scaling units respectively. Depending upon the operations specified by the user, these signals can be asserted to selectively enable a particular module and thus, this arrangement offers a greater flexibility to carry out the desired operations in an interactive manner. As for example, if the user intends to carry out the rotation operation only,

the logic states assumed by the signals R, Sh and Sc will be 'HIGH', 'LOW' and 'LOW' respectively. This essentially means that while the rotation module is in enable condition the other two, *viz*., the shearing and the scaling modules are in disabled state. To save the power dissipation in such a case, where the user utilizes only a fraction of the complete functionality provided by the Affine unit, simple power management strategy is employed which shuts down the unused blocks of the system.

Being composed of multiplierless CORDIC units, this architecture is expected to consume less floor space compared to that of its multiplier-based counterparts. This implies less parasitic and routing capacitances. The pipelining and parallelism incorporated in the architecture enables sustained and high throughput rate and at the same time are also profitable for low power applications [4]. The asynchronous data transaction between the PEs supplemented by the efficient power management strategy also enhances the low power compatibility of this architecture.

4. Conclusions

The proposed architecture provides a flexible means to carry out the required operations interactively and depending upon the mode of operations the same is also capable to compute multidimensional Affine transform as well. The architecture is highly suitable for low power application also, which is almost mandatory for current state-of-the-art systems.

References

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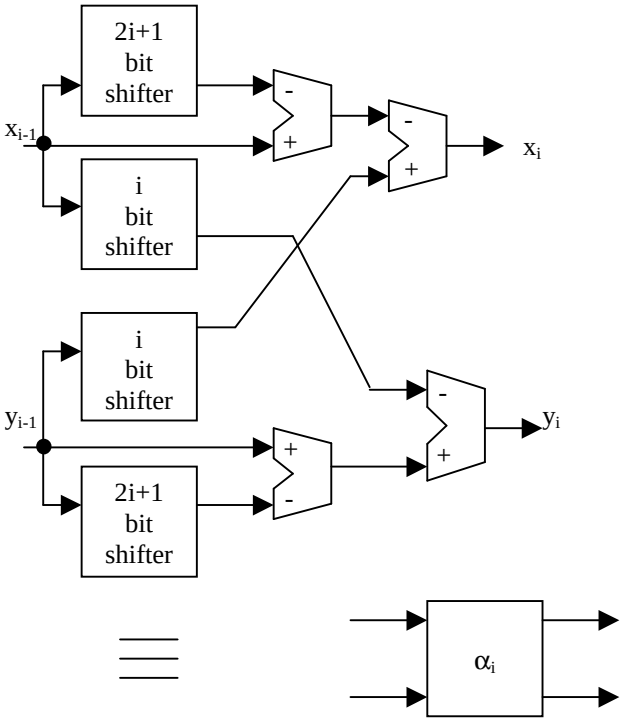

Figure 1.1 The elementary CORDIC element

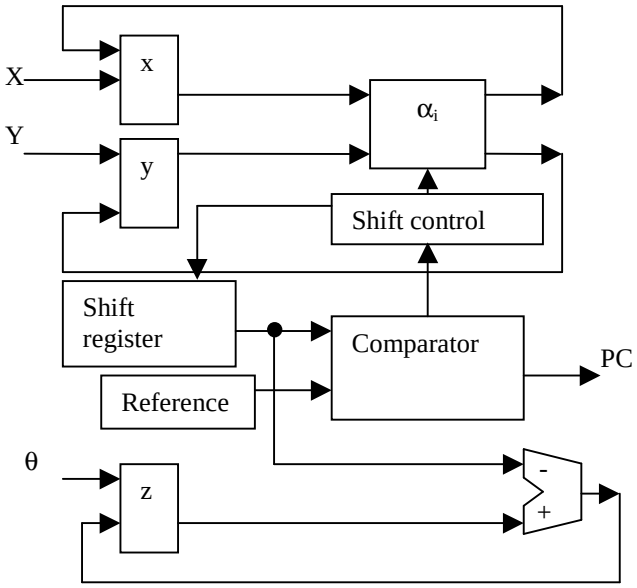

Figure 1.2 The complete rotational CORDIC unit

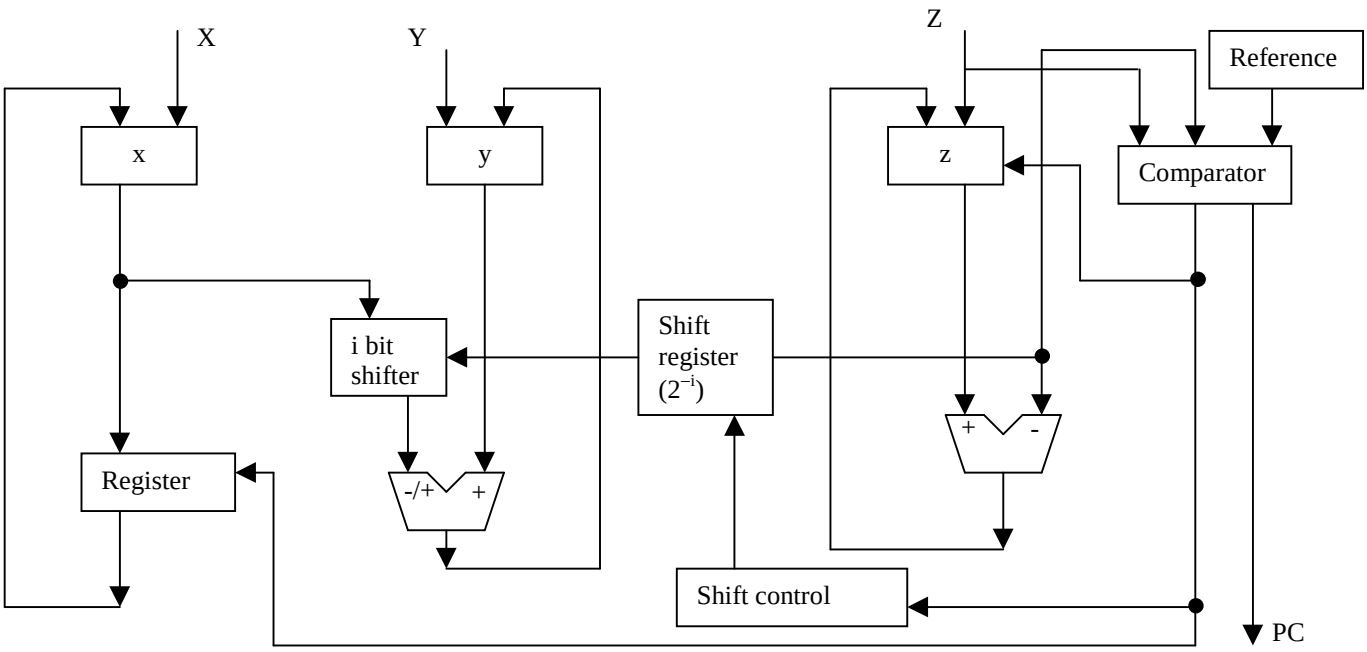

Figure 2. The linear CORDIC unit

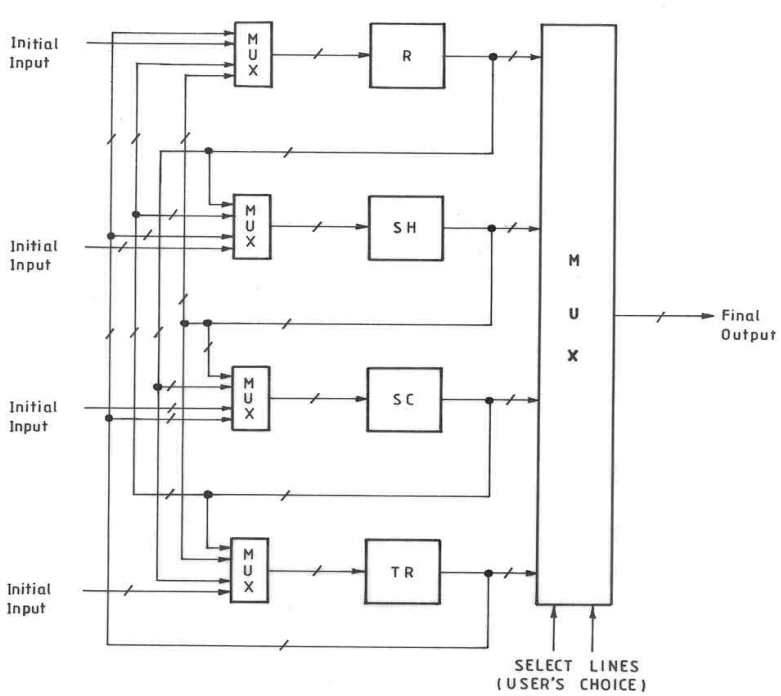

Figure 3. The complete Affine transformation unit