

A Low-Power 64-point FFT/IFFT Architecture for Wireless Broadband Communication

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Abstract:

A low power 64-point FFT/IFFT architecture is developed for the application in OFDM based wireless broadband communication system. The proposed architecture satisfies the specifications of IEEE 802.11a and ETSI Bran. The architecture requires 25% multiplication and 86% addition/subtraction operation compared to the conventional Cooley-Tukey approach. This leads to power and area saving as well. The architecture is capable to perform FFT and IFFT without changing the internal coefficients which makes it highly suitable for practical applications.

Index terms: FFT/IFFT, OFDM, Low-power.

1. Introduction

FFT/IFFT is an integral component of the Physical layer (PHY) of Orthogonal Frequency Division Multiplexing (OFDM) based wireless communication system. The specifications of IEEE 802.11a [1] and ETSI Bran [2], which eventually forms the basis of such a communication system, shows that FFT/IFFT is one of the most computation intensive component of the PHY layer. According to these specifications, the transceiver of the OFDM based wireless communication system has to perform 64-point FFT (in the transmit direction) or IFFT (in the receive direction) within 4 μ sec. This tight timing constraint implies that one has to use highly specialized architecture for the same. It is obviously possible to use the conventional Cooley-Tukey algorithm [3] for this purpose but to meet the specification one has to employ a highly parallel structure or use a very high frequency of operation that leads to high area and power consumption. Thus, it is always better to apply different design

methodology to keep the area and power consumption as low as possible and at the same time satisfying the timing constraint.

In this paper, we propose a power efficient 64-point FFT/IFFT architecture that satisfies the specification of IEEE 802.11a and ETSI Bran. The architecture internally uses only 8-point FFT for computation of the 64-point FFT/IFFT. The performance analysis of the architecture exhibits its superiority compared to the conventional butterfly approach. The rest of the paper is structured as follows: in Section 2, the mathematical formulation of it is discussed and the architecture is described in Section 3. Section 4 is devoted to the performance evaluation of it and conclusions are drawn in Section 5.

2. The mathematical formulation

The FFT $A(r)$ of a complex data sequence $B(k)$ of length N where $r, k \in \{0, 1, \dots, N-1\}$ can be described as,

$$A(r) = \sum_{k=0}^{N-1} B(k)W_N^{rk} \quad (1)$$

where $W_N = e^{-2\pi j/N}$. One can formulate the radix-8 representation in the following manner:

Let, $N = 8T$, $r = s + Tt$ and $k = l + 8m$, where, $s, l \in \{0, 1, \dots, 7\}$ and $m, t \in \{0, 1, \dots, T-1\}$. Applying these values in equation (1) and simplifying one gets,

$$A(s + Tt) = \sum_{l=0}^7 W_8^{lt} [W_{8T}^{sl} \sum_{m=0}^{T-1} B(l + 8m)W_T^{sm}] \quad (2)$$

For $N = 64$, $T = 8$. Thus, the 64-point FFT can be expressed as

$$A(s + 8t) = \sum_{l=0}^7 [W_{64}^{sl} \sum_{m=0}^7 B(l + 8m)W_8^{sm}] W_8^{lt} \quad (3)$$

Thus, the 64-point FFT can be computed by first taking 8-point FFT of the appropriate data slot (described in equation (3)) then multiplying them with 8 interdimensional constants and once again taking 8-point FFT of the resultant data.

The IFFT can be performed by first swapping the real and imaginary parts of the incoming data and then performing the forward FFT on them and once again swapping the real and imaginary parts of the data at the finale. This method allows one to perform the IFFT without changing any internal coefficients and thus, resulting into more efficient hardware implementation.

3. Architectural description

The basic architecture of the proposed 64-point FFT/IFFT module is shown in Figure 1. It utilizes two input buffers, one 8-point FFT module, an internal buffer and four multipliers. According to the specification IEEE 802.11a and ETSI Bran, the FFT block receives the data every 4 μ sec for duration of 3.2 μ sec. in serial manner. To satisfy this constraint, we used two input buffers. The input data slots are stored alternately in these buffers and the 8-point FFT module switches from one buffer to another to fetch new set of data as soon as the computation of 64-point FFT for a particular data slot is completed.

After computation of first 8-point FFT on the initial input data sequence, the resultant data undergoes the interdimensional constant multiplication operation. The multiplied data are stored in an internal register 'cb' (shown in Figure 1) from where they are rerouted to the 8-point FFT module in appropriate order to generate the final result. The final results are stored in the buffer cb once again from where the output is generated in serial manner.

The input mechanism, the internal computation process and the data output mechanism are carried out in pipelined fashion. The parallelism and pipelining introduced in this architecture is favorable from the power consumption point of view.

To perform the FFT and IFFT using the same architecture, we introduce a signal 'mode'. The logic LOW state of mode implies the forward FFT operation while its logic HIGH state enables one to perform IFFT operation. Two additional signal 'data_valid' and 'data_next' are kept that indicate input valid data and output valid data respectively. These signals are important from the point of view of the

integration of the complete wireless broadband communication systems. They indicate valid data operation condition to the previous and the next block of the system. Thus, this FFT/IFFT processor can be utilized as the stand-alone processor or it can be integrated with other required components to form a complete system.

4. Performance of the architecture

From the algorithmic point of view, the proposed architecture requires less number of arithmetic computations compared to that of the conventional Cooley-Tukey algorithm. This is shown in Table 1.

Algorithm	Complex Multiplication	Addition / subtraction
Cooley-Tukey [3]	192	1152
Proposed	49	994

Table 1. Comparison of the number of arithmetic operations with the Cooley-Tukey algorithm

The above comparison shows that the proposed architecture requires 25% real multiplication compared to that of the conventional approach. In terms of the number of addition, the proposed architecture requires 86% of those required in the conventional approach. This results into significant reduction of power dissipation.

The architecture is first coded in VHDL and then simulated using Mentor graphics' Quicksim simulator. For convenience, the simulation result of FFT for a pure cosine function input is shown in Figure 2(a). The result of IFFT on the resulting data is shown in Figure 2(b) that shows the functional correctness of the architecture. The architecture is synthesized for 0.25 μ m CMOS technology at 20 MHz clock frequency using Synopsis Design Analyzer tool. The synthesized circuit is simulated using Mentor graphics' Modelsim simulator that once again exhibits the correctness of the structure. The synthesis result shows that the area consumption of the complete FFT structure is 4.9 mm² that is equivalent to 81.666K inverter count at that technology. At the operating frequency of 20 MHz the power consumption of the whole structure is 78.5169 mW. At 20 MHz clock frequency the core architecture is capable to compute 64-point FFT/IFFT within 2.8 μ sec. However, with the serial input and serial output circuitry, it completes the computation of the

same in 4 μ sec. These figures indicates that the proposed architecture is highly suitable for application in OFDM based wireless broadband communication systems.

5. Conclusion

A FFT/IFFT processor that satisfies the specification of IEEE 802.11a and ETSI Bran is described in this article. The architecture gives advantage in terms of area, timing and power dissipation. The proposed one can be used as a stand-alone processor or can be integrated with other components to construct a complete wireless broadband communication system.

References

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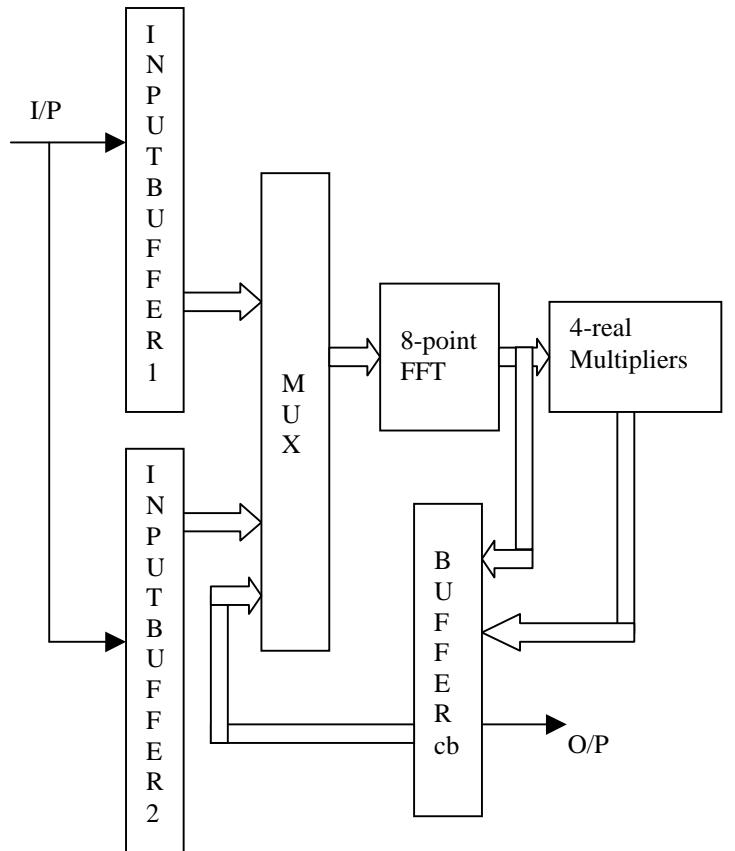


Figure 1. The basic architecture of the FFT/IFFT processor.

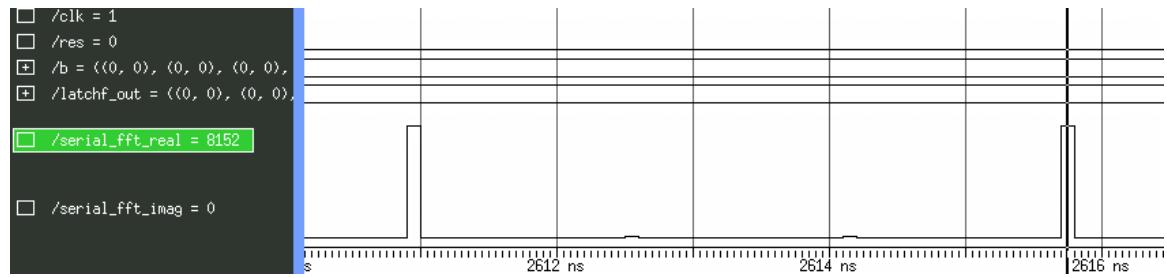


Figure 2(a). The simulation result for FFT on a pure cosine wave input.

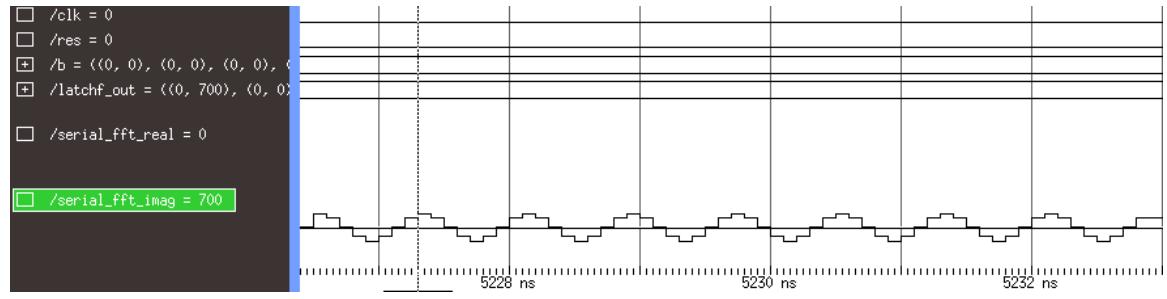


Figure 2(b). The simulation result for IFFT on the data of Figure 2(a).