# **Reducing Interconnect Cost in NoC through Serialized Asynchronous Links**\*

Simon Ogg<sup>1</sup>, Enrico Valli<sup>2</sup>, Crescenzo D'Alessandro<sup>3</sup>, Alex Yakovlev<sup>3</sup>, Bashir Al-Hashimi<sup>1</sup>, Luca Benini<sup>2</sup> <sup>1</sup>University of Southampton, <sup>2</sup>University of Bologna, <sup>3</sup>Newcastle University {so04r, bmah}@ecs.soton.ac.uk

### Abstract

This work investigates the application of serialization as a means of reducing the number of wires in NoC combined with asynchronous links in order to simplify the clocking of the link. Throughput is reduced but savings in routing area and reduction in power could make this attractive.

## **1. Introduction and Motivation**

As multiprocessor SoC solutions increase there are benefits to provide a scalable on chip communication structure such as NoC. Interconnect cost, in terms of the number of wires required between switches, could also be considerable in NoC structures since each switch is connected by a point-to-point link to a neighboring switch. The high cost of parallel links has been shown in [1] when inter-wiring spacing, shielding and repeaters are considered. The number of links in NoC will grow as more cores are integrated into a system. This work proposes the application of serialization as a means of reducing the interconnect cost in NoC.

### 2. Proposed Link & Results

The link, shown in Figure 1, has several blocks; synchronous/asynchronous converter interfaces (1&5), asynchronous serializer (2) and de-serializer (4), and wire buffers (3). The implementation uses a bundled request with the data. The synchronous/asynchronous interfaces uses a FIFO mechanism to pass data between the synchronous and asynchronous domains. The serializer and de-serializer split each 32 bit flit into smaller bit slices which are then sent serially along the buffered wires. The buffered wires allow pipelining of the bit slices to improve throughput.



The synchronous 32 bit wide link was compared to our proposed asynchronous 4 and 8 bit wide link. All circuits were simulated with Cadence Spectre using ST 0.12µm technology. The logic area cost for the synchronous implementation is 15850  $\mu$ m<sup>2</sup>. For the asynchronous 8 and 4 bit wide the logic area cost is 18900  $\mu$ m<sup>2</sup> and 18950  $\mu$ m<sup>2</sup> respectively. Figure 2 shows for a wire length of 1000  $\mu$ m wiring area of the synchronous link is reduced from 30000  $\mu$ m<sup>2</sup> down to 7500  $\mu$ m<sup>2</sup> and 3750  $\mu$ m<sup>2</sup> for the asynchronous 8 and 4 bit wide links respectively. Throughput in the asynchronous links is limited due to need to acknowledge each transfer, the link saturates 207 MFlits/s for the 8 bit wide link. Figure 3 shows power in the 8 bit wide asynchronous link (I3) is up to 25% lower compared to the synchronous link (I1) depending on link usage. Power in the link is dominated by the synchronous/asynchronous converters.





A feasible serialized asynchronous link has been demonstrated which lowers the point to point wiring interconnect cost. Throughput is limited due to the pertransfer acknowledgement scheme and the authors are currently investigating ways to improve this.



#### 3. References

[1] A. Morgenshtein, I. Cidon,, "Comparative analysis of serial vs parallel link in NoC", *in International Symposium on SoC*, Finland, 04, pp. 185-186.

<sup>\*</sup> This work is funded by EPSRC (UK) grant EP/C512804/1 and is greatly acknowledged.