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NEAR-CAPACITY TRANSCEIVER DESIGN USING EXIT-CURVE FITTING: THREE-STAGE TURBO DETECTION OF IRREGULAR CONVOLUTIONAL CODED JOINT SPHERE-PACKING MODULATION AND SPACE-TIME CODING

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Abstract - **Conventional two-stage turbo-detected schemes typically suffer from a Bit Error Rate (BER) floor, preventing them from achieving infinitesimally low BER values, especially, when the inner coding stage is of non-recursive nature. We circumvent this deficiency by proposing a three-stage turbo-detected Sphere Packing (SP) aided Space-Time Block Coding (STBC) STBC-SP scheme, where a rate-1 recursive inner precoder is employed to avoid having a BER floor. The convergence behaviour of this serially concatenated scheme is investigated with the aid of 3D Extrinsic Information Transfer (EXIT) Charts. Furthermore, the capacity of the STBC-SP scheme is shown and an algorithm is proposed for calculating a tighter upper bound on the maximum achievable bandwidth efficiency. The proposed three-stage turbo-detected scheme operates within about 1.0 dB of the capacity and within 0.5 dB of the maximum achievable bandwidth efficiency limit.**

1. INTRODUCTION

The concept of combining orthogonal transmit diversity designs with the principle of sphere packing was introduced by Su *et al.* in 2003 [1] in order to maximise the achievable coding advantage[1], where it was demonstrated that the proposed Sphere Packing (SP) aided Space-Time Block Coded (STBC) system, referred to here as STBC-SP, was capable of outperforming the conventional orthogonal design based STBC schemes of [2, 3]. *The ultimate rationale of this paper is to use a novel three-dimensional Extrinsic Information Transfer (EXIT)-chart-based technique to jointly design the two time-slots' STBC signal by near-optimally combining them into an iteratively detected SP symbol.*

The turbo principle of [4] was extended to multiple serially concatenated codes in 1998 [5]. The appeal of concatenated coding is that low-complexity iterative detection replaces the potentially more complex optimum decoder, such as that of [6]. In [7], the employment of the turbo principle was considered for iterative soft demapping in the context of bit-interleaved coded modulation (BICM), where a soft demapper was used between the multilevel demodulator and the channel decoder. In [8], a turbo coding scheme was proposed for the multiple-input multiple-output (MIMO) Rayleigh fading channel, where a block code was employed as an outer channel code, while an orthogonal STBC scheme was considered as the inner code. The iterative soft demapping principle of [7] was extended to STBC-SP schemes in [9], where it was demonstrated that turbo-detected STBC-SP schemes provide useful performance improvements over conventionally-modulated orthogonal design based STBC schemes. It was shown in [10] that a recursive inner code is needed in order to maximise the interleaver gain and to avoid the formation of a bit-error rate (BER) floor, when employing iterative decoding. This principle has been adopted by several authors designing serially concatenated schemes, where rate-1 inner codes were employed for designing low complexity turbo codes suitable for bandwidth and power limited systems having stringent BER requirements [11–13].

Recently, studying the convergence behaviour of iterative decoding has attracted considerable attention [14–17]. In [14], ten Brink proposed the employment of the so-called EXIT characteristics between a concatenated decoder's output and input for describing the flow of extrinsic information through the soft-in/soft-out constituent decoders. The computation of EXIT charts was further simplified in [15] to a time average, for scenarii when the PDFs of the communicated information at the input and output of the constituent decoders are both symmetric and ergodic. The concept of EXIT chart analysis has been extended to three-stage concatenated systems in [16, 17].

In this paper, we propose a capacity-approaching three-stage turbo-detected STBC-SP scheme, where iterative decoding is carried out between three constituent decoders, namely an STBC-SP demapper, an inner rate-1 recursive A Posteriori Probability (APP)-based decoder and an outer APP-based decoder. We first show the capacity limit for STBC-SP schemes. Then, an upper bound on the maximum achievable rate is calculated, based on the EXIT charts of the STBC-SP demapper. ***At a spectral efficiency of $\eta = 1$ bits/s/Hz, the upper bound of the maximum achievable rate is within 0.5 dB of the capacity, and our proposed three-stage scheme operates within 1.0 dB of the capacity. The rationale of the proposed architecture is explicit: (1) SP modulation maximises the coding advantage of the transmission scheme by jointly designing and detecting the SP symbols hosting the two time-slots' STBC symbols; (2) the inner rate-1 recursive decoder maximises the interleaver gain and hence avoids having a BER floor; and (3) the outer irregular convolutional codes (IRCCs) [15, 18] minimise the area of the EXIT chart's convergence tunnel and hence facilitate near-capacity operation [19].***

This paper is organised as follows. In Section 2, a brief description of our three-stage system is presented. Section 3 provides our 3D EXIT chart analysis along with its simplified 2D projections. The capacity of STBC-SP schemes is shown in Section 4, where an upper bound on the maximum achievable rate is also calculated based on the EXIT chart analysis. Our simulation results and discussions are provided in Section 5. Finally, we conclude in Section 6.

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[1]The diversity product or coding advantage was defined as the estimated gain over an uncoded system having the same diversity order as the coded system [1].

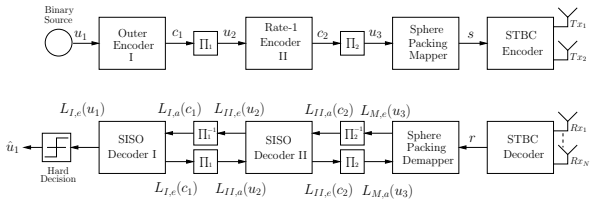

Figure 1: Three-stage serially concatenated system.

2. SYSTEM OVERVIEW

The schematic of the entire system is shown in Fig. 1, where the transmitted source bits $\mathbf{u}_1$ are encoded by the outer channel Encoder I having a rate of R_I. The outer channel encoded bits $\mathbf{c}_1$ are then interleaved by the first random bit interleaver, where the randomly permuted bits $\mathbf{u}_2$ are fed through the rate-1 Encoder II. The concatenated coded bits $\mathbf{c}_2$ at the output of the rate-1 encoder are interleaved by the second random bit interleaver, producing the permuted bits $\mathbf{u}_3$. After channel interleaving, the sphere packing mapper first maps blocks of B channel-coded bits $\mathbf{b} = b_{0,\ldots,B-1} \in \{0,1\}$ to the $L = 2^B$ number of legitimate four-dimensional sphere packing modulated symbols $\mathbf{s}^l \in S$, where $S = \{\mathbf{s}^l = [a_{l,1}\ a_{l,2}\ a_{l,3}\ a_{l,4}] \in \mathbb{R}^4 : 0 \le l \le L-1\}$ constitutes a set of L legitimate constellation points from the lattice D_4 [20] having a total energy of $E \triangleq \sum_{l=0}^{L-1}(|a_{l,1}|^2 + |a_{l,2}|^2 + |a_{l,3}|^2 + |a_{l,4}|^2)$. The STBC encoder then maps each sphere packing modulated symbol $\mathbf{s}^l$ to a space-time signal $\mathbf{C}_l$ as [1, 9]:

$$\mathbf{C}_l = \sqrt{\frac{2L}{E}}\mathbf{G}_2(x_{l,1}, x_{l,2}), \qquad 0 \le l \le L-1, \tag{1}$$

where $x_{l,1}$ and $x_{l,2}$ are complex-valued symbols constructed from the 4-dimensional real-valued coordinates of the SP symbol $\mathbf{s}^l$ in order to maximise the coding advantage of the space-time signal $\mathbf{C}_l$ [1], since the lattice D_4 has the best minimum Euclidean distance in the four-dimensional real-valued Euclidean space $\mathbb{R}^4$ [20]. Specifically, $x_{l,1}$ and $x_{l,2}$ may be written as $\{x_{l,1}, x_{l,2}\} = T_{sp}(a_{l,1}, a_{l,2}, a_{l,3}, a_{l,4}) = \{a_{l,1} + ja_{l,2}, a_{l,3} + ja_{l,4}\}$. Furthermore, $\mathbf{G}_2(x_{l,1}, x_{l,2})$ is the space-time transmission matrix given by [2]

$$\mathbf{G}_2(x_1, x_2) = \begin{bmatrix} x_1 & x_2 \\ -x_2^* & x_1^* \end{bmatrix}, \tag{2}$$

where the rows and columns of Eq. (2) represent the temporal and spatial dimensions, corresponding to two consecutive time slots and two transmit antennas, respectively.

In this treatise, we considered a correlated narrowband Rayleigh fading channel, associated with a normalised Doppler frequency of $f_D = f_d T_s = 0.1$, where f_d is the Doppler frequency and T_s is the symbol period. The complex-valued fading envelope is assumed to be constant across the transmission period of a space-time coded symbol spanning $T = 2$ time slots. The complex Additive White Gaussian Noise (AWGN) of $n = n_I + jn_Q$ is also added to the received signal, where n_I and n_Q are two independent zero-mean Gaussian random variables having a variance of $\sigma_n^2 = \sigma_{n_I}^2 = \sigma_{n_Q}^2 = N_0/2$ per dimension, where $N_0/2$ represents the double-sided noise power spectral density expressed in W/Hz.

As shown in Fig. 1, the received complex-valued symbols are first decoded by the STBC decoder in order to produce the received SP soft-symbols $\mathbf{r}$, where each SP symbol represents a block of B coded bits [9]. Then, iterative demapping/decoding is carried out between the SP demapper, APP-based soft-in/soft-out (SISO) module II and APP-based SISO module I, where extrinsic information is exchanged between the three constituent demapper/decoder modules. More specifically, $L_{\cdot,a}(\cdot)$ in Fig. 1 represents the $a\ priori$ information, expressed in terms of the log-likelihood ratios (LLRs) of the corresponding bits, whereas $L_{\cdot,e}(\cdot)$ represents the $extrinsic$ LLRs of the corresponding bits. The iterative process is performed for a number of consecutive iterations. During the last iteration, only the LLR values $L_{I,e}(\mathbf{u_1})$ of the original uncoded systematic information bits $\mathbf{u}_1$ are required, which are passed to a hard decision decoder in order to determine the estimated transmitted source bits $\hat{\mathbf{u}}_1$ as shown in Fig. 1.

3. EXIT CHART ANALYSIS

3.1. Preliminaries

The main objective of employing EXIT charts [14], is to predict the convergence behaviour of the iterative decoder by examining the evolution of the input/output mutual information exchange between the inner and outer decoders in consecutive iterations. The application of EXIT charts is based on the two assumptions that upon assuming large interleaver lengths, (1) the $a\ priori$ LLR values are fairly uncorrelated; (2) the $a\ priori$ LLR values exhibit a Gaussian PDF. In this section, the approach presented in [17] is adopted in order to provide the EXIT chart analysis of the proposed three-stage system of Fig. 1.

Let $I_{\cdot,a}(x)$, $0 \le I_{\cdot,a}(x) \le 1$, denote the mutual information (MI) between the $a\ priori$ LLRs $L_{\cdot,a}(x)$ as well as the corresponding bits x and let $I_{\cdot,e}(x)$, $0 \le I_{\cdot,e}(x) \le 1$, denote the MI between the $extrinsic$ LLRs $L_{\cdot,e}(x)$ and the corresponding bits x, where the subscript $(\cdot)$ is used to distinguish the different constituent decoders, i.e. Decoder I, Decoder II and the SP demapper.

3.2. 3D EXIT Charts

As seen from Fig. 1, the input of Decoder II is constituted by the $a\ priori$ input $L_{II,a}(c_2)$ and the $a\ priori$ input $L_{II,a}(u_2)$ provided after bit-deinterleaving by the SP demapper and Decoder I, respectively. Therefore, the EXIT characteristic of Decoder II can be described by the following two EXIT functions [14, 17]:

$$I_{II,e}(c_2) = T_{II,c_2}(I_{II,a}(u_2), I_{II,a}(c_2)), \tag{3}$$
$$I_{II,e}(u_2) = T_{II,u_2}(I_{II,a}(u_2), I_{II,a}(c_2)), \tag{4}$$

which are illustrated by the 3D surfaces drawn in dotted lines in Figs. 2 and 3, respectively. On the other hand, the EXIT characteristic of the SP demapper as well as that of Decoder I are each dependent on a single $a\ priori$ input, namely on $L_{M,a}(u_3)$ and $L_{I,a}(c_1)$, respectively, both of which are provided by the rate-1 Decoder II after appropriately ordering the bits, as seen in Fig. 1. The EXIT characteristic of the SP demapper is also dependent on the E_b/N_0 value. Consequently, the corresponding EXIT functions for the SP demapper and Decoder I, respectively, may be written as

$$I_{M,e}(u_3) = T_{M,u_3}(I_{M,a}(u_3), E_b/N_0), \tag{5}$$
$$I_{I,e}(c_1) = T_{I,c_1}(I_{I,a}(c_1)), \tag{6}$$

which are illustrated by the 3D surfaces drawn in solid lines in Figs. 2 and 3, respectively.

Eqs. (4) to (6) may be represented with the aid of two 3D EXIT charts. More specifically, the 3D EXIT chart of Fig. 2 can be used to plot Eq. (3) and Eq. (5), which describe the EXIT relation between the SP demapper and Decoder II. Similarly, the 3D EXIT chart of Fig. 3 can be used to describe the EXIT relation between Decoder II and Decoder I by plotting Eq. (4) and Eq. (6). Figs. 2 and 3 show an example of these 3D EXIT charts, when Encoder I is a half-rate memory-1 recursive systematic convolutional (RSC) code having octally represented generator polynomials of

$(G_r, G) = (3, 2)_8$, where G_r is the feedback polynomial, while Encoder II is a simple rate-1 accumulator, described by the pair of octal generator polynomials $(G/G_r) = (2/3)_8$.

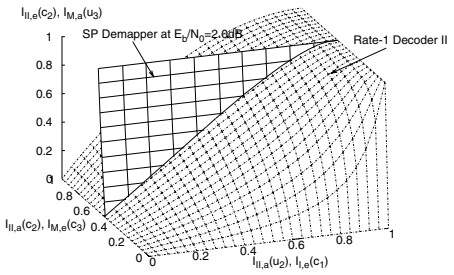

Figure 2: 3D EXIT chart of Decoder II and the SP demapper at $E_b/N_0 = 2.0$ dB.

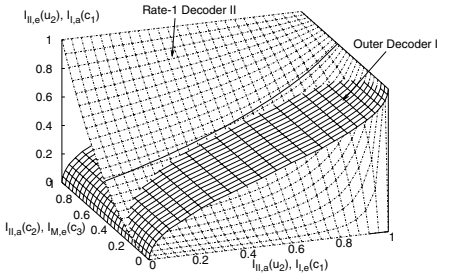

Figure 3: 3D EXIT chart of Decoder II and Decoder I with projection from Fig. 2.

3.3. 2D EXIT Chart Projections

The 3D EXIT charts of Figs. 2 and 3 are somewhat cumbersome to interpret as well as to plot. Hence in this section we derive their unique and unambiguous 2D representations, which can be interpreted in the usual way.

The intersection of the surfaces in Fig. 2, shown as a thick solid line, portrays the best achievable performance, when exchanging mutual information between the SP demapper and the rate-1 Decoder II for different fixed values of $I_{II,a}(u_2)$ spanning the range of $[0, 1]$. Each $(I_{II,a}(u_2),\ I_{II,a}(c_2),\ I_{II,e}(c_2))$ point belonging to the intersection line in Fig. 2 uniquely specifies a 3D point $(I_{II,a}(u_2), I_{II,a}(c_2), I_{II,e}(u_2))$ in Fig. 3, according to the EXIT function of Eq. (4). Therefore, the line corresponding to the $(I_{II,a}(u_2), I_{II,a}(c_2), I_{II,e}(c_2))$ points along the thick line of Fig. 2 is projected to the solid line shown in Fig. 3, while the 2D projection of the solid line in Fig. 3 at $I_{II,a}(c_2) = 0$ onto the plane spanned by the lines $(I_{II,a}(u_2), I_{II,e}(u_2))$ and $(I_{I,e}(c_1), I_{I,a}(c_1))$ is shown in Fig. 4-a, represented by the dotted line at $E_b/N_0 = 2.0$ dB. This projected EXIT curve may be written as

$$I_{II,e}(u_2) = T^p_{II,u_2}(I_{II,a}(u_2), E_b/N_0). \tag{7}$$

Projected 2D EXIT charts of similar nature will be used throughout the rest of the paper for the sake of describing the convergence behaviour of the three-stage turbo-detected STBC-SP scheme. More details on the related 3D-to-2D EXIT chart projection are provided in [17].

Fig. 4-a shows the 2D-projected EXIT curve of the SP demapper, when operating at $E_b/N_0 = 2.0$ dB and employing Anti-Gray Mapping[2] (AGM-1) scheme, which is described in Appendix A and in Table 1. The figure also shows the 2D-projected EXIT curve of the outer RSC Decoder I and the 2D-projected EXIT curves of the combined SP demapper and the rate-1 Decoder II at different E_b/N_0 values, when employing AGM-1 of Table 1. Observe in Fig. 4-a that an open convergence tunnel is taking shape for the three-stage scheme upon increasing the Signal-to-Noise Ratio (SNR) beyond $E_b/N_0 = 2.0$ dB. This implies that according to the predictions of the 2D EXIT chart seen in Fig. 4-a, the iterative decoding process is expected to converge to the $(1.0, 1.0)$ point and hence an infinitesimally low BER may be attained beyond $E_b/N_0 = 2.0$ dB. By contrast, for the traditional two-stage turbo-detected STBC-SP scheme, there would be a BER floor preventing it from achieving an infinitesimally low BER due to the non-recursive nature of the SP demapper, which also prevents the intersection of the EXIT curves of the SP demapper and the outer RSC Decoder I from reaching the $(1.0, 1.0)$ point of convergence, despite increasing the SNR or the number of iterations. In contrast to this, the three-stage scheme of Fig. 1 becomes capable of achieving an infinitesimally low BER, as suggested by the EXIT-chart predictions of Fig. 4-a.

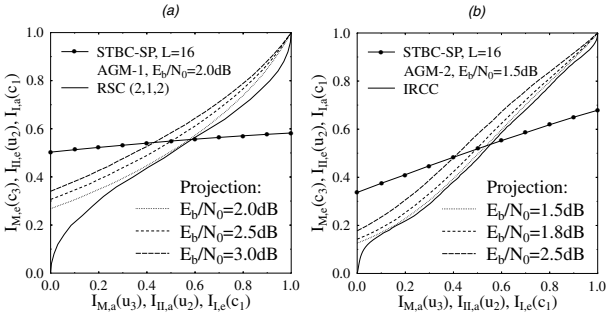

Figure 4: 2D projection of the EXIT charts of the three-stage STBC-SP scheme. (a) RSC-coded STBC-SP scheme with AGM-1 of Table 1. (b) IRCC-coded STBC-SP scheme with AGM-2 of Table 1.

3.4. EXIT Tunnel-Area Minimisation for Near-Capacity Operation

In this section we will exploit the well-understood properties of conventional 2D EXIT charts that a narrow and open EXIT-tunnel represents a near-capacity performance. Therefore, we invoke Irregular Convolutional Codes (IRCCs) for the sake of appropriately shaping the EXIT curves by minimising the area within the EXIT-tunnel using the procedure of [15, 18].

Let $\mathcal{A}_I$ and $\bar{\mathcal{A}}_I$ be the areas under the EXIT-curve $T_{I,c_1}(i)$ of Eq. (6) and its inverse $T^{-1}_{I,c_1}(i)$, $i \in [0, 1]$, respectively, which is expressed as:

$$\mathcal{A}_I = \int_0^1 T_{I,c_1}(i)\mathrm{d}i, \qquad \bar{\mathcal{A}}_I = \int_0^1 T^{-1}_{I,c_1}(i)\mathrm{d}i \ = \ 1 - \mathcal{A}_I. \tag{8}$$

Similarly, the area $\mathcal{A}^p_{II}$ is defined under the EXIT-curve $T^p_{II,u_2}(i)$ of Eq. (7). It was observed in [15, 21] that for the APP-based outer Decoder I, the area $\bar{\mathcal{A}}_I$ maybe approximated by $\bar{\mathcal{A}}_I \approx R_I$, where the equality $\bar{\mathcal{A}}_I = R_I$ was later shown in [19] for the family of Binary Erasure Channels (BECs). The area property of $\bar{\mathcal{A}}_I \approx R_I$ implies that the lowest SNR convergence threshold occurs, when we have $\mathcal{A}^p_{II} = R_I + \epsilon$, where ϵ is an infinitesimally small number, provided that the following convergence constraints hold [18]:

$$T^p_{II,u_2}(0) > 0,\ T^p_{II,u_2}(1) = 1,\ T^p_{II,u_2}(i) > T^{-1}_{I,c_1}(i),\ \forall i \in [0, 1). \tag{9}$$

Observe, in Fig. 4-a, however that there is a 'larger-than-necessary' tunnel area between the projected EXIT curve $T^p_{II,u_2}(i)$ and the

[2] Anti-Gray Mapping (AGM) is used here to refer to any non-Gray mapping scheme, while the specific scheme AGM-1 and other AGM schemes employed in this paper are described in Appendix A and Table 1.

EXIT curve $T_{I,c_1}^{-1}(i)$ of the outer 1/2-rate RSC code at $E_b/N_0 = 2.0$ dB. This implies that the BER curve is farther from the achievable capacity than necessary, despite the fact that the specific bit-to-SP-symbol mapping scheme of AGM-1 and the 1/2-rate RSC code employed in Fig. 4-a were specifically optimised for convergence at a low E_b/N_0 value. More quantitatively, the area under the projected EXIT curve $T_{II,u_2}^p(i)$ is $\mathcal{A}_{II}^p \approx 0.55$ at $E_b/N_0 = 2.0$ dB, which is larger than the outer code rate of $R_I = 0.50$. Therefore, according to Fig. 4-a and to the area property of $\bar{\mathcal{A}}_I \approx R_I$, a lower E_b/N_0 convergence threshold may be attained, provided that the constraints outlined in Eq. (9) are satisfied. In other words, the EXIT curve $T_{I,c_1}^{-1}(i)$ of the outer code should match the 2D-projected EXIT curve $T_{II,u_2}^p(i)$ of Fig. 4-a more closely. Hence we will invoke IRCCs [15, 18] as outer codes that exhibit flexible EXIT characteristics, which can be optimised to more closely match the 2D-projected EXIT curve $T_{II,u_2}^p(i)$ of Fig. 4-a, rendering the near-capacity code optimisation a simple curve-fitting process.

An IRCC scheme constituted by a set of $P = 17$ subcodes was constructed in [18] from a systematic 1/2-rate memory-4 mother code defined by the octally represented generator polynomials $(G_r, G) = (23, 35)_8$. Each of the $P = 17$ subcodes encodes a specific fraction of the uncoded bits determined by the weighting coefficient, α_i, $i = 0, \ldots, P$. Hence the coefficients α_i are optimised with the aid of the iterative algorithm of [15], so that the EXIT curve of the resultant IRCC closely matches the 2D-projected EXIT curve $T_{II,u_2}^p(i)$ at the specific E_b/N_0 value, where we have $\mathcal{A}_{II}^p \approx 0.50$. Observe in Fig. 4-b that we have $\mathcal{A}_{II}^p \approx 0.51$ at $E_b/N_0 = 1.5$dB, indicating that this E_b/N_0 value is close to the lowest attainable convergence threshold, when employing a 1/2-rate outer code. Fig. 4-b also shows the 2D-projected EXIT curve of the resultant IRCC, where the optimised weighting coefficients are as follows:

$$\begin{aligned}[\alpha_1, \ldots, \alpha_{17}] &= [0,\ 0.0559066,\ 0.236757,\ 0,\ 0,\ 0,\\ &\quad 0.23844,\ 0,\ 0,\ 0.0306247,\ 0,\ 0.205574,\\ &\quad 0, 0,\ 0.110076,\ 0,\ 0.122621]. \qquad (10)\end{aligned}$$

4. CAPACITY AND MAXIMUM ACHIEVABLE RATE

The channel capacity and bandwidth efficiency valid for STBC schemes using N_D-dimensional so-called L-orthogonal signalling [22] over the Discrete-input Continuous-output Memoryless Channel (DCMC) [23] was derived in [24]. Fig. 5 shows the DCMC bandwidth efficiency $\eta_{DCMC}^{STBC-SP}$ of the 4-dimensional SP modulation assisted STBC scheme for $L = 16$, where the Continuous-Input Continuous-Output Memoryless Channel (CCMC) [23] capacity of the MIMO scheme is given by [25]. More specifically, Fig. 5 demonstrates that at a bandwidth efficiency of $\eta = 1$ bit/s/Hz, the capacity limit for the DCMC STBC-SP scheme employing $N_t = 2$ transmit and $N_r = 1$ receive antennas is $E_b/N_0 = 0.78$ dB. The EXIT chart analysis of Fig. 4-b predicts that our three-stage system will converge at $E_b/N_0 = 1.5$ dB, i.e. within 0.72 dB from the capacity limit. The dotted curve referring to the maximum achievable rate of the three-stage turbo-detected STBC-SP scheme is discussed next.

A tighter upper limit on the maximum achievable rate of the system can be calculated based on the area property of $\bar{\mathcal{A}}_I \approx R_I$ of EXIT charts as discussed in Section 3.4. More explicitly, it was shown in Section 3.4 that the outer Decoder I may have a maximum rate of $R_I^{max} \approx \mathcal{A}_{II}^p$ at a specific E_b/N_0 value, where $\mathcal{A}_{II}^p$ is the area under the projected EXIT curve of the SP demapper and the rate-1 Decoder II of Eq. (7). Therefore, if $\mathcal{A}_{II}^p$ is calculated for different E_b/N_0 values, the maximum achievable bandwidth

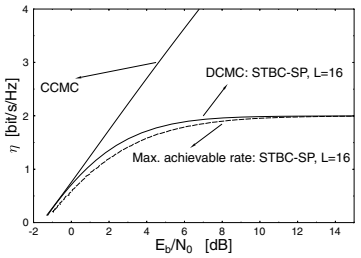

Figure 5: Bandwidth efficiency of the STBC-SP based system with $L = 16$, when employing $N_t = 2$ transmit antennas and $N_r = 1$ receive antenna.

efficiency may be formulated as a function of the E_b/N_0 value as follows

$$\begin{aligned}\eta_{max}(\underline{E_b/N_0}) &= B \cdot R_{STBC-SP} \cdot R_I^{max}\\ &\approx B \cdot R_{STBC-SP} \cdot \mathcal{A}_{II}^p(E_b/N_0) \quad \text{[bit/s/Hs]},\end{aligned} \qquad (11)$$

where $B = \log_2(L)$ is the number of bits per SP symbol and $R_{STBC-SP} = \frac{1}{2}$, since $T = 2$ time slots are needed to transmit one SP symbol according to Eqs. (1) and (2). Additionally, $\underline{E_b/N_0}$ and E_b/N_0 are related as follows

$$\underline{E_b/N_0} = E_b/N_0 + 10\log\left(\frac{R_o}{\mathcal{A}_{II}^p(E_b/N_0)}\right) \quad \text{[dB]}, \qquad (12)$$

where R_o is the original outer code rate used when generating the 2D-projected EXIT curves of the SP demapper and the rate-1 Decoder II of Eq. (7) corresponding to the different $\mathcal{A}_{II}^p$ values. A simple procedure may be used to calculate the maximum achievable bandwith efficiency of Eq. (11). For computational simplicity, the area $\mathcal{A}_M$ under the EXIT curve T_{M,u_3} of Eq. (5) may be used instead of the area $\mathcal{A}_{II}^p$ under the 2D-projected EXIT curve T_{II,u_2}^p of Eq. (7), since $\mathcal{A}_M = \mathcal{A}_{II}^p$, when $R_{II} = 1$. More specifically, the maximum achievable bandwith efficiency of Eq. (11) can be calculated using the following procedure for $E_b/N_0 \in [\rho_{min}, \rho_{max}]$, assuming that R_o is an arbitrary rate and ϵ is a small constant.

Algorithm 1 (*Maximum Achievable Bandwidth Efficiency using EXIT Charts):*

Step 1: Let $R_I = R_o$.

Step 2: Let $E_b/N_0 = \rho_{min}$ dB.

Step 3: Calculate N_0.

Step 4: Let $I_{M,a}(u_3) = 0$.

Step 5: Activate the SP demapper.

Step 6: Save $I_{M,e}(u_3) = T_{M,u_3}(I_{M,a}(u_3), E_b/N_0)$.

Step 7: Let $I_{M,a}(u_3) = I_{M,a}(u_3) + \epsilon$. If $I_{M,a}(u_3) \leq 1.0$, go to Step 5.

Step 8: Calculate $\mathcal{A}_M(E_b/N_0) = \int_0^1 T_{M,u_3}(i, E_b/N_0)\,\mathrm{d}i$.

Step 9: Calculate $\underline{E_b/N_0}$ using Eq. (12).

Step 10: Save $\eta_{max}(\underline{E_b/N_0})$ of Eq. (11).

Step 11: Let $E_b/N_0 = E_b/N_0 + \epsilon$. If $E_b/N_0 \leq \rho_{max}$ dB, go to Step 3.

Step 12: Output $\eta_{max}(\underline{E_b/N_0})$ from Step 10.

Observe that ρ_{min} and ρ_{max} are adjusted accordingly in order to produce the desired range of the resultant $\underline{E_b/N_0}$ values. Furthermore, the output of Algorithm 1 is independent of the specific choice of R_o, since Eq. (12) would always adjust the E_b/N_0 values, regardless of R_o. For example, R_o may be set to the desired final R_I to be employed in the three-stage system.

The resultant maximum achievable bandwidth efficiency is demonstrated in Fig. 5, which is slightly lower than the bandwidth efficiency calculated according to [24], i.e. we have $\eta_{max} < \eta_{DCMC}^{STBC-SP}$. Observe that the bandwidth efficiency calculated according to [24] and using the EXIT charts as well as Eq. (11) were only proven to be equal for the family of BECs [19]. Nonetheless, similar trends have been observed for both AWGN and Inter-Symbol-Interference (ISI) channels [16, 18], when APP-based decoders are used for all decoder blocks [19]. However, the discrepancy between the two bandwidth efficiency curves shown in Fig. 5 is due to the fact that the SP demapper is not an APP-based decoder. Nevertheless, the bandwidth efficiency calculated based on the EXIT charts using Eq. (11) and Algorithm 1 constitutes a tighter bound on the maximum achievable bandwidth efficiency of the system.

Fig. 5 shows that at a bandwidth efficiency of $\eta = 1$ bit/s/Hz, the capacity limit for the STBC-SP scheme is about $E_b/N_0 = 1.3$ dB, which is within 0.2 dB from the prediction of our EXIT chart analysis seen in Fig. 4-b, where convergence is predicted at $E_b/N_0 = 1.5$ dB.

5. RESULTS AND DISCUSSIONS

5.1. System Parameters

Without loss of generality, we considered a sphere packing modulation scheme associated with $L = 16$ using two transmit and a single receiver antenna in order to demonstrate the performance improvements achieved by the proposed system. The communication channel is described in Section 2, while the outer Encoder I is a half-rate memory-4 IRCC constructed using $P = 17$ subcodes according to the weighting coefficients of Eq. (10). Encoder II is a simple rate-1 accumulator, described by the pair of octal generator polynomials $(G/G_r) = (2/3)_8$. A three-stage iteration involves the following decoder activation sequence: (SP Demapper - Decoder II - SP Demapper - Decoder II - Decoder I - Decoder II). The overall system throughput is 1 bit/symbol.

5.2. Decoding Trajectory and BER Performance

EXIT chart based convergence predictions are usually verified by the actual iterative decoding trajectory. Fig. 4-b shows that the three-stage turbo-detected STBC-SP scheme is expected to converge at $E_b/N_0 = 1.5$ dB, where convergence to the $(1.0, 1.0)$ point requires an excessive number of three-stage iterations. However, convergence to the $(1.0, 1.0)$ point becomes more feasible for $E_b/N_0 > 1.5$dB. Fig. 6 illustrates the actual decoding trajectory of the three-stage turbo-detected STBC-SP scheme of Fig. 1 at $E_b/N_0 = 1.8$ dB, when using an interleaver depth of $\mathcal{D} = 10^6$ bits and 33 three-stage iterations. The zigzag-path seen in Fig. 6 represents the actual extrinsic information transfer between the SP demapper and the rate-1 Decoder II on one hand and the outer IRCC Decoder I on the other.

Fig. 7 compares the performance of the proposed three-stage IRCC-coded STBC-SP scheme employing anti-Gray mapping (AGM-2) against that of an identical-throughput 1 Bit Per Symbol (1BPS) uncoded STBC-SP scheme [1] using $L = 4$ and against Alamouti's conventional $\mathbf{G}_2$-BPSK scheme [2]. The system is also benchmarked against a two-stage RSC-coded STBC-SP scheme [9], when employing the system parameters outlined in Section 5.1 and using an interleaver depth of $\mathcal{D} = 10^6$ bits. Fig. 7 specifically demonstrates that the proposed three-stage turbo-detected scheme is capable of achieving infinitesimally low BER values, where its performance is not limited by a BER floor, which is in contrast to the two-stage turbo-detected STBC-SP scheme. Observe that the two-stage turbo-detected STBC-SP scheme uses

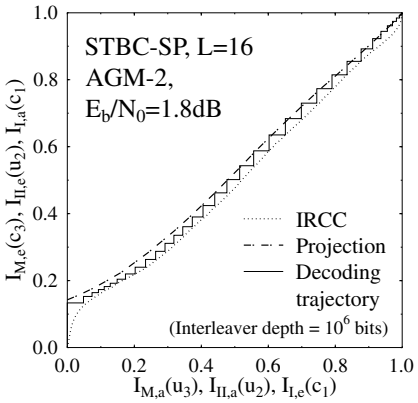

Figure 6: Decoding trajectory of the three-stage IRCC-coded STBC-SP scheme, when employing the anti-Gray mapping AGM-2 of Table 1 in combination with the system parameters outlined in Section 5.1 and operating at $E_b/N_0 = 1.8$ dB with an interleaver depth of $\mathcal{D} = 10^6$ bits after 33 three-stage iterations.

only 10 iterations since the advantage of employing any further iterations diminishes owing to the presence of a BER floor. Explicitly, Fig. 7 demonstrates that a coding advantage of about 22.2 dB was achieved at a BER of 10^{-5} after 28 iterations by the three-stage turbo-detected STBC-SP system over both the uncoded STBC-SP [1] and the conventional orthogonal STBC design based [2, 3] schemes for transmission over the correlated Rayleigh fading channel considered. Additionally, a coding advantage of approximately 2.0 dB was attained over the 1BPS-throughput RSC-coded AGM-3 STBC-SP scheme [9] at the expense of an increased decoding complexity due to the employment of the rate-1 decoder and the additional three-stage iterations. According to Fig. 7, the three-stage turbo-detected STBC-SP scheme operates within approximately 1.0 dB from the capacity limit calculated from [24] and 0.5 dB from the maximum achievable bandwidth efficiency limit of Eq. (11).

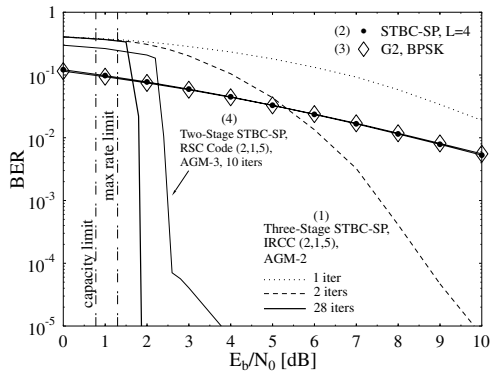

Figure 7: Performance comparison of the anti-Gray mapping AGM-2$^{(1)}$ based IRCC-coded three-stage STBC-SP scheme in conjunction with $L = 16$ against an identical-throughput 1 bit/symbol (BPS) uncoded STBC-SP scheme$^{(2)}$ using $L = 4$ and against Alamouti's conventional $\mathbf{G}_2$-BPSK scheme$^{(3)}$ as well as against a two-stage RSC-coded STBC-SP scheme$^{(4)}$, when employing the system parameters outlined in Section 5.1 and using an interleaver depth of $D = 10^6$ bits.

6. CONCLUSION

We proposed a three-stage serial concatenated turbo-detected STBC-SP scheme that is capable of achieving infinitesimally low

BER values, where the performace is not limited by a BER floor, which is routinely encountered in conventional two-stage systems. The convergence behaviour of the three-stage system was analysed with the aid of novel 3D EXIT charts and their 2D projections [16, 17]. With the advent of 2D projections, an IRCC [15, 18] was constructed for the sake of matching the projected EXIT curve of the SP demapper and the rate-1 inner decoder leading to a near-capacity performance. The capacity of the STBC-SP scheme was calculated and a procedure was proposed for calculating a tighter upper bound on the maximum achievable bandwidth efficiency of the three-stage system using EXIT chart analysis. Our proposed three-stage scheme operated within about 1.0 dB from the capacity limit and within 0.5 dB from the maximum achievable bandwidth efficiency limit.

Appendix A
Anti-Gray Mapping Schemes for Sphere Packing Modulation of Size $L = 16$

In this appendix, the different anti-Gray mapping (AGM) schemes introduced in this paper for STBC-SP signal sets of size $L = 16$ are described. There are more than $L = 16$ legitimate SP symbols in the lattice D_4 and hence the required $L = 16$ SP symbols were chosen according to the minimum energy and highest minimum Euclidean distance (MED) criterion proposed in [9]. All mapping schemes described here use the same 16 optimum constellation points. More specifically, for all mapping schemes, constellation points of the lattice D_4 are given for each integer index $l = 0, 1, \ldots, 15$. The normalisation factor of these constellation points is $\sqrt{\frac{2L}{E}} = 1$. The constellation points corresponding to each mapping scheme are given in Table 1.

Points from D_4				Integer Index		
a_1	a_2	a_3	a_4	AGM-1	AGM-2	AGM-3
+1	−1	0	0	0	2	12
0	−1	−1	0	1	4	11
0	−1	+1	0	2	5	7
−1	−1	0	0	3	0	15
−1	0	0	+1	4	13	14
0	0	−1	+1	5	9	5
0	0	+1	+1	6	11	9
+1	0	0	+1	7	15	2
−1	0	0	−1	8	12	13
0	0	−1	−1	9	8	6
0	0	+1	−1	10	10	10
+1	0	0	−1	11	14	1
−1	+1	0	0	12	1	3
0	+1	−1	0	13	6	8
0	+1	+1	0	14	7	4
+1	+1	0	0	15	3	0

Table 1: Bit mappings for the different anti-Gray mapping schemes introduced for STBC-SP signals of size $L = 16$.

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