

Yield Predictive Model Characterization In Analog Circuit Design

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Abstract—A new technique is presented that produces a characterized yield-predictive model by incorporating yield into the goal function directly. We explore the trade off between performance functions and yield estimation during the design optimization process. Through the integration of yield into the optimization process, the trade off between the performance functions can be better treated that able to produce a higher yield. This concept together with full circuit simulation and global search algorithm provides a robust solution across process corners and parameter variations. Encouraging results have been obtained and an example is presented to demonstrate the technique.

I. INTRODUCTION

Statistical parameter variation in analog circuit design has become one of the important criteria and has attracted good attention in recent times. The reason for this is simple, as the transistor dimension decrease, the statistical variations of the devices become more prominent. Therefore this variations become increasingly significant especially in deep submicron design and must be considered in the design process. These statistical variations will estimate the yield of a circuit. A significant amount of research has been devoted to analog circuit synthesis [1] [2]. Most previous research work had developed several synthesis techniques to trade the accuracy of the optimization for the speed of operation [3], [5]-[11].

In this paper, we present a new fully simulation-based analog circuit design strategy which incorporates yield as the cost function in the optimization process. As a contrary to the previous approach which optimize the yield during post-design process, our strategy is to include yield in the beginning of the performance optimization. Here, yield is treated as one of the performance parameters. The optimization procedure is based on Genetic Algorithm taken from GALib library [6]. The paper is organized as follows. Section II briefly reviews previous work in analog circuit synthesis. Section III describes the proposed methodology and focuses on yield optimization approach. Results are given in section IV and finally concluding remarks are given in section V.

II. BACKGROUND

Previous work in analog circuit synthesis can be classified into three main categories, namely knowledge-based, equation-based and simulation-based.

Early work in analog synthesis is mostly based on knowledge-based techniques. Some of the synthesis tools that were developed based on this approach are BLADES [3] and OASYS [5]. BLADES used expert systems technology from a stored knowledge to create a complete analog design environment. The limitation of this approach lies in the sense of having to codify extensive circuit knowledge and design heuristics.

In an equation-based approach, explicit scripts of equation is used to evaluate each circuit candidate. A number of techniques have been attempted with this approach. OPASYN [6] uses simple analytical equations of OPAMP performance. Symbolic analysis techniques [7] have been developed to automate the process to obtain some of the design equations. Recent work in equation-based approach involved on convex optimization techniques via a geometric programming formulation [8],[9]. Even though equation-based approach offers fast circuit evaluation, but the simplifications that is required to form the analytical model limit their accuracy.

Reference [10], ASTRX/OBLX [11], ANACONDA [12], MAELSTROM[13] and ASF [14] use simulation-based approach which is relevant to the ideas developed in this paper. This approach does not require much circuit knowledge, support wide range of circuit that can be synthesized and gives high accuracy result in the expense of computational cost. None of the techniques above include yield as one of the parameter for optimization.

However, there are some efforts that have been developed that include parameter variations in the analog circuit synthesis.[15],[16] use post-design yield analysis to change the cost function of the inner circuit optimization. While [17] incorporates mismatch parameter as the cost function, but this is done only for global variations and the mismatch is represented by a simplified model rather than simulation-based estimation.[18] had proposed a synthesis technique that include yield parameter during optimization which is based on symbolic equation model which we argue will limit the accuracy. HOLMES [19] uses a design centering method that push the design far from specification boundary as the method to optimize the yield. Here the yield is estimated by using analytical approach.

III. PROPOSED METHODOLOGY

This paper propose a technique that utilizes full simulation-based approach that incorporates yield as one of the performance parameter for optimization. The key concepts in the methodology are first to include yield as the cost function in the very beginning of the design and second to use full simulation-based optimization strategy. Monte Carlo simulation is used to simulate the yield performance.

There are two main components in the synthesis model : the Optimizer and the Evaluator. The Optimizer will provide all the necessary parameters of a circuit candidate. The circuit candidate is then evaluated by the evaluator in order to determine a fitness score. This fitness score will be passed back to the optimizer. An interfacing tool connects these two different components as illustrated in figure 1.

The reason to include yield as the cost function in the beginning of the design is to give a direction to the optimization process. With this approach, the searching algorithm (optimizer) will find the best solution that meets all these performance functions, including yield. This is a 100% simulation-based synthesis technique including direct-yield measurement. Below is the basic optimization formulation used where w_{f_i} is a scalar weight and $f_i(x)$ is the performance objective function.

$$O_{(x)} = \sum_{i=1}^k w_{f_i} f_i(x)$$

The idea to this formulation is that the maximum $O_{(x)}$ corresponds to the circuit that best matches the specification and at the same time provides the higher yield result. The weight attachment in the formulation will balance the competing objectives and gives high flexibility to maximize the objective function.

In this work, a global stochastic search algorithm, the Genetic Algorithm (GA) technique, was chosen to do the searching process. The GA was chosen rather than a gradient-style local optimization because of its empirical

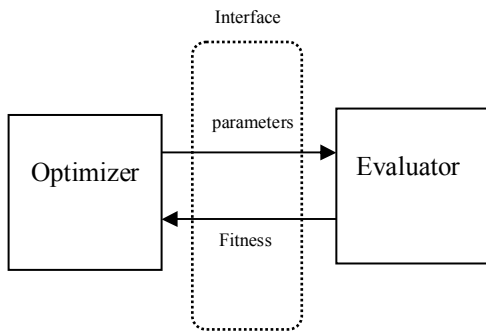


Figure 1 : Synthesis Model

robustness in nonlinear and non-convex objective functions. Global search optimization also has the potential to avoid many local minima that can degrade the searching efficiency.

The algorithm that has been used in this work is based on the C++ GALib Library developed by Matthew Wall [4]. It is based on simple GA algorithm that uses non-overlapping population described by Goldberg [20]. The algorithm starts with random initial generation of individuals based on the population size. In each generation, a new set of individuals will be created. The new generation will have offspring from previous generations using selection and recombination processes. This process continues until the total number of generation is reached. The “Elitism” technique was used in the algorithm meaning that the best individual from each generation is carried over to the new generation. Linear fitness scaling is used to avoid premature convergence. Without fitness scaling, there is a possibility a mediocre individuals would take over a significant proportion of the finite population in a single generation which is undesirable and can lead to premature convergence. A “roulette wheel” method was used for the selection scheme. This method picks an individual based on magnitude of fitness score relative to the rest of the population. The higher the score, the more likely the individual will be selected. The probability p of being chosen is equal to the fitness of the individual divided by the sum of the fitness of each individual in the population.

An interface unit connects the optimizer and evaluator. All the result calculation and data processing is done by this unit. Figure 2 shows the flow chart of the synthesis methodology.

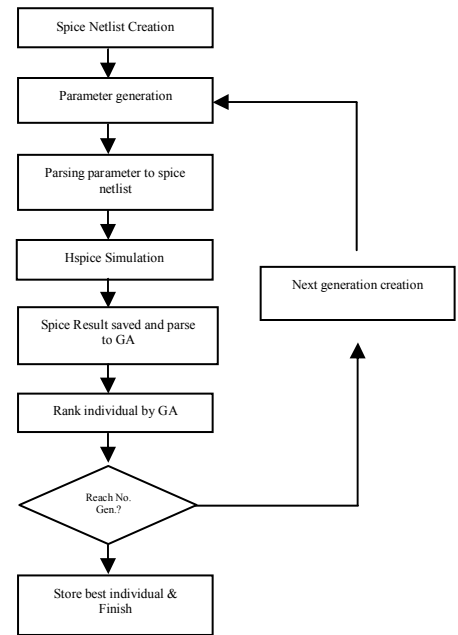


Figure 2: Synthesis Methodology

This methodology yields an adequate result, albeit somewhat slowly. The reason for this is because of the large number of circuit solutions that must be visited during the searching algorithm. Each visited solution requires more

than one circuit simulation to evaluate it. In addition to that, monte-carlo simulation consumes higher cpu time to be completed. This issue is one that is common across all optimization approaches.

II. SIMULATION RESULT

The ideas presented in this paper have been implemented on balanced-Operational Trans-conductance Amplifier (OTA) in a 0.35um AMS technology. Its circuit topology is shown in Fig. 3. Table 1 shows the design parameters of the simulation.

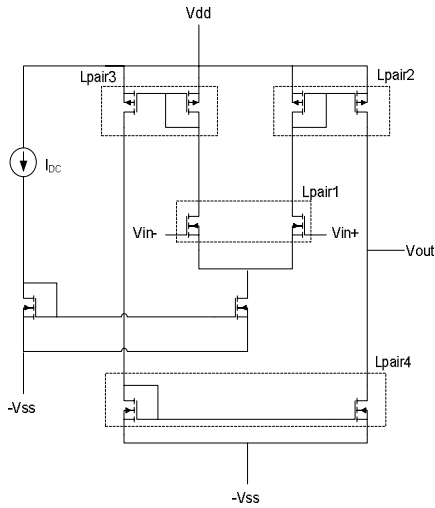


Figure 3: Balanced Operational Transconductance Amplifier

TABLE I
Design Parameters

Design Variables	Description
Designable Parameters with Statistical variations	Lpair 1, Lpair2, Lpair3 & Lpair 4
Non-Designable Parameters with Statistical variations	All transistor Widths
Transistor Length	0.35u ~ 2.0u
Transistor Widths	15u
Monte Carlo Simulation	100 samples, 1000 samples for verification
Statistical Variations	Gaussian Distribution, 3σ , 5%
GA Populations	100
GA Generations	30

The objective function which is based on a weighted summation of the performances were calculated and the result was used to determine the fitness score for each individual. The Genetic algorithm optimized the design by

maximizing this fitness score. Mean and maximum values of the objective function were plotted to show how the data track each other until converge to the solution point. The graphs (Figure 4) show how the optimization process reaches the final solution after 30 generations.

Table 2 shows the result of the optimization process. We have compared the proposed method with previous work that did not imply yield prediction. The table shows the performance, specifications and the final results between these two methods.

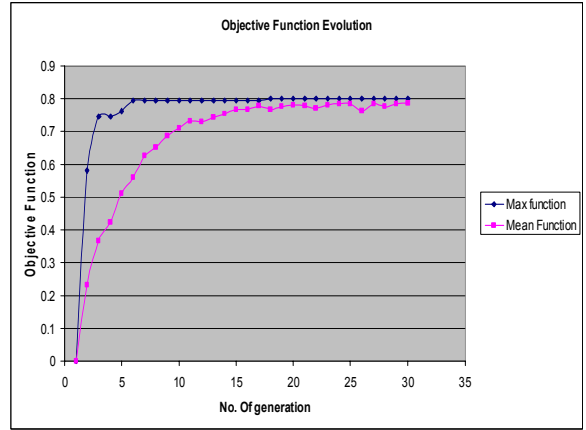


Figure 4: Max and Mean Plot

TABLE II
Optimization Results

Performance Function	Spec	Yield-Predictive Approach		Non-Predictive Approach	
		Result	Indiv. Yield	Result	Indiv. Yield
Gain	> 50dB	50.7 dB	100%	50.9 dB	100%
Volt. Offset	< 13mV	7.5 mV	89%	10.77 mV	72%
GBW	> 16 MHz	16.67 MHz	96%	17.08 MHz	100%
Phase Margin	> 67 deg	68 deg	94%	69.8 deg	100%
Slew Rate	> 15 V/us	16.1 V/us		17.7 V/us	
Power	Minimised	256.2 uW		255.7 uW	
Area	Minimised	209.3um ²		195.3um ²	
Overall Yield		89%		72%	

In yield-predictive approach, the yield parameter caused the optimizer to search for a solution that will give high overall yield. From the table, the yield is improved by 23%.

In Traditional method, the optimization will go towards achieving better performance trade-offs. From our

simulation, we found out that the best performance trade-off will not necessary gives the best overall yield. This is because some performances are too sensitive to process variations. However it might happened with the other approach to reach to an improved yield by running additional or separate optimisation. With our approach, the problem is tackled in one-shot. Figure 6 and 7 show the Monte Carlo simulation result for the voltage offset and open loop gain. The Monte Carlo simulation was done with 1000 samples. This simulation is to verify the yield result for each of the performance function.

V. CONCLUSIONS

We have presented a new strategy in analog circuit design that able to produce higher yield result. The contribution of the work is towards achieving higher yield design based on a yield-predictive approach. By integrating yield parameter in the beginning of the optimization process and with Monte Carlo technique that is used to estimate the yield, a relatively high accuracy result is achieved at the expense of increased computational cost. The balanced-OTA circuit was used to illustrate this new methodology and a comparison was done with the non-predictive approach. The result shows that a higher yield was achieved with the proposed method. The computational cost is one that can be overcome with a parallelization of the optimization process [15].

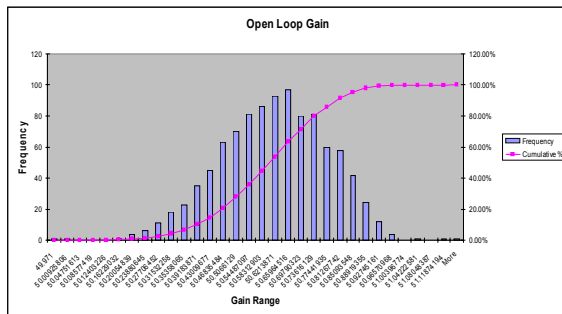


Figure 5 Monte Carlo Simulation for Open Loop Gain

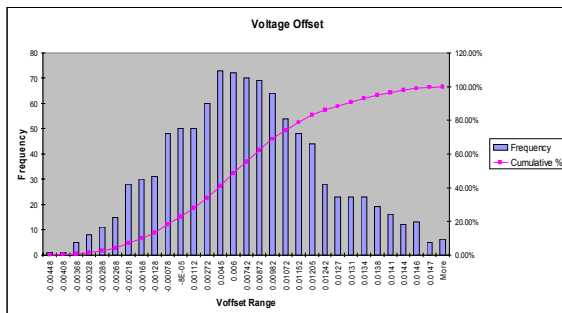


Figure 6 Monte Carlo Simulation for Voltage Offset

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