Variable polarisation compensator using artificial dielectrics for millimetre and sub-millimetre waves

T.D. Drysdale, H.M.H. Chong, R.J. Blaikie and D.R.S. Cumming

A variable polarisation compensator has been designed and demonstrated experimentally at 100GHz. The device uses two silicon plates with interlocking artificial dielectric surfaces to produce a birefringence that varies with the separation distance. The experimental results indicate a maximum differential phase-shift of 74°, and show good agreement with computer simulations.

Introduction: Variable polarisation compensators are well known in classical optics [1], but there are no analogues for sub-millimetre and millimetre wavelengths. However, artificial dielectric materials can have strong birefringence that may be used to provide low-cost, compact alternatives to devices such as box prisms, for instrumentation and communications applications [2 – 4]. In this Letter we report the first experimental demonstration of a micromachined silicon variable artificial dielectric retarder (VADR) that provides variable polarisation compensation at 100GHz.

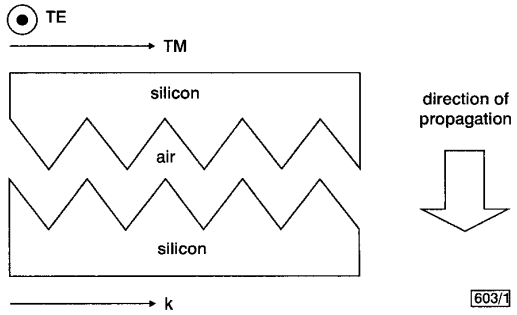

Fig. 1 *Cross-section of partially interlocked birefringent artificial dielectric gratings*

VADR (see Fig. 1) consists of two dielectric plates with interlocking sub-wavelength period V-groove gratings. There is no birefringence when the plates are fully interlocked, as the device is effectively a single, uniform dielectric slab. As the plates are separated, sub-wavelength air-dielectric gratings develop in the region of the V-grooves, creating an artificial dielectric with increasing birefringence. Once the plates are fully separated, the device acts as a Fabry-Perot resonant cavity with birefringent mirrors, and the composite birefringence oscillates as a function of separation distance [5].

Fabrication: VADR plates have been fabricated with bulk silicon micro-machining techniques. A 100mm-diameter (100)-orientation *p*-doped silicon wafer of resistivity 10–20Ω-cm was coated in 200nm of silicon nitride and cleaved into 20mm by 22mm samples. The silicon nitride on each sample was reactive ion etched (RIE) to form a linear grating of period 500μm and line width 40μm. Each plate was wet etched in 40% w/w potassium hydroxide (KOH) at 80°C for 280min. The KOH solution etches vertically at 1.2μm/min, but is prevented from etching laterally by the (111) etch stop planes that extend from mask edges at an angle of 54.7° to the surface [6]. These etch stop planes form the sloping sidewalls of the V-grooves. Two such gratings are interlocked to form complete VADR devices.

Experimental and simulation results: The complex transmission of a –15dBm 100GHz beam through VADR devices was measured using pyramidal transmitting and receiving horns connected to a W-band network analyser. The beam was normally incident and linearly polarised with the electric field perpendicular to **k** (TE) and parallel to **k** (TM), where **k** is the grating vector as shown in Fig. 1. Each plate was mounted over a fibreglass (FR-4) aperture. One holder was mounted on a fixed support, the other on a micrometre-driven translation stage that controlled plate separation. VADR was first mounted for a TE polarisation and S-parameters were recorded for a range of plate separations. The VADR was rotated 90° and the experiment repeated for the TM polarisation. The complex transmission coefficients are plotted as solid lines in Figs. 2*a–d*, with TE magnitude (Fig. 2*a*), TM magnitude (Fig. 2*b*), TE phase (Fig. 2*c*) and TM phase (Fig. 2*d*). The difference in the phase response between TE and TM is the birefringence property that is desired, and this is plotted in Fig. 3.

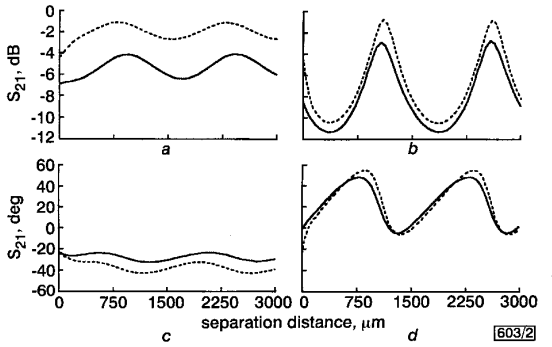

Fig. 2 *Complex transmission coefficients of VADR variable polarisation compensator for incident TE and TM linearly polarised radiation*

a TE, magnitude
b TM, magnitude
c TE, phase
d TM, phase
– – – – simulation
——— measurement

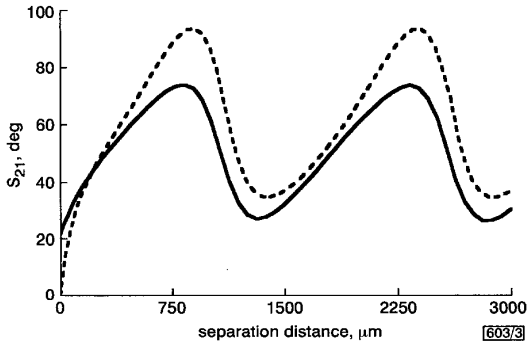

Fig. 3 *Phase difference between TE and TM polarisation*

– – – – simulation
——— measurement

The expected performance of the VADR devices has been simulated using a commercial rigorous coupled-wave analysis package [7]. The silicon substrate was modelled with complex permittivity $n' = 3.42 + 0.0384i$ for 200Ω-cm silicon [8]. A ten-layer staircase structure approximated the V-grooves. The complex transmission coefficients were extracted from field data, and are plotted as dashed lines in Fig. 2.

Discussion: The phase difference between the TE and TM polarisation, plotted in Fig. 3, gives a measure of the birefringence of the device as a function of the plate separation. The maximum phase difference of 74° was measured at a separation of 830μm. The first area of operation is in the interlock region, where separation distance is less than the groove depth. The phase difference changes linearly, from 22° to 34°, for separation distances 0–100μm, yielding a sensitivity of 120°/mm. A 0° shift was not observed owing to mechanical imperfections inhibiting full interlock. A second region of linear phase-shift lies between separations of 1000 to 1300μm, giving a relative phase difference of –36°, and sensitivity of –120°/mm. Over the entire operating range, the worst case insertion loss for TE and TM radiation is 7 and 11dB, respectively (Figs. 2*a*, *b*).

The simulations correctly predict the shape of the oscillation in the phase of the TM response, the relative magnitudes of the oscillations in both phase and magnitude responses, and the positions of the peaks and troughs of those oscillations (see Fig. 2). Quantitatively, the measured and simulated results for the TM polarisation agree within 2dB and 10° for magnitude and phase,

respectively, while the TE polarisation shows discrepancies of up to 4dB and 11°. The differences between the experimental and simulated data arise from the finite size of the test structure, resulting in field leakage. Similarly, despite the deep sub-wavelength grating period, there is some loss owing to diffraction.

Conclusions: A variable polarisation compensator using artificial dielectrics has been fabricated, tested and modelled at a frequency of 100GHz. Phase-shifts of up to 74° have been measured, in good agreement with simulations. The phase-shift can be greatly modified for small, easily controlled, changes in separation distance. Operation is wavelength specific, but the fabrication process scales easily. The VADR devices provide a compact, low-cost alternative to classical optical compensators at sub-millimetre and millimetre wavelengths.

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2.7V 50MHz IF sampling ΔΣ modulator with +37dBV IIP3

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The design and experimental results of a 2.7V 50MHz switched-capacitor DS modulator in 0.35μm BiCMOS process are presented. The circuit is targeted for the IF section of a radio receiver in a GSM cellular phone. It combines frequency downconversion with analogue to digital conversion by directly sampling an input signal from an IF of 50MHz. The measured peak signal-to-noise ratio for a 100kHz bandwidth is 81dB with a 53MHz blocking signal and the measured IIP3 for IF input is +36.9dBV.

Introduction: As the minimum feature sizes in integrated circuits shrink, it is becoming increasingly attractive to implement functions with digital rather than analogue circuitry. In radio receivers, the most straightforward way of eliminating analogue circuitry is to push the A/D conversion boundary higher in frequency. Unfortunately, this increases both the sampling frequency and dynamic range requirements of the ADC, leading to bottlenecks. Although wideband intermediate frequency (IF) A/D conversion may be feasible for base stations, it is typically too power consuming as a solution for cellular phones.

Alternatively, the IF A/D conversion can be realised by combining quadrature subsampling downconversion to DC with two lowpass ΔΣ modulators [1]. Passive switched-capacitor sampling consumes no extra power, which, combined with high resolution lowpass ΔΣ modulators, provides high dynamic range low-power IF A/D conversion.

The subsampling frequency downconversion is based on the (usually undesired) frequency aliasing effect. Any signal above the Nyquist frequency f_N will alias down below the Nyquist frequency when sampled. In principle, this allows an arbitrarily low local oscillator (LO) frequency (sampling clock) to be selected. However, decreasing the sampling frequency has the effect of moving the unwanted alias frequencies closer to the desired signal and making them more difficult to filter. Furthermore, the sampling aperture jitter induced noise power density is inversely proportional to the sampling frequency, which favours a high rather than low sampling frequency.

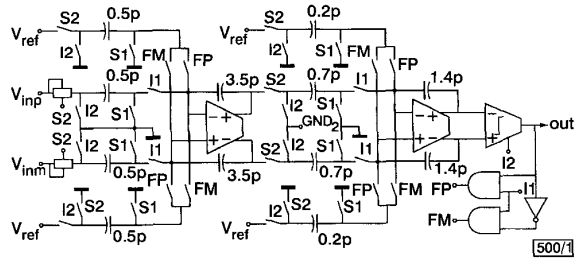

Fig. 1 *Circuit implementation of IF sampling ΔΣ modulator*

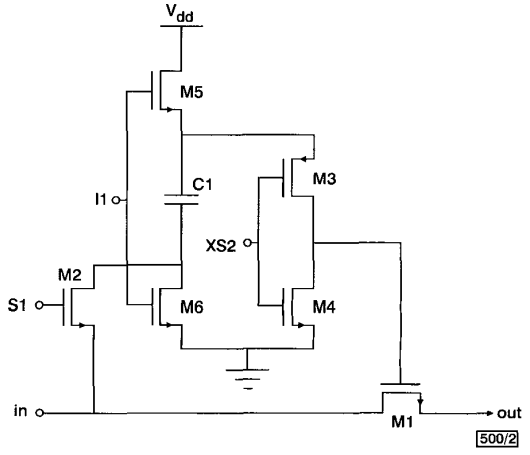

Fig. 2 *Input switch circuit arrangement*

Circuit design: To relax the anti-alias filtering and clock jitter requirements, the clock frequency of the implemented ΔΣ modulator was selected to equal the intermediate input frequency of 50MHz. The oversampling ratio for a 100kHz signal band then becomes 250, which makes a second-order loop filter more than sufficient with respect to noise shaping. The ΔΣ modulator was implemented as a fully differential SC circuit (Fig. 1). The reference voltage was selected as 1V and the kT/C noise of the input capacitors was designed to be 96dB below the signal over the bandwidth of 100kHz. The integration capacitors were scaled, on the basis of behavioural level simulations, to ensure that the opamps were not overloaded during the normal operation.

At a low supply voltage, the output swing capability of the opamps should be maximised by setting the common-mode level at mid-supply. However, this is not an optimal choice for the input differential pair. By selecting the common-mode level closer to the negative voltage supply, the tail current source of a PMOS differential pair is easier to implement. Also, the turn-on voltage of NMOS-transistor switches is increased, enabling the use of smaller switches and lower tracking distortion. This contradiction was solved by separating the input and output common-mode lev-