is attributed to the absence of gate depletion but of a comparable gate resistance. However, it is important to mention that for device architectures (FinFET, FD-SOI) that require a higher gate work function, the RF performance of deposited metal-gate devices will be reduced.

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Depletion-Isolation Effect in Vertical MOSFETs During the Transition From Partial to Fully Depleted Operation

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***Abstract*—A simulation study is made of floating-body effects (FBEs) in vertical MOSFETs due to depletion isolation as the pillar thickness is reduced from 200 to 10 nm. For pillar thicknesses between 200–60 nm, the output characteristics with and without impact ionization are identical at a low drain bias and then diverge at a high drain bias. The critical drain bias $V_{\rm dc}$ for which the increased drain–current is observed is found to decrease with a reduction in pillar thickness. This is explained by the onset of FBEs at progressively lower values of the drain bias due to the merging of the drain depletion regions at the bottom of the pillar (depletion isolation). For pillar thicknesses between 60–10 nm, the output characteristics show the opposite behavior, namely, the critical drain bias increases with a reduction in pillar thickness. This is explained by a reduction in the severity of the FBEs due to the drain debiasing effect caused by the elevated body potential. Both depletion isolation and gate–gate coupling contribute to the drain–current for pillar thicknesses between 100–40 nm.**

***Index Terms*—Depletion isolation, fully depleted (FD), partially depleted (PD), vertical MOSFETs (VMOS).**

I. INTRODUCTION

Aggressive scaling of CMOS devices has highlighted the requirement for fully depleted (FD) double-gate (DG) or surround-gate MOSFETs in order to control short channel effects at very-short channel lengths [1]–[3]. Technologically, these FD DG or surround-gate MOSFETs can be realized using DG silicon-on-insulator (SOI) [2]–[6], fin field-effect transistors (FinFETs) [7]–[9], or vertical MOSFETs (VMOS) [10]–[15]. Although a major advantage of DG SOI and FinFET technologies is the ease of device isolation, the body is left floating in most cases. Hence, these devices can suffer from floating-body effects (FBEs), whereby a weak avalanche in the drain causes hole injection to the body, which raises the potential there. The rise in body potential reduces the threshold voltage and forward biases the source–body junction, which can result in parasitic-bipolar-transistor (PBT) latch-up. Extensive work has been done on FBEs in both partially depleted (PD) and (FD) planar SOI transistors [16]–[19].

Fig. 1(a) and (b) shows schematic cross-sectional views of planar PD SOI and depletion-isolated VMOS devices, respectively. The FBEs are somewhat different for these two architectures and bulk MOSFET. The SOI device usually experiences a steepening of the subthreshold slope for a low drain voltage, leading to a latch effect due to the PBT at higher drain voltage. The SOI-PBT gain tends to be emitter efficiency limited and so can be controlled by source engineering [20]. In a body-contacted bulk MOSFET, FBEs occur due to a resistive voltage drop caused by the flow of generated holes to the body contact. However, for very-short channel devices, a direct PBT action also contributes as

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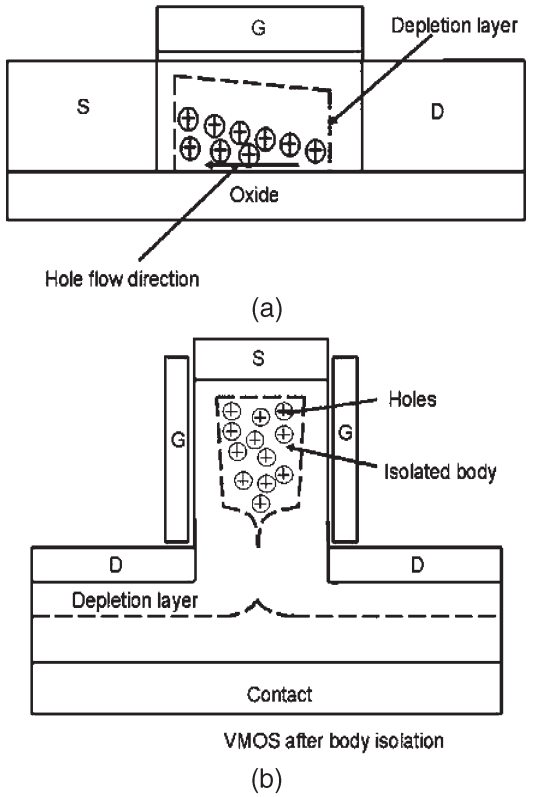

Fig. 1. Schematic cross-sectional views of (a) planar SOI and (b) VMOS device operated in the depletion-isolated mode.

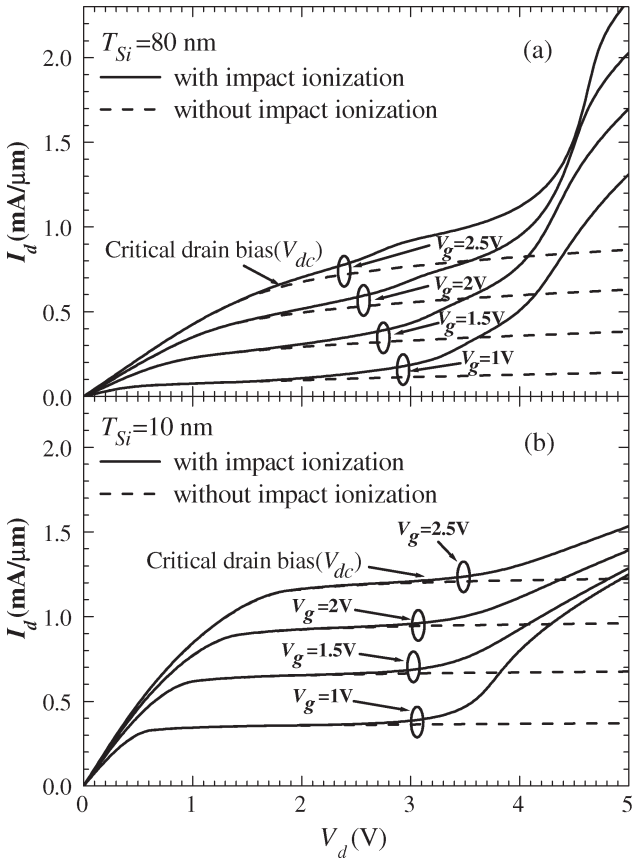

Fig. 2. Simulated output characteristics (I_d versus V_d) of VMOS transistors with body contact for pillar thicknesses of (a) 80 and (b) 10 nm. Solid lines represent simulations with impact ionization, and dashed lines represent simulations without impact ionization.

generated holes preferentially flow from the body to the source. In the case of the VMOS with the drain at the bottom [Fig. 1(b)], generated holes are separated by the geometry of the architecture. Holes are swept both upward and toward the source, causing the FBE, and also downward where they diffuse to the body contact.

Surround-gate VMOS have the advantage that it is easier to make a body contact, but FBEs are still observed at thin pillar thicknesses. Terauchi *et al.* [21] showed that FBEs occurred in VMOS due to the penetration of the depletion region of the bottom drain junction towards the center of the pillar and the eventual isolation of the pillar from the body contact. This depletion-isolation effect was measured in transistors with pillar widths varying from 1.2 μm to 400 nm. In a preliminary investigation, we noticed this effect even in very-thin pillar devices close to the FD regime [22]. In this letter, we simulate depletion isolation in surround-gate VMOS with pillar thicknesses between 200 and 10 nm and characterize the impact of the body contact during the transition from PD to FD operation. The relative contributions to the drain–current of the depletion isolation and gate–gate charge coupling are characterized during this transition.

II. Modeling Procedure

Analysis of the FBE was performed with the aid of numerical simulations using the Silvaco Atlas device simulator [23] implemented on a Sun workstation. A 100-nm-channel length vertical ion-implanted DG nMOSFET, as shown in Fig. 1(b), was simulated for different pillar thicknesses (T_{Si}). The gate oxide thickness was 2 nm, and a metal-gate electrode was chosen with a midgap work function of 4.5 eV [24]. The metal gate was chosen for optimal characteristics with no gate depletion problem [25] and low gate resistance. Fermi–Dirac statistics and bandgap narrowing were included, and the mobility was modeled using the Lombardi continuously variable transmission (CVT) model calibrated against a bulk silicon transistor [23]. In particular, the mobility degradation due to surface roughness arising from the dry etch of the vertical pillar was accounted for by adjusting the surface roughness factor to $\delta(\mathrm{elec}) = 2.91 \times 10^{13}$ V/S and $\delta(\mathrm{holes}) = 1.027 \times 10^{13}$ V/S in the model. Impact ionization was modeled by the Selberherr law for the generation rate, and the model parameters have already been optimized for submicrometer bulk silicon transistors [26]. The Shockley–Read–Hall (SRH) electron and hole lifetimes τ_n and τ_p were modeled as concentration dependent. The simulations were performed at room temperature, and the silicon parameter values were taken from [23] and [26]. The model was calibrated against experimental VMOS characteristics [13] for a substrate-doping concentration of $10^{18}/\mathrm{cm}^3$ and source/drain doping densities taken from SIMS profiles [13]. A good fit for the transfer characteristic at a low drain voltage was obtained.

III. Results

Fig. 2 shows the output characteristics of simulated VMOS transistors with body contact for pillar thicknesses of 80 and 10 nm and for the source-on-top mode of operation. Results are shown for simulations with and without impact ionization. For thick pillars, ideal characteristics were obtained with no evidence of breakdown up to a drain bias of 5 V. For the 80-nm pillar thickness in Fig. 2(a), the simulation with impact ionization exhibits strong FBEs; whereas the simulation without impact ionization shows ideal characteristics up to a drain bias of 5 V. The characteristics with and without impact ionization coincide up to a drain bias of about 1.8 V and diverge at higher biases. This result is indicative of depletion isolation at this

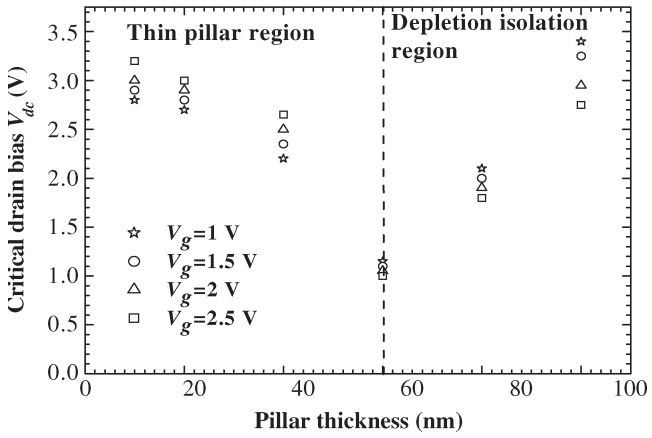

Fig. 3. Extracted values of the critical drain bias $V_{\rm dc}$ (voltage at which the current with impact ionization diverges from the current without impact ionization) as a function of pillar thickness for several values of gate voltage.

pillar thickness. For the 10-nm pillar in Fig. 2(b), the characteristic with impact ionization shows FBEs but the breakdown is less severe than that in Fig. 2(a). The characteristics with and without impact ionization coincide up to drain biases between 2.7–3.1 V (dependent on gate bias) and diverge at higher biases. Since the 10-nm pillar is FD at all drain biases, this result cannot be explained by depletion isolation.

To investigate these FBEs in more detail, we now investigate the effect of the pillar thickness on the critical drain bias $(V_{\rm dc})$ for which the excess drain–current is observed. Fig. 3 shows the simulated values of $V_{\rm dc}$ as a function of pillar thickness for several values of gate voltage. The $V_{\rm dc}$ was calculated by comparing the output characteristics of body-contacted devices with and without impact ionization and by identifying the voltage at which the characteristics diverged. For pillar thicknesses $\geq$ 60 nm, $V_{\rm dc}$ reduces with decreasing pillar thickness; whereas for pillar thicknesses $<$ 60 nm, $V_{\rm dc}$ increases with decreasing pillar thickness. A similar transition at a pillar thickness of 60 nm can also be seen in the dependence of $V_{\rm dc}$ on the gate voltage V_g. For pillar thicknesses $\geq$ 60 nm, $V_{\rm dc}$ decreases with increasing V_g; whereas for pillar thicknesses $<$ 60 nm, $V_{\rm dc}$ increases with increasing V_g.

IV. Discussion

We now consider the physical explanation for the transition in the critical drain bias $(V_{\rm dc})$ at a pillar thickness of 60 nm. Simulations show that for a pillar thickness of 80 nm, the pillar is not isolated at a low drain bias but becomes isolated at higher values of drain bias by the merging of the drain depletion regions at the bottom of the pillar. The output characteristics with impact ionization in Fig. 2(a) reflect the existence of depletion isolation, as can be seen from the presence of breakdown and the divergence from the characteristics without impact ionization above a drain bias of 1.8 V. Definitely, the depletion edge is not abrupt but extends over 2–3 Debye lengths on each side of the pillar so that, for a body doping of $10^{18}/{\rm cm}^3$, there is a 10–15-nm transition region for depletion-isolation consideration.

For a pillar thicknesses of 60 nm and less, simulations show that the pillar is isolated at all drain biases; hence, the pillar is FD. In this regime, the drain debiasing effect due to the elevated body potential reduces the severity of the breakdown as can be seen in Fig. 2(b) for a 10-nm pillar thickness. The moderate breakdown observed at this pillar thickness is well known from studies of planar SOI devices [17]–[19].

The transition in the $V_{\rm dc}$ seen in Fig. 3 at a pillar thickness of 60 nm can be explained from the competing mechanisms of depletion isolation at progressively lower drain biases and the decreasing severity of the FBEs as the pillar thickness is decreased. Reducing the pillar thickness at a fixed gate bias (or increasing the gate voltage at a given pillar thickness) brings the depletion regions at the bottom of the pillar closer together. Therefore, as the pillar thickness is reduced from 120 to 60 nm, $V_{\rm dc}$ decreases with a decreasing pillar thickness (and also decreases with an increasing gate voltage), because depletion isolation occurs at progressively lower values of drain bias. In contrast, for pillar thicknesses $<$ 60 nm, the pillar is FD and isolated even at zero drain bias. Scaling of the pillar thickness from 60 to 10 nm results in a transition to a more strongly depleted regime of operation; therefore, $V_{\rm dc}$ increases with a decreasing pillar thickness (and also increases with an increasing gate voltage).

To investigate the nature of the hole flow with a decreasing pillar thickness, Fig. 4 shows the potential in the middle of the pillar for pillar thicknesses of 80 and 60 nm at $V_g = 1$ V and $V_d = 5$ V. At this bias voltage, the pillar is isolated in both devices. For the pillar thickness of 80 nm, the potential barrier is small, with a value of 0.052 eV (i.e., 2 kT) and will not fully block the diffusion of holes into the substrate. In contrast, for a pillar thickness of 60 nm, the potential barrier is much bigger (0.52 eV); hence, the hole flow from pillar to substrate is more effectively blocked. This indicates that the body contact is still partially effective even when the pillar is isolated but becomes more ineffective with a decreasing pillar thickness due to the gradual strengthening of the drain depletion region at the pillar bottom, which would also affect the relative contributions to the drain–current of depletion isolation and gate–gate charge coupling at different pillar thicknesses.

To consider the relative contributions of depletion isolation and gate–gate charge coupling in thin pillar VMOS, we have simulated devices at various pillar thicknesses with and without impact ionization. A relative drain–current was then calculated by dividing the drain–current of the device at a given pillar thickness by the drain–current of a 200-nm pillar device with a deactivated impact ionization. The curve without impact ionization allows us to see the rise in the drain–current due to gate–gate charge coupling alone, whereas the curve with impact ionization takes into account both depletion isolation and gate–gate charge coupling. Fig. 5 shows the relative drain–current as a function of pillar thickness for VMOS devices with and without impact ionization and for $V_g = 2$ V and $V_d = 3.5$ V. The bulk MOSFET behavior is apparent for pillar thicknesses $\geq$ 140 nm. The rise in drain–current due to gate–gate charge coupling starts at a pillar thickness of 100 nm, whereas the effect of depletion isolation starts at a pillar thickness of 120 nm. For pillar thicknesses between 120–80 nm, we see that the rise in the relative drain–current is mainly due to depletion isolation. For a pillar thickness 60 nm, the two mechanisms contribute similar amounts to the rise in current; for pillar thicknesses $\leq$ 40 nm, the rise in current is mainly due to the gate–gate charge coupling. For pillar thicknesses between 100–60 nm, the device is actually in the transition from PD to FD due to Debye length considerations; hence, the gate–gate charge coupling, i.e., the amount of body depletion, is not strong. Scaling the pillar thickness in this regime results in a small current rise due to weak gate–gate charge coupling, but the isolation imposed by the bottom drain depletion region also increases as shown in Fig. 4. Therefore, in this regime, we see an increase in the depletion-isolation effect with a reduction in pillar thickness, as the device is driven to a stronger depletion-isolation regime. Effective suppression of depletion isolation occurs when the device is driven into a strongly FD regime below 40 nm.

To further validate the presence of gate–gate charge coupling, we have investigated the subthreshold slopes of the devices at different pillar thicknesses. For a drain bias of 0.1 V, subthreshold slopes were found to be 79, 77, and 61 mV/dec for 200-, 80-, and 10-nm pillar

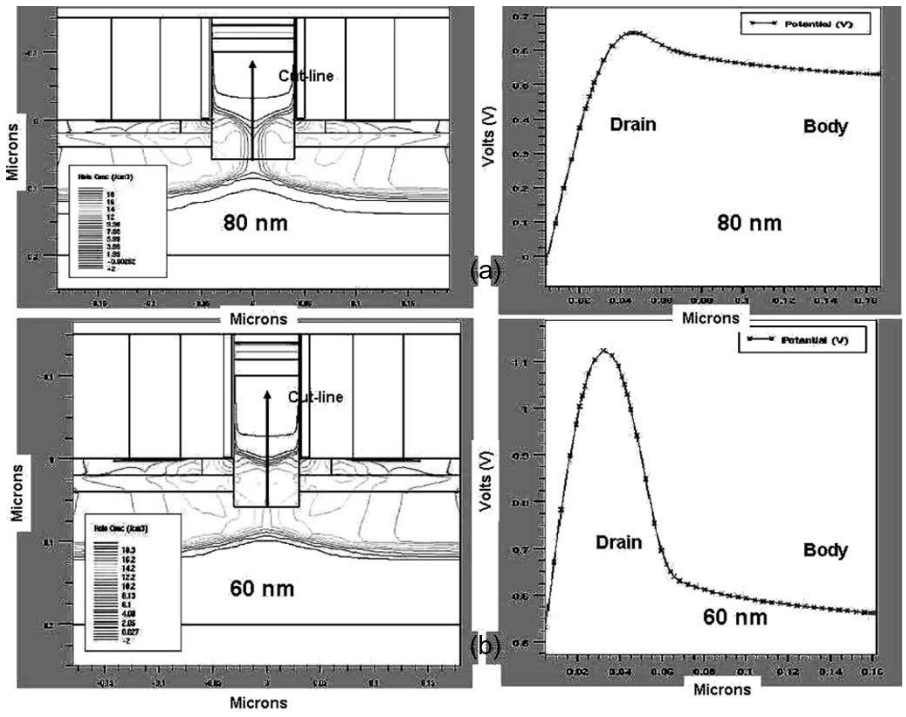

Fig. 4. Hole-concentration contour plot and drain body-potential barrier of a VMOS device in the middle of the pillar, for pillar thicknesses of (a) 80 and (b) 60 nm. The gate voltage is 1 V, and the drain voltage is 5 V. The cutline of the device structure for which the potential profile is drawn is shown on the contour plot.

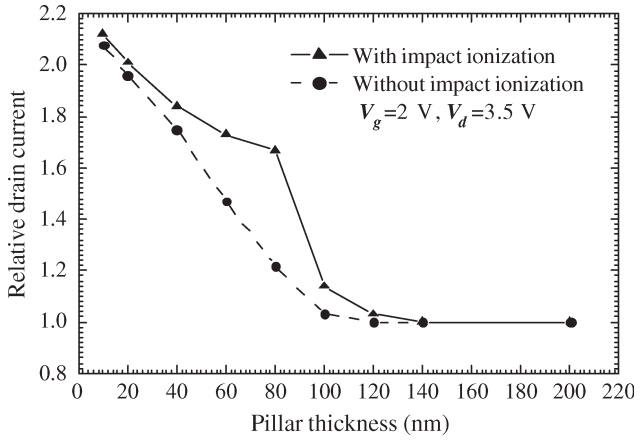

Fig. 5. Relative drain–current of body-contacted VMOS devices as a function of pillar thickness with and without impact ionization for $V_g = 2$ V and $V_d = 3.5$ V. The relative drain–current was calculated by dividing the drain–current of the device at a given pillar thickness by the drain–current of a 200-nm pillar device with deactivated impact ionization.

devices, respectively. This decreasing value of subthreshold slope with a decreasing pillar thickness confirms an increase in gate–gate charge coupling with a decreasing pillar thickness.

V. Conclusion

We have studied in some detail, the depletion-isolation effect and the role of the body contact in VMOS with pillar thicknesses in the range 200–10 nm, covering the transition from PD to FD behavior. Simulated output characteristics with and without impact ionization are identical at low drain biases but diverge at high drain bias. The critical drain bias $(V_{\rm dc})$, at which the current diverges, decreases with a decreasing pillar thickness. This trend continues down to a pillar thickness of 60 nm. However, for thinner pillars, the opposite trend is observed. The decrease in $V_{\rm dc}$ with a decreasing pillar thickness is due to depletion isolation, which occurs at progressively lower drain biases as the pillar thickness is reduced. The increase in $V_{\rm dc}$ with a pillar thickness below 60 nm is explained by a reduction in the severity of the FBEs as is observed in planar SOI devices at thin pillar thicknesses. Depletion isolation has a significant effect on the drain–current down to a pillar thickness of 40 nm. In summary, our results indicate that pillar-thickness scaling is advantageous for VMOS if the device operates in the strongly FD regime (i.e., less than 40 nm for a body doping of $10^{18}/{\rm cm}^3$). However, in the PD regime and even in the transition from PD to FD operation, pillar-thickness scaling results in increased FBEs due to the stronger isolation imposed by the drain depletion region at the pillar bottom.

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