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Accurate modeling of gate capacitance in deep submicron MOSFETs with high-*K* gate-dielectrics

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Abstract

Gate capacitance of metal-oxide-semiconductor devices with ultra-thin high-*K* gate-dielectric materials is calculated taking into account the penetration of wave functions into the gate-dielectric. When penetration effects are neglected, the gate capacitance is independent of the dielectric material for a given equivalent oxide thickness (EOT). Our self-consistent numerical results show that in the presence of wave function penetration, even for the same EOT, gate capacitance depends on the gate-dielectric material. Calculated gate capacitance is higher for materials with lower conduction band offsets with silicon. We have investigated the effects of substrate doping density on the relative error in gate capacitance due to neglecting wave function penetration. It is found that the error decreases with increasing doping density. We also show that accurate calculation of the gate capacitance including wave function penetration is not critically dependent on the value of the electron effective mass in the gate-dielectric region.

Keywords: MOS structures; Gate capacitance modeling; Quantum effects; Wave function penetration; High-*K* gate-dielectric

1. Introduction

Current scaling of metal-oxide-semiconductor (MOS) field-effect transistor (FET) feature sizes has led to the fabrication of devices in deep sub-100 nm regime with gate-oxide thickness equal to or less than 1 nm. In such devices, an exponential increase of direct tunneling (DT) gate current is observed, raising concern about chip standby power consumption. Another problem is the reliability of using SiO_2 as a gate-dielectric material below 1 nm thickness. To overcome these problems, it is required that gate-oxide be replaced by suitable high-*K* gate-dielectric materials [1]. Due to higher physical thickness of the high-*K* dielectric layers for a given equivalent oxide thickness (EOT), the DT current is reduced and further scaling down becomes possible. In this context, EOT is defined as the scaled (to SiO_2) physical width of the high-*K* dielectric layer.

Extensive amount of work has been done in recent years exploring quantum mechanical (QM) effects on DT gate leakage current. QM effects also influence gate capacitance. The quantization of inversion charges leads to a degradation of the gate capacitance. However, modeling of gate capacitance in deep sub-100 nm devices is somewhat complicated. QM effects are usually incorporated by self-consistent solution of coupled Schrödinger's and Poisson's equations. Closed boundary conditions are typically used for the solution of Schrödinger's equation which assume that the wave function is zero at silicon–gate-oxide interface [2]. When this boundary condition is used, effects of wave function penetration into the gate-dielectric are neglected. Consequently, for a given EOT, the calculated gate capacitance becomes independent of the gate-dielectric material.

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Since the potential barrier height for inversion carriers at silicon–gate-dielectric interface is finite and is of the order of 1 eV, some penetration of the wave function into the gate-dielectric occurs. When this penetration is taken into account by using an open boundary condition at silicon–gate-dielectric interface, the wave function is shifted towards the interface by a few tenth of a nanometer, but its shape essentially remains unchanged [3,4]. A number of studies have been reported recently on the modeling of gate capacitance with open boundary conditions in the inversion region as well as in the accumulation region [5–8]. It has been shown that the gate capacitance is under-estimated if calculated with closed boundary conditions and this effect is stronger at higher surface electric field. Most of the works on gate capacitance modeling with open boundary conditions reported so far have considered SiO_2 as the gate-dielectric material. Although different high-K dielectric materials are characterized by different values of conduction (valence) band offsets with silicon, $\Delta E_C(\Delta E_V)$, dielectric constant, K, and electron effective mass in dielectric region, m_{ox}, combined effects of these parameters through wave function penetration on gate capacitance calculation are yet to be investigated.

In this paper, we perform a quantitative analysis of the gate capacitance of MOS structures with high-K gate-dielectric materials to study the effects of different dielectric materials on the modeling of the gate capacitance. Open boundary conditions, incorporating wave function penetration, are used to solve Schrödinger's equation. MOS electrostatics is calculated by self-consistent solution of coupled Schrödinger's and Poisson's equations including the effects of wave function penetration on the electrostatic potential inside the self-consistent loop.

2. Theory

We use the logarithmic derivative technique of the retarded Green's function, G^R, to solve the one-dimensional (1D) Schrödinger's equation in the direction normal to the silicon–gate-dielectric interface (z direction) with open boundary conditions. The theory is described in detail in [3,9]. G^R satisfies the equation,

$$\left[E+\frac{\hbar^2}{2m_z^*}\frac{\partial^2}{\partial z^2}-qV(z)+\mathrm{i}\varepsilon\right]G^R(z,z';E)=\delta(z-z'), \quad (1)$$

where E is the eigenenergy, $V(z)$ is the electrostatic potential, m_z^* is the quantization effective mass in the direction normal to the interface and ε is an infinitesimally small positive energy. The logarithmic derivative of the retarded Green's function, G^R, is defined as

$$Z(z,z';E)=\frac{2\hbar}{\mathrm{i}m_z^*}\left[\frac{\partial G^R(z,z';E)}{\partial z}\Big/G^R(z,z';E)\right]. \quad (2)$$

Owing to the property of G^R, $Z(z,z';E)$ has a discontinuity at $z=z'$, and one needs two boundary conditions to determine $Z(z,z';E)$. Our boundary conditions are based on the realistic assumption that the electric field is zero deep inside the gate-electrode as well as deep inside bulk silicon. This assumption implies that the wave function is exponentially decreasing in bulk silicon and is a plane wave in the gate-electrode. From the properties of the Green's function, it can be shown that $Z(z,z';E)$ does not depend on z' as long as $z>z'$ ($z<z'$) [9]:

$$Z(z,z';E)=Z_{iR}(z;E) \quad \text{for all } z'<z, \quad (3a)$$

$$Z(z,z';E)=Z_{iL}(z;E) \quad \text{for all } z'>z. \quad (3b)$$

Z_{iR} and Z_{iL} can be calculated easily using a method analogous to the impedance transformation technique of microwave transmission lines [9].

When open boundary conditions are used, the Hamiltonian for the MOS structure becomes non-Hermitian and the eigenenergies become complex. The real part gives the energy of the nth quasi-bound state, E_n, and the imaginary part is related to the lifetime of the corresponding state. In order to avoid determining complex eigenenergies of a non-Hermitian operator, we evaluate the local 1D density-of-states (DOS), $N(z;E)$ at some point within the quantum well using the following relationship.

$$N(z;E)=-\frac{1}{\pi}\mathrm{Im}\left[G^R(z,z;E)\right]. \quad (4)$$

Relating the diagonal part of G^R to its logarithmic derivative, Eq. (4) is re-written as [9],

$$N(z;E)=\frac{4}{\pi\hbar}\mathrm{Im}\left[\frac{\mathrm{i}}{Z_{iR}(z;E)-Z_{iL}(z;E)}\right]. \quad (5)$$

$N(z;E)$ broadens in energy in the presence of tunneling. We now calculate E_n by locating the peaks of $N(z;E)$. Once E_n are calculated, corresponding wave functions, φ_n, including penetration into the gate-dielectric, are evaluated in a straight-forward manner using the following equation [9]:

$$|\varphi_n(z)|^2=\frac{4\varepsilon}{\hbar}\mathrm{Im}\left[\frac{\mathrm{i}}{Z_{iR}(z;E_n)-Z_{iL}(z;E_n)}\right]. \quad (6)$$

1D Poisson's equation is solved for the combined metal-oxide-semiconductor regions. Thus, the effect of wave function penetration on the electrostatic potential is also taken into account within the self-consistent loop. This effect has been found to be non-trivial in strong inversion [6]. After the convergence of the self-consistent

loop, the gate capacitance, C_g, is determined from the fundamental relationship

$$C_g = \frac{q\partial(N_{inv} + N_{dep})}{\partial V_g}. \quad (7)$$

Here, V_g is the gate voltage, N_{inv} and N_{dep} are the number of charges per unit area in the inversion layer and in the depletion layer, respectively. Expressions for N_{inv} and N_{dep} are given in Ref. [2].

3. Results and discussion

The results of our self-consistent calculations for nMOS devices fabricated on (1 0 0) silicon are presented in this section. Calculations are performed at room temperature and values for different parameters for (1 0 0) silicon are taken from Ref. [2]. Aluminum, with a work function equal to 4.1 eV, has been used as the gate-electrode material. Conduction band offsets with silicon, ΔE_C, and dielectric constant, K, of the high-K gate-dielectric materials are taken from Ref. [10] and are presented in Table 1.

Effective mass of electrons in gate-dielectric region has been a topic of controversy. Using a microscopic model, Städele et al. have shown that the representation of electrons in SiO_2 by a constant effective mass is not strictly valid [11]. However, the use of such models makes routine device simulation computationally prohibitive. On the other hand, a constant effective mass for electrons in SiO_2 gate region has been used to model experimental DT current with reasonable success [12,13]. Although a few recent studies have focused on estimating m_{ox} in SiO_2 and a few other high-K dielectric materials [14], in the absence of any detailed knowledge about the band structures of the dielectric materials, m_{ox} is still widely treated as a fitting parameter. For this reason, we too represent electrons in gate-dielectric region by a constant m_{ox}. We choose $m_{ox} = 0.5m_0$ in SiO_2 [12,13] as well as in other high-K gate-dielectrics. The effects of the choice of m_{ox} on gate capacitance will be discussed later in this section.

Fig. 1 shows the average distance of inversion carriers, z_{avg}, from silicon–gate-dielectric interface as a function of gate voltage V_g for four different dielectric materials. In these calculations, EOT = 1 nm, and the silicon substrate doping density $N_A = 10^{18}$ cm^{-3}. It is observed that z_{avg} is independent of gate-dielectric material when calculated with closed boundary conditions (neglecting wave function penetration). But when wave function penetration is considered, z_{avg} decreases with decreasing ΔE_C (Table 1). As the conduction band offset decreases, wave functions penetrate more into the gate dielectric. As a result, the carrier distribution is shifted towards the interface and z_{avg} is decreased. It should be mentioned that the dielectric constant K directly affects the calculation results only through Poisson's equation. It has no influence on the carrier quantization other than the fact that ΔE_C tends to decrease with increasing K. Since we explicitly take ΔE_C into account, K has only a minor effect on our calculations.

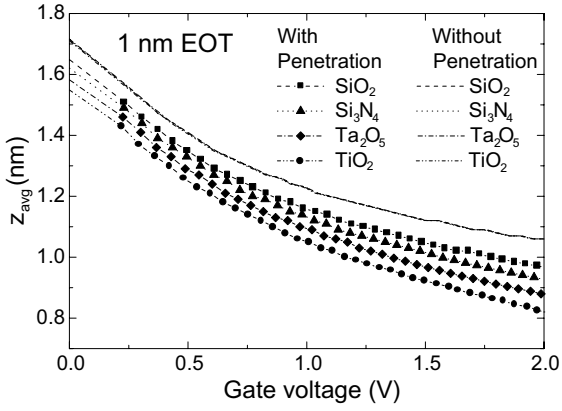

Fig. 1. Average distance of inversion carriers z_{avg} as a function of gate voltage for four different gate-dielectric materials of 1 nm EOT calculated both considering and without considering wave function penetration.

Table 1
Dielectric constants and conduction band offsets at silicon–dielectric interface for different dielectric materials used in our calculation (from Ref. [10])

Material	Dielectric constant (K)	ΔE_C (eV) to silicon
SiO_2	3.9	3.2
Si_3N_4	7	2
Ta_2O_5	26	1.3
TiO_2	80	1.2

Next, we study the inversion layer capacitance defined by the relationship $C_{inv} = q\partial N_{inv}/\partial\phi_S$, where ϕ_S is the silicon surface potential. C_{inv} calculated as a function of N_{inv} is plotted in Fig. 2. These results are independent of the dielectric layer thickness [6]. Again, we observe that the results do not depend on dielectric materials if closed boundary conditions are used for the solution of Schrödinger's equation. In the presence of wave function penetration, devices with higher-K dielectric materials exhibit higher C_{inv} due to a smaller value of ΔE_C. Since C_{inv} is inversely proportional to z_{avg}, especially in strong inversion, a lower z_{avg} associated with a lower ΔE_C results in a higher C_{inv}.

Gate capacitance C_g for all four dielectric materials with EOT = 1 nm is shown in Fig. 3. Again, $N_A = 10^{18}$ cm^{-3} in these calculations. For a given EOT, C_g does not depend on gate-dielectric material when wave function

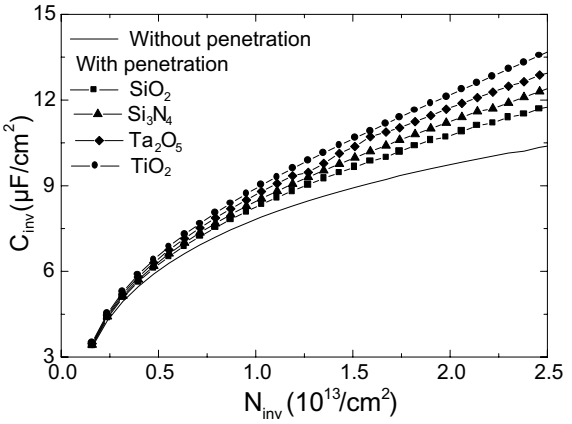

Fig. 2. Inversion layer capacitance C_{inv} versus inversion carrier density N_{inv} for four different gate-dielectric materials calculated both considering and without considering wave function penetration.

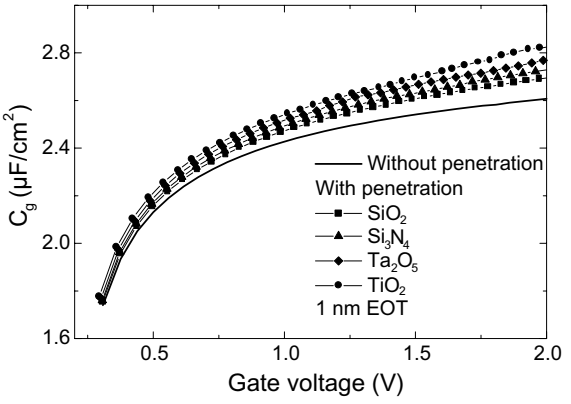

Fig. 3. Gate capacitance C_g as a function of gate voltage for four different gate-dielectric materials of 1 nm EOT calculated both considering and without considering wave function penetration.

penetration is neglected. As expected [5], inclusion of penetration effects increases C_g, particularly in strong inversion. An important observation in Fig. 3 is that for the same EOT, the increase in C_g due to wave function penetration is different for different gate-dielectric materials. C_g is found to increase with decreasing ΔE_C. Fig. 3 can be explained in terms of Fig. 2. It is known that in strong inversion, the gate capacitance can be expressed as a series combination of the dielectric layer capacitance $C_{di} = \varepsilon_0 K/t_{di}$ and C_{inv}. Here, t_{di} is the physical thickness of the dielectric layer. For a given EOT, C_{di} is the same for all the materials. As already discussed, in devices with higher-K dielectric materials (lower ΔE_C), C_{inv} is higher. Therefore, for a fixed gate voltage, C_g becomes greater as ΔE_C decreases or the dielectric constant increases. The relative error in calculating C_g due to neglecting wave function penetration is plotted in Fig. 4. The error is the minimum for SiO_2 (lowest K, highest ΔE_C) and the maximum for TiO_2 (highest K, lowest ΔE_C). Moreover, the error increases with increasing inversion (increasing gate voltage), and the rate of increase of the error is higher for materials with lower ΔE_C. According to the International Technology Roadmap for Semiconductors (ITRS), by 2006, the gate capacitance should be modeled within 3% error [1]. Our results show that for accurate modeling of gate capacitance in MOS structures with high-K gate-dielectric materials, wave function penetration into the gate-dielectric should be taken into consideration. Since SiO_2-high-K dielectric stack structures are also becoming technologically important, we point out that in such devices, the gate capacitance will be determined primarily by the dielectric material adjacent to the silicon surface as the penetration of the wave function is significant only within a few tenths of a nanometer from the silicon surface.

We also investigate the effects of substrate doping density (N_A) on the error in gate capacitance calculation. This is important since the doping density increases with device scaling. It is observed in Fig. 5 that for a given dielectric material with a fixed EOT, at a given gate voltage, the error decreases with increasing substrate doping. This is due to the reason that a higher N_A causes a larger fraction of the gate voltage to drop across the depletion region. Consequently, the inversion carrier density is lower, resulting in a reduced error in the gate capacitance. We have also checked that the error increases with a reduction in EOT. Thus, with device scaling, as the substrate doping density is increased and EOT decreased, the two competing effects make the error in the gate capacitance weakly dependent on device scaling.

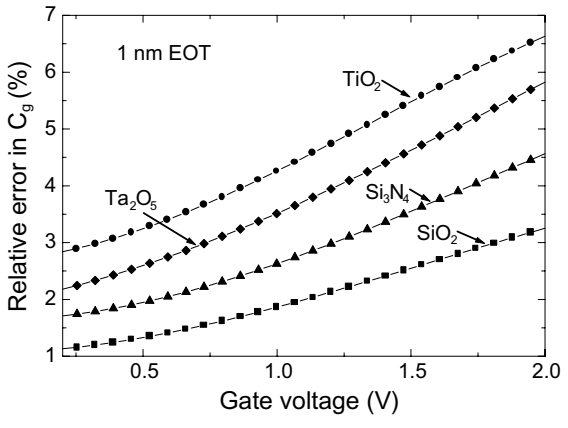

Fig. 4. Relative error in gate capacitance due to the neglect of wave function penetration for different gate-dielectric materials of 1 nm EOT. Here, substrate doping density $N_A = 10^{18}$ cm^{-3}.

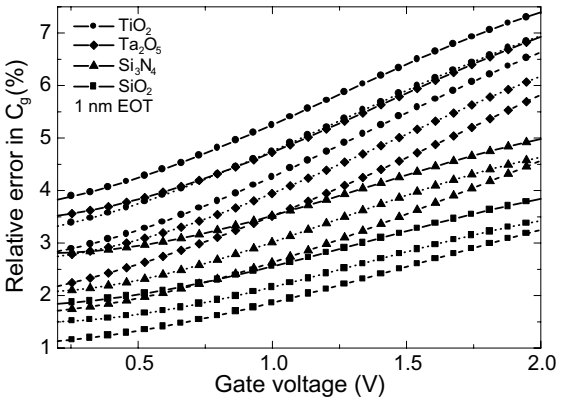

Fig. 5. Relative error in gate capacitance due to the neglect of wave function penetration for four different gate-dielectric materials of 1 nm EOT calculated for three different substrate doping density N_A. For a given material, solid line represents $N_A = 10^{17}$ cm^{-3}, dotted line represents $N_A = 5 \times 10^{17}$ cm^{-3}, and dashed line represents $N_A = 10^{18}$ cm^{-3}, respectively.

The effect of m_{ox} on modeling of C_g with open boundary conditions is considered next. While it is known that the direct tunneling gate current is rather sensitive to a change in m_{ox} [14,15], its influence on the gate capacitance is yet to be studied in detail. In Fig. 6(a), C_g is calculated for SiO_2 gate-dielectric with $m_{ox} = 0.4m_0$ and $0.6m_0$. Most reported values of m_{ox} for SiO_2 fall within this range. Fig. 6(b) shows C_g for Ta_2O_5 with $m_{ox} = 0.25m_0$ and $0.35m_0$. Lower values of m_{ox} for Ta_2O_5 are chosen because of the observation that m_{ox} tends to decrease with a decrease in ΔE_C [14]. It may be mentioned that the slight ripple in C_g in Fig. 6(b) is a consequence of numerical differentiation and has no physical significance. We find that m_{ox} has only a minor effect on C_g even when wave function penetration effects are included. For both SiO_2 and Ta_2O_5, at a gate voltage of 2 V, the difference in C_g for the two values of m_{ox} is around 0.65%. This value is much smaller than the error caused by neglecting wave function penetration (Figs. 4 and 5). Therefore, it may be argued that m_{ox} is not a critical parameter in accurate calculation of the gate capacitance in MOS structures with ultra-thin gate-dielectrics.

Finally we present the effects of wave function penetration on gate capacitance from the view point of the effective thickness of the gate-dielectric. While EOT is conventionally defined as the equivalent thickness of SiO_2 that would produce the same C–V curves (neglecting wave function penetration) as that obtained from the high-K gate-dielectric (EOT $= t_{di}K_{SiO_2}/K$), capacitive effective thickness (CET), also known as the electrical dielectric thickness, is simply defined by the relationship CET $= \varepsilon_0 K_{SiO_2}/C_g$ [16]. In case of ultra-thin gate-dielectrics, EOT and CET are related according to Eq. (8).

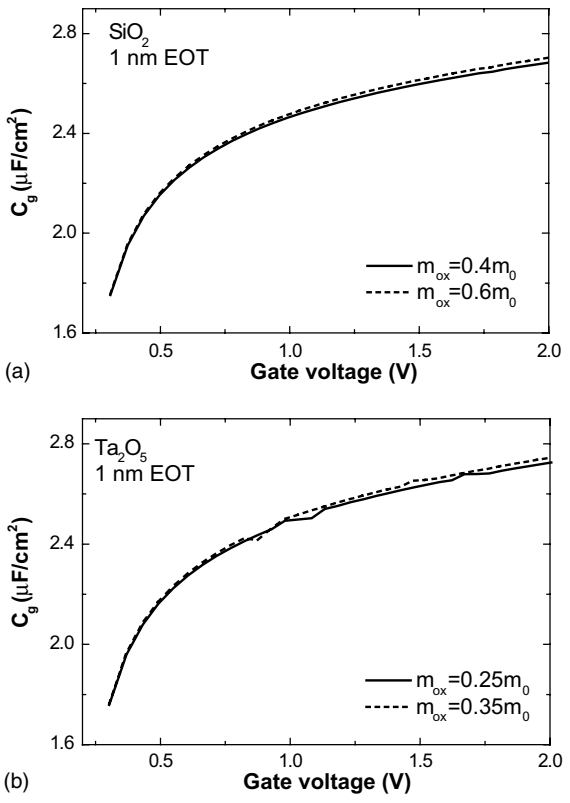

Fig. 6. Gate capacitance C_g as a function of gate voltage calculated considering wave function penetration for different values of m_{ox}: (a) SiO_2 gate dielectric and (b) Ta_2O_5.

$$\mathrm{CET} = \mathrm{EOT} + (K_{SiO_2}/K_{Si})z_{avg}. \tag{8}$$

The error in CET due to neglecting wave function penetration effects can be represented as

$$\Delta\mathrm{CET} = (K_{SiO_2}/K_{Si})(z_{avg(cbc)} - z_{avg(obc)}). \tag{9}$$

Here, cbc (obc) stands for closed boundary condition (open boundary condition). For an EOT of 1 nm, at a gate voltage of 2 V, ΔCET is 0.32 Å for SiO_2 and 0.81 Å for TiO_2. Corresponding errors in C_g are 3.1% for SiO_2 and 6.6% for TiO_2, respectively. Thus the dependence of the wave function penetration effects on the gate-dielectric material is also clearly presented in terms of the error in CET.

4. Conclusions

We have calculated the gate capacitance of MOS structures with ultra-thin high-K gate-dielectric materials. An open boundary condition, allowing for wave function penetration into the gate-dielectric, is used at silicon–gate-dielectric interface to solve Schrödinger's equation. In the absence of wave function penetration,

for a given EOT, gate capacitance is independent of gate-dielectric material. However, when penetration effects are taken into account, it is found that even for the same EOT, gate capacitance is different for different dielectric materials. The calculated gate capacitance is higher for materials with lower conduction band offsets with silicon. We have studied the dependence of the error in gate capacitance calculation on substrate doping density. The relative error is found to decrease with increasing substrate doping density. Consequently, this error depends only weakly on device scaling. Our results show that unlike the direct tunneling gate current, calculation of the gate capacitance with open boundary condition is not sensitive to small changes of the electron effective mass in the gate-dielectric region. The dependence of the error in gate capacitance on the gate-dielectric material can also be expressed in terms of the error in the capacitive effective thickness.

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