Observation of Quantum Level Spectrum for Silicon Double Single-Electron Transistors

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We observed the spectrum of quantum levels on series-connected double single-electron transistors (DSETs). The DSETs, composed of double quantum dots are formed with lateral confinements on the silicon-on-insulator substrate. To characterize DSETs, the electrical measurements were carried out at the base temperature of 22 mK by using a dilution refrigerator. The estimated energy spacing from the measurement characteristics agreed with the values from the geometrically defined quantum dots size. These results exhibit the significant potential of DSETs as a readout device for two charge quantum bits (qubits). © 2008 The Japan Society of Applied Physics

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Semiconductor-based double quantum dots (DQDs) have been extensively studied as attractive candidates for charge quantum bits (qubits) due to their scalabilities. Initially, DQDs were studied by means of surface gates depletion on the two-dimensional electron gas of GaAs:AlGaAs hetero-structures below the temperature of 1 K.[1–5] In contrast, silicon-based DQDs are more promising candidates for charge qubits because of the absence of piezoelectric electron-phonon coupling, acoustic mismatch of the amorphous oxide surrounding silicon dots, and the effect of phonon localization.[5–7] However, compared with GaAs-based DQDs, the number of research on silicon double DQDs below 1 K is quite small regardless of their unique properties and their compatibilities with the existing large-scale integration silicon process. In a silicon-based substrate, resonant tunneling has recently been observed by using accidentally fabricated parasitic dots in a thin silicon-on-insulator (SOI) layer (10 nm).[6] In contrast, in lateral confinement-induced quantum dots, capacitance values are controlled by the device geometrical structures.[8] The device shown here defines quantum dots by lateral confinements that act as tunnel barriers through SOI technology.

For the readout of extremely small charge polarizations of DQDs, single-electron transistors (SETs) have been extensively used[9,10] because of their ultra-high charge sensitivity. The theoretical limit of charge sensitivity for a SET is about $1 \times 10^{-6}\,\mathrm{eHz}^{-1/2}$.[11] Recently, a research on series-connected double dots transistor as a readout for adjacent double charge qubits has been proposed and actively studied by our research group.[12] This readout is called double SETs (DSETs) because of the series connection of two SETs. In this work, we report the observation of spectroscopy for quantum levels on the silicon DSETs.

The DSETs were fabricated using a SOI substrate with an initial SOI thickness of 100 nm and buried-oxide (BOX) thickness of 200 nm. Phosphorous at the concentration of $10^{19}\,\mathrm{cm}^{-3}$ was doped into the SOI layer. The initial SOI layer thickness was reduced to 40 nm by repeated thermal oxidation and wet etching. After the thinning process, negative resist RD-2000N was coated for electron-beam (EB) direct writing because RD-2000N shows good sensitivity to EB exposure and offers good etching resistance and simple handling.[13] The device pattern on the resist was transferred to the SOI layer by using electron cyclotron resonance reactive ion etching (ECR-RIE), followed by thermal oxidation at 1000 °C for 20 min to reduce the dots size and to passivate the surface states. A scanning electron micrograph image of DSETs is shown in Fig. 1(a). The bright and the dark regions indicate the SOI and the BOX layers, respectively. Double quantum dots with two SET gates (G1, G2) and five qubit control gates (G3–G7) are shown in Fig. 1(a). In the reported results of this paper, qubit control gates are always grounded during the measurement. In the future, double qubits composed of DQDs will be integrated at the positions marked by dotted circles.[10,12] The equivalent circuit of the DSETs is shown in Fig. 1(b). The final oxidation led to the resulting Si dots core diameter of approximately 55 nm.

The electrical measurements were carried out at the base temperature of 22 mK. The effective electron temperature was estimated to be about 0.2 K. Voltages to the terminals were applied by using HP 3245A and Keithley Quad Voltage Source 213. The SET current was measured by using the Toyo Corp. current amplifier with its output connected to the HP 34401A digital multi-meter. At an ultra low temperature, the voltage drop in Si leads should be considered. We extracted the effective source–drain voltage V_{DSeff}, defined as the voltage drop between the leftmost and the rightmost tunnel barriers, by measurements at different temperatures. Figure 2(a) shows the contour plot of I_{D} as a function of V_{G1} and V_{G2} at $V_{\mathrm{DSeff}} = -7.5$ mV. In the gray scale plot, the absolute value of the current decreases from the dark region to the white region. In this measurement result, in every point, two triangle conductive regions coexist, indicating the sequential tunneling transport through the DQDs.[2] From this measurement characteristic, the total capacitances of the left dot (Dot 1) and the right dot (Dot 2) and the interdot capacitance were extracted to be $C_{\mathrm{C1}} = 16$ aF and $C_{\mathrm{C2}} = 12$ aF, and $C_{\mathrm{C}m} = 3.1$ aF, respectively. The corresponding charging energies are $E_{\mathrm{C1}} = 10$ meV, $E_{\mathrm{C2}} = 14$ meV, and interdot coupling energy $E_{\mathrm{C}m} = 2.7$ meV. Additionally, gate capacitances $C_{\mathrm{G1D1}} = 0.75$ aF, $C_{\mathrm{G1D2}} = 0.50$ aF, $C_{\mathrm{G2D2}} = 0.80$ aF, and $C_{\mathrm{G2D1}} = 0.70$ aF were also extracted from the measured double dot stability characteristics. At 4.2 K, similar stability characteristics were observed and the extracted gate capacitances of the dots

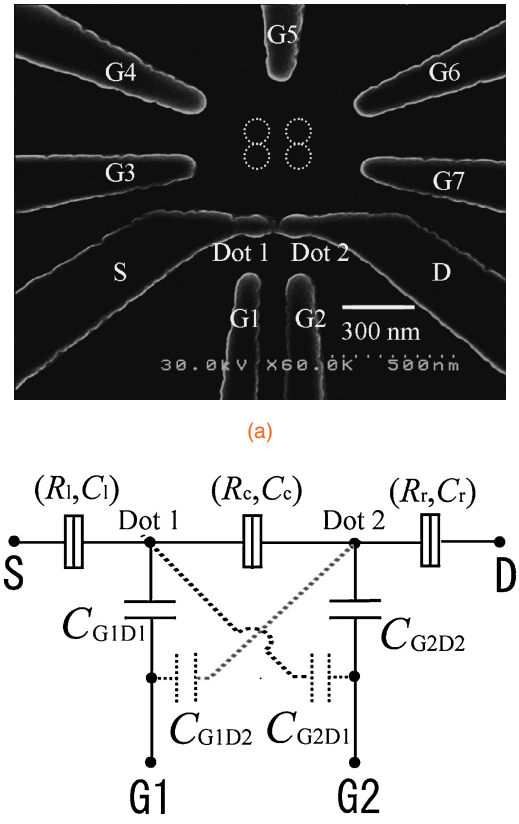

Fig. 1. (a) Scanning electron micrograph image of DSETs with qubit control gates. The bright and dark regions indicate the SOI and the BOX layers, respectively. The fabricated device is structured with double quantum dots (DQDs), two SET gates (G1, G2) and five qubit control gates (G3–G7). In the future, double qubits composed of DQDs will be integrated at the positions marked by dotted circles. (b) The equivalent circuit for DSETs.

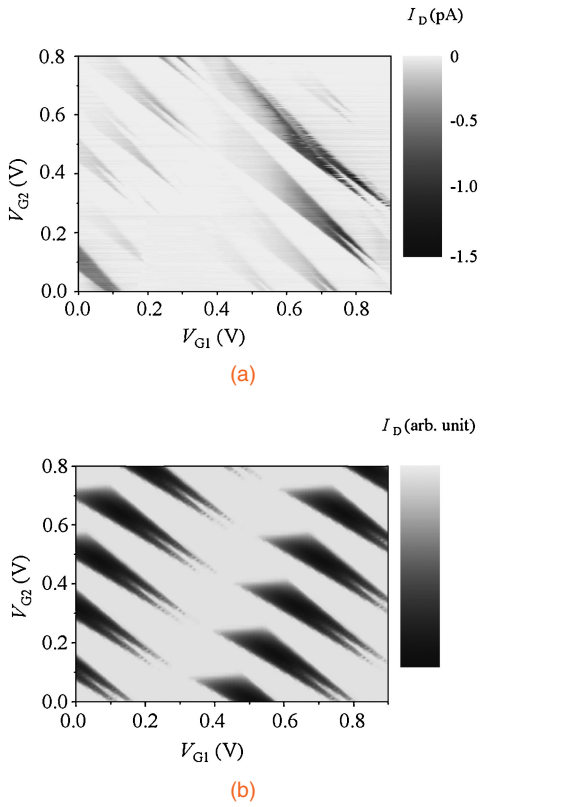

Fig. 2. (a) Stability diagram of the DSETs by sweeping V_{G1} for different values of V_{G2} at $V_{DSeff} = -7.5$ mV. Qubit control gates (G3–G5) are grounded during the measurement. (b) The result of the equivalent circuit simulation. A triangle-shaped characteristic is clearly reproduced.

were almost the same as those extracted at 22 mK. With this consistency in the device characteristics at different temperatures, the origin of the dots is attributed to the well-defined geometrical lateral confinements. But in the case of dopant-induced dots, the dots are formed by random dopant potential fluctuations with respect to the Fermi energy.[14] Characteristics of the DSETs composed of dopant-induced dots are considered to change complicatedly with the temperature, because the configurations and the number of dopant-induced dots change with the temperature. Furthermore, the gate capacitances are considered to be different among the fabricated DSETs if the dots are formed by random dopant potential fluctuations. The extracted gate capacitances of the device in this paper are in the same order with the geometrically defined double dots reported in ref. 12. So, the possibility of the dopant-induced dots is ruled out. Figure 2(b) shows the result of the equivalent circuit simulation of the DSETs. The simulation revealed triangle-shaped characteristics that were apparently reproduced by implementing the above mentioned values into the equivalent circuit model as shown in Fig. 1(b).

A fine sweep across the charge triple points is shown in Fig. 3(a). In this measurement, the primary sweep was done with the gate G1. This gray scale plot displays the values of differential conductance $(\partial I_{DS}/\partial V_{G1})$ as a function of V_{G1} and V_{G2} for $V_{DSeff} = -8.5$ mV. Fine structures in the triangle-shaped region are clearly visible. Figure 3(b) blows up the square region marked in Fig. 3(a) and I_D–V_{G1} characteristic along the dotted line in the $(\partial I_{DS}/\partial V_{G1})$ plot. The current peaks in I_D–V_{G1} plot are located between high differential conductive peaks in the triangle-shaped region in the $(\partial I_{DS}/\partial V_{G1})$ plot. These current peaks and $(\partial I_{DS}/\partial V_{G1})$ peaks are caused by the resonant tunneling through DQDs. These $(\partial I_{DS}/\partial V_{G1})$ peaks can be used to detect charge polarizations for double qubits integrated in the future. In reality, it is complicated and difficult to take into the consideration every transition between all states of the Nth electron and all states of the $(N+1)$th electron in each dot. Given that all the level intervals are the same for two dots, the energy spacing was estimated to be 0.5 meV. This value is in good agreement with the value 0.6 meV estimated from the dots diameter of 55 nm. Interestingly, a number of fine structures were successfully observed. This result is ascribed to resonant tunneling from more than one of the excited states or the ground state in the right dot to more than one of the excited states or the ground state in the left dot. This indicates the electron tunneling from the right dot to the left dot before relaxations to the lower levels. Current in the off-resonant conditions are attributed to resonant tunneling broadening and inelastic tunneling. Inelastic tunneling I_{inel} is given by $I_{inel} = e[\Gamma_L^{-1} + \Gamma_i^{-1} + \Gamma_R^{-1}]^{-1}$ where Γ_L (Γ_R) is tunnel couplings between the left dot (right dot) and the source (drain) electrode, and Γ_i is the inelastic rate from a

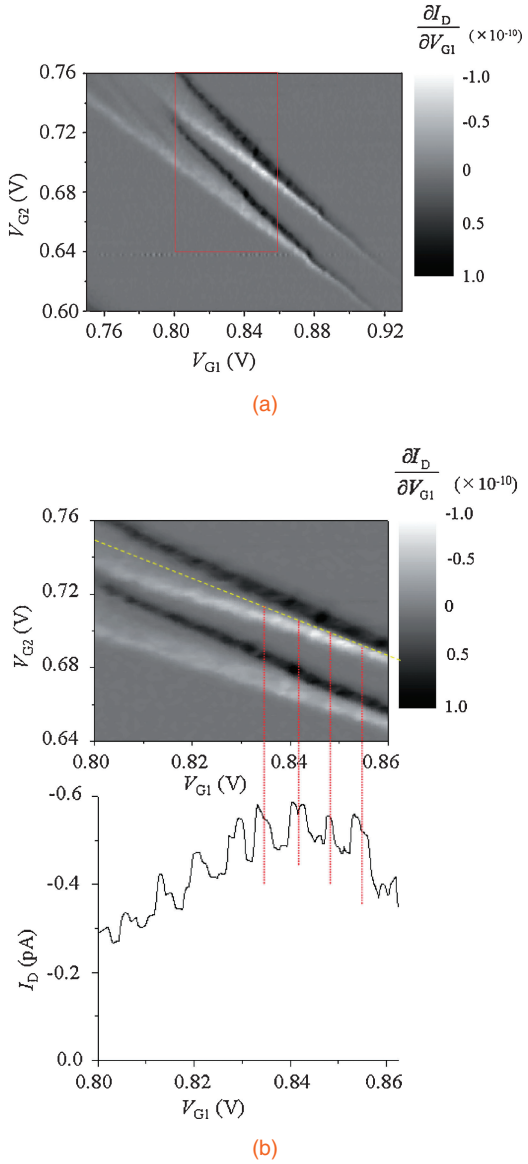

Fig. 3. (a) A fine sweep across the charge triple points. In this measurement, primary sweep was done with the gate G1. This gray scale plot displays the values of differential conductance ($\partial I_{DS}/\partial V_{G1}$) as a function of V_{G1} and V_{G2} for $V_{DSeff} = -8.5$ mV. Fine structures in the triangle-shaped region are clearly visible. (b) The square region marked in Fig. 3(a) and I_D–V_{G1} characteristic along the dotted line in the ($\partial I_{DS}/\partial V_{G1}$) plot are shown. The current peaks in I_D–V_{G1} plot are located between differential conductive peaks in the triangle-shaped region in ($\partial I_{DS}/\partial V_{G1}$) plot. These current peaks are caused by the resonant tunneling through DQDs.

state in the right dot to a state in the left dot.[4] When Γ_i is much smaller than Γ_L and Γ_R, then $I_{inel} = e\Gamma_i$. Γ_i is 3.0×10^6 Hz at most, estimated from the off-resonance current $I_{off} \approx 0.48$ pA at $V_{G1} = 0.835$ V in I_D–V_{G1} plot. Because of the present device geometry [Fig. 1(a)], the interdot tunneling rate at resonance Γ_{LR} is considered to be smaller than Γ_L and Γ_R, and is dominant so that $\Gamma_{LR} \approx 3.6 \times 10^6$ Hz can be estimated from the resonant current 0.58 pA at $V_{G1} = 0.843$ V in the I_D–V_{G1} plot. This inelastic tunneling rate is quite small compared with GaAs DQDs.[3] Finally, the peak-to-valley current ratio is evaluated to be 1.2. Although the resonant tunneling is still not clear on the present stage, this characteristic can be explicit via the reduction of dot size and electron temperature by improving measurement setup. Through this kind of effort, bonding states and anti-bonding states in qubits could also be detected by measuring the current through quantum states in the DSETs.

In conclusion, we observed the spectrum of quantum levels for the silicon DSETs composed of DQDs. The quantum dots were not attributed to the random fluctuation of the dopants potential, but to the well-defined lateral confinement even at the dilution base temperature of 22 mK. The estimated level spacing in the quantum dots from the measured characteristics was also in agreement with the value from the quantum dot size. The estimated inelastic tunneling rate between the dots was less than 3.0×10^6 Hz, which is quite small compared with GaAs-based DQDs. The observed differential conductance peaks can be used to detect double qubits integrated in the future.

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