

Control of Electrostatic Coupling Observed for Silicon Double Quantum Dot Structures

Gento YAMAHATA*, Yoshishige TSUCHIYA, Shunri ODA, Zahid A. K. DURRANI¹, and Hiroshi MIZUTA^{2,3}

*Quantum Nanoelectronics Research Center, Tokyo Institute of Technology and SORST JST,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan*

¹*Department of Electrical and Electronic Engineering, Imperial College London, South Kensington Campus, London SW7 2AZ, U.K.*

²*School of Electronics and Computer Science, University of Southampton, Highfield, Southampton SO17 1BJ, U.K.*

³*Department of Physical Electronics, Tokyo Institute of Technology and SORST JST,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan*

(Received January 4, 2008; accepted February 17, 2008; published online June 13, 2008)

We study the electrostatic coupling in the silicon double quantum dot (DQD) structure as a key building block for a charge-based quantum computer and a quantum cellular automaton (QCA). We realize the three interdot coupling regimes of the DQD structure only by optimizing the DQD design and the thermal oxidation condition. We then demonstrate that the electrostatic coupling between DQDs can be modulated by tuning the negative voltage of the side gate electrode. Note that the interdot coupling was largely modulated with a small decrease in the gate voltage from 0 to -100 mV because our structure initially has the DQD geometry. Furthermore, the device fabrication is compatible with the conventional silicon complementary metal–oxide–semiconductor (CMOS) process. This structure is suitable for the future integration of CMOS devices. In addition, we show the derivation of the DQDs' capacitances, including the gate cross capacitances, as a function of the spacing between the two adjacent charge triple points. By using these capacitances, the electron transport properties of the DQD structure are simulated, and the modulation of the electrostatic coupling is successfully simulated as the change of the total capacitance in DQDs. [DOI: [10.1143/JJAP.47.4820](https://doi.org/10.1143/JJAP.47.4820)]

KEYWORDS: silicon double quantum dot, quantum information device, electrostatic coupling

1. Introduction

In recent years, semiconductor double quantum dot (DQD) structures have attracted much attention as a building block for the solid-state quantum computer.¹⁾ While there are several studies^{2–5)} focusing on the qubit, which is the basic component for the quantum computer, one of the candidates is the electronic states in DQDs. The coherent manipulation of the electronic states in DQDs has been studied by using several materials such as the GaAs/AlGaAs heterostructure⁶⁾ and the silicon isolated DQD.⁷⁾ Silicon qubits have a great advantage in realizing the future quantum circuit because of their compatibility with the conventional silicon complementary metal–oxide–semiconductor (CMOS) process. However, the decoherence time of the silicon qubit of about 200 ns is not enough for the $\sim 10^4$ operations that are required for the fault-tolerant quantum computation.⁷⁾ To address this problem, it is necessary to improve the decoherence time itself or decrease the gate operation time. One possibility for realizing these improvements is to increase the interdot coupling,⁷⁾ which leads to wide two-level splitting. The modulation of the interdot coupling results in several advantages for the qubit operation. First, when the two-level splitting increases, the coherent oscillation that is realized in the electron state qubits becomes fast, with the frequency corresponding to the angular frequency of Larmor Precession given by $\Omega = \sqrt{\varepsilon^2 + \Delta^2}/\hbar$, where ε is the energy difference between the uncoupled charge state, and Δ is the two-level splitting.⁶⁾ Consequently, the qubit operation becomes fast. Second, the wide two-level splitting reduces the influence of the thermal fluctuation, which may result in the improvement of decoherence time. Finally, if the energy of the small phonon density of states corresponds to the electron energy difference of two levels, it is possible to reduce the electron–

phonon interaction, thereby leading to the reduction of decoherence time. Moreover, the DQD structure is the basic component for the QCA.⁸⁾ It is very important to control the coupling between two dots because electron switching in the double dot is necessary. There are two methods to increase interdot coupling. One is by scaling down the size of the DQD. When the DQDs' size becomes smaller, the superposition of the electron wave function between each dot becomes stronger. This leads to the wider two-level splitting. Another is the tuning of the interdot coupling by using the gate voltage.

In this paper, we discuss the modulation of the coupling between the two dots. Actually, we demonstrate the tuning of the electrostatic coupling within the orthodox theory through the electronic property of the silicon DQD structures connected to the source and the drain lead. If the dot size is sufficiently small in the extent of the electron wave function, the modulation of the electrostatic coupling must lead the change in the two-level splitting. We can observe the three regimes of the interdot coupling (weak, intermediate, and strong coupling) in the DQD structure only by optimizing the DQD design and the thermal oxidation condition. Furthermore, we modulate the electrostatic coupling in the DQD structures by using the negative voltage of the side gate electrode. While it has been reported that the coupling of the DQD structure in group IV materials (Si or Ge) was controlled with the top-gate,^{9,10)} we realize the control of the coupling with the low voltage of the side gate electrode because our structure initially has the DQD geometry. In addition, because our DQD device has a more compact structure than that of the top-gate devices, it is suitable for integration of the DQD structures with not only the charge sensor⁷⁾ but also the conventional silicon CMOS devices. Finally, we introduce an equivalent circuit model for the DQD structures in order to simulate the electron transport theoretically. It has a good agreement with our experimental data.

*E-mail address: ygent@neo.pe.titech.ac.jp

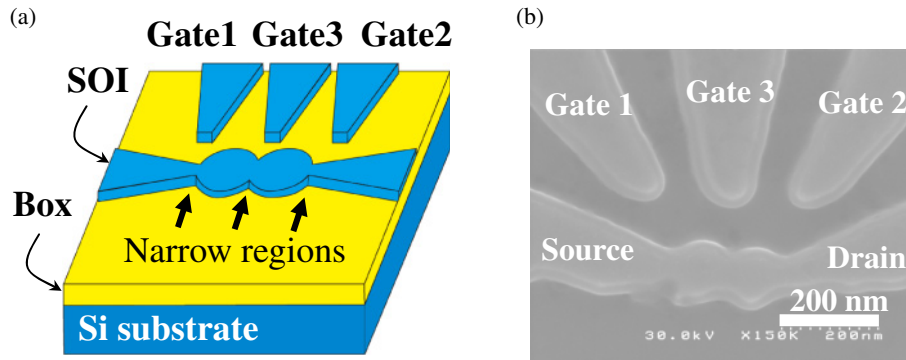


Fig. 1. (Color online) (a) The schematic image of the DQD structure. Three side gate electrodes are aligned on one side. (b) SEM image of the DQD structure with the 40 min oxidation time at 1000 °C after EBL.

2. Device Structure and Fabrication Process

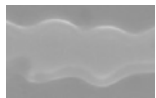
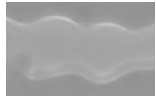
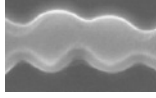
Figure 1(a) shows the schematic illustration of the Si DQD structure. The DQD structure is connected to the source and drain leads because we would like to observe the change of electrostatic coupling as the tunneling current through the DQD structure. At the narrow regions in the DQD structure, which are indicated by using the black arrows shown in Fig. 1(a), the bottom of the conduction band is expected to rise due to the quantum-mechanical size effect. These potential barriers are presumably the origin of forming three tunnel junctions of the DQD structure. We carefully designed multiple side gate electrodes with sharp tips located in the vicinity of the tunnel junction between DQDs. The role of Gate 1 and Gate 2 is to change the electrochemical potential of the left dot and the right dot, respectively, whereas the role of Gate 3 is the modulation of electrostatic coupling, although Gate 3 changes the electrochemical potential of the DQD structure.

The DQD structures were defined on the heavily doped silicon-on-insulator (SOI) of about 40 nm and the buried oxide (BOX) of 200 nm in thickness. First, a 40-nm-thick SOI film, whose thickness was reduced via thermal oxidation at 1100 °C for 75 min, was doped heavily by ion implantation (n-type, phosphorous, doping concentration $\sim 1 \times 10^{20} \text{ cm}^{-3}$). The DQD structures were then patterned using high-resolution electron beam lithography (EBL) with the ZEP520A positive resist. The electron cyclotron resonance reactive ion etching was used to transfer the resist pattern onto the SOI layer, and CF_4 was used as etching gas. Thermal oxidation was then done for 30 or 40 min at 1000 °C in order to passivate the surface states and reduce the dot size. Finally, Ohmic contacts were formed by evaporating about 300-nm-thick Al. Figure 1(b) shows the scanning electron micrograph (SEM) image of the DQD structure, which has an oxidation time of 40 min at 1000 °C after EBL.

3. Experimental Results and Discussion

All measurements of the DQD structures were performed using the Hewlett-Packard 4156A parameter analyzer at the temperature of 4.2 K in liquid helium. We characterized the three DQD devices (DQD A, DQD B, and DQD C) which have different fabrication conditions as shown in Table I. DQD A, B, and C have 30, 40, and 40 min oxidation time after EBL, respectively. With the increase of the oxidation

Table I. Fabrication condition and the coupling at the interdot region of the three different DQD devices.

	Oxidation time after EBL (min)	Constriction	Coupling
DQD A	30	Weak	 Weak
DQD B	40	Weak	 Intermediate
DQD C	40	Strong	 Strong

time, the bottom of the conduction band in the interdot region becomes high due to the reduction of the size, leading the weak coupling between the two dots. DQD A and B have the same DQD design, whereas DQD C has the stronger constriction in the interdot region than DQD A and B. We intended to realize the three different coupling regimes (weak, intermediate, and strong) between the two dots.

Figures 2(a)–2(c) show the gray-scale plots of the source–drain current, I_{sd} , as a function of the two side gate voltages in DQD A, B, and C, respectively. In the case of DQD A, the voltages of Gate 1 and Gate 3 electrode are used (V_{g1} and V_{g3}), and the source–drain voltage, V_{sd} , is 1 mV [Fig. 2(a)]. The current peak lines are almost parallel with each other. This fact indicates that a single quantum dot is responsible for the current oscillation because the coupling between DQDs is so strong. This is the strong coupling regime. The current oscillation in the center region of Fig. 2(a) is smeared because of another oscillation. Figure 3(a) shows the I_{sd} versus V_{g1} characteristics of DQD A, where V_{sd} is 2.5 mV. There are two types of Coulomb oscillations, which have a long and small period, respectively. The short period oscillation corresponds to the characteristics shown in Fig. 2(a) because the short period reflects the strong coupling between the gate and the charging island, and the size of the associated charging island should be relatively large, which should be defined by the entire DQD geometry. We then plot I_{sd} as a function of V_{g1} and V_{g3} in wide range, where $V_{sd} = -5 \text{ mV}$, as shown in

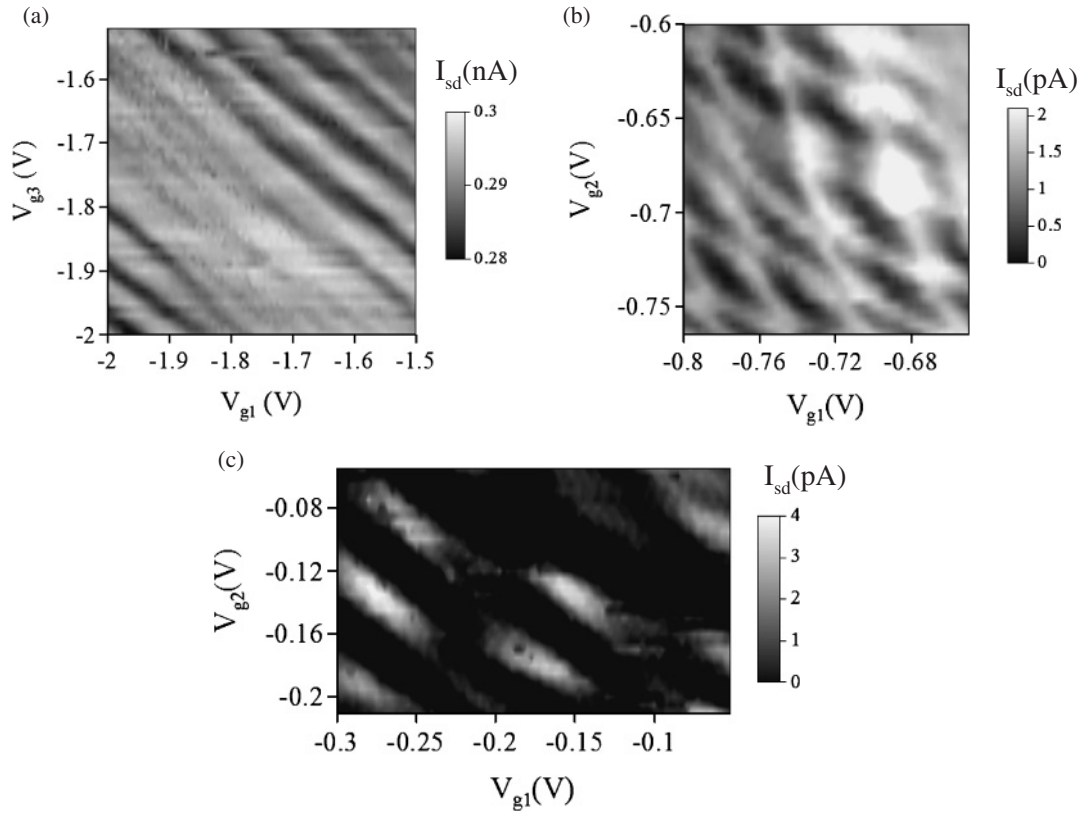


Fig. 2. The gray-scale plot of I_{sd} vs the two side gate voltages of the DQD structure with different interdot couplings. (a) The strong interdot coupling device is oxidized for 30 min at 1000 °C after EBL. Gate 1 and Gate 3 are used and $V_{sd} = 1$ mV. (b) The intermediate interdot coupling device is oxidized for 40 min at 1000 °C after EBL. Gate 1 and Gate 2 are used and $V_{sd} = 0.2$ mV. (c) The weak interdot coupling device is oxidized for 40 min at 1000 °C after EBL. Gate 1 and Gate 2 are used and $V_{sd} = 2$ mV. This device has a stronger constriction at the interdot region.

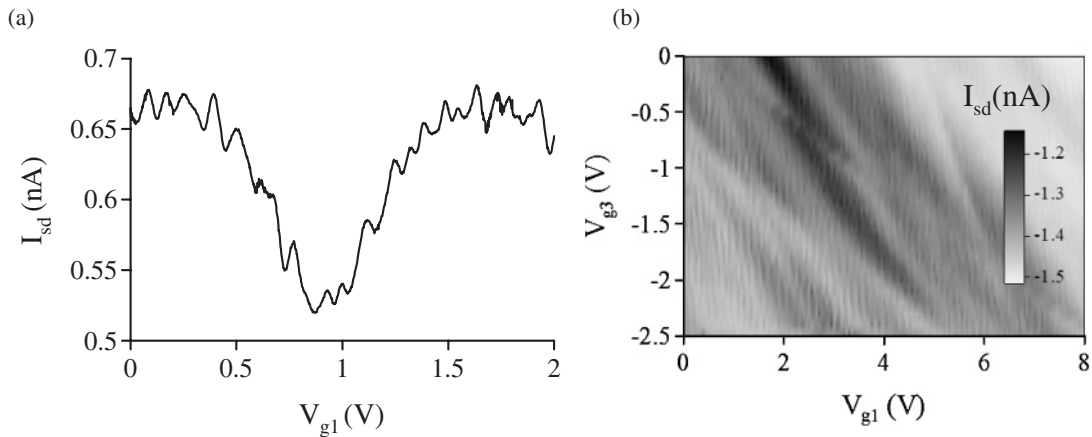


Fig. 3. The electrical characteristics of the first DQD device (strong coupling), which has a 30 min oxidation time at 1000 °C after EBL. (a) The I_{sd} vs V_{g1} characteristics, where $V_{sd} = 2.5$ mV. (b) The gray-scale image of the I_{sd} vs V_{g1} and V_{g3} characteristics, where $V_{sd} = -5$ mV.

Fig. 3(b). We observed several hexagonal charge stability regions as indicated by the black region. However, the long-period oscillations have obviously random peaks, and the charge triple point is not seen clearly. Therefore, the origin of the long-period oscillation may be multiple islands formed naturally by the potential of random impurities or defects. The smearing of the current peaks in Fig. 2(a) results from such long-period oscillation.

In the case of DQD B, the voltages of Gate 1 and Gate 2 electrode (V_{g1} and V_{g2}) are used, and V_{sd} is 0.2 mV

[Fig. 2(b)]. Because the interdot coupling in the DQD is reduced by oxidation, we observed successfully the hexagonal charge stability region of the DQD structure, which indicates that the intermediate coupling is realized.¹¹⁾ In the black region, the charges on each dot are stable. The current peaks appear at not only the charge triple points but also at the boundary of the charge stability region in Fig. 2(b). Since the constrictions of the DQDs are weak, leading the relatively strong electrostatic coupling between the DQD and the leads, the charging energies of each dot, which is

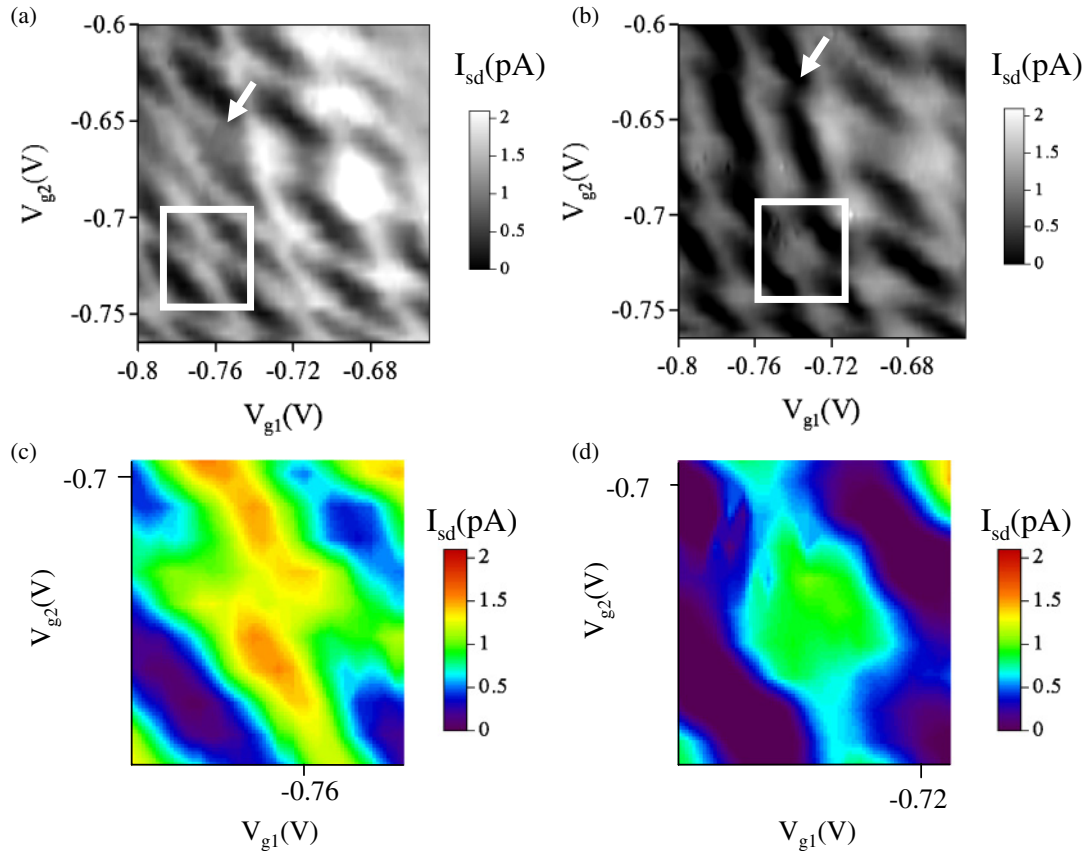


Fig. 4. (Color online) (a, b) The I_{sd} vs V_{g1} and V_{g2} characteristics of the second DQD device (intermediate coupling) with the 40 min oxidation time at 1000°C after EBL, where $V_{sd} = 0.2\text{ mV}$ and $V_{g3} = 0, -100\text{ mV}$, respectively. (c, d) The extended figures corresponding to the white square as shown in (a) and (b), respectively. The plot color is different to clearly show the change in the characteristics.

represented as E_{c1} and E_{c2} (see Appendix), are small. As a result, the thermal fluctuation current appears at the boundary of the charge stability region. Its current may also contain co-tunneling current.

In the case of DQD C, V_{g1} and V_{g2} are used and V_{sd} is 2 mV [Fig. 2(c)]. We observed the weak interdot coupling regime, in which the adjacent two charge triple points almost merge by making the interdot constriction stronger than that in DQD A and B. The island size is smaller than that of DQD A and B due to the strong constriction, and the thermal fluctuation current at the boundary of the charge stability region almost disappears. We realize the three different interdot coupling regimes in the DQD structure only by optimizing the structure design and thermal oxidation condition.

Subsequently, we choose the intermediate coupling device (DQD B) and apply the negative voltage at Gate 3 for controlling the electrostatic coupling in the DQD structures. In Fig. 4, the I_{sd} versus $V_{g1} - V_{g2}$ characteristics in DQD B are shown, where $V_{sd} = 0.2\text{ mV}$ and V_{g3} is changed from 0 [Fig. 4(a)] to -100 mV [Fig. 4(b)]. Figure 4(a) shows the same data as those in Fig. 2(b). Judging from the similarity of the entire current property between Figs. 4(a) and 4(b), the white squares indicate the same charge triple point. Figures 4(c) and 4(d) show the extended figures corresponding to the white square in Figs. 4(a) and 4(b), respectively, where the plot color is different. First, increasing the negative voltage of V_{g3} results in the shift of the charge

triple point to the upper right way because negative V_{g3} increases the electrochemical potential of each dot. Second, the current peaks at the boundary of the hexagonal region decrease with the increase of the negative gate voltage because of the change of the electrostatic coupling in the DQD structure. An electrostatic barrier is formed by the negative gate voltage, and the coupling between DQDs becomes weak. As a result, the charging energy becomes large, and the thermal fluctuation current decreases. Because the current peaks at the boundary, which are relevant to the electron number in the right dot [see the white arrows in Figs. 4(a) and 4(b)], mainly disappear in this device, the total capacitance of the left dot decreases more than that of the right dot.¹²⁾ Finally, the separation of the charge triple points merges with the increase of the negative gate voltage as shown clearly in Figs. 4(c) and 4(d). The interdot electrostatic coupling was modulated successfully from the intermediate-coupling state to the weak-coupling state by using the gate voltage. An applied voltage of as small as 100 mV was needed to change the DQD coupling state. This is about one order of magnitude smaller than those reported for other top-gate devices.^{9,10)} This is because the DQD structure initially has the intermediate coupling. The interdot coupling is roughly controlled by fabricating the DQD structure geometrically, and then we can precisely modulate the coupling in the DQD by applying the small voltage. This is a very useful technique for future integration with Si SOI CMOS structures because of its low-power consumption.

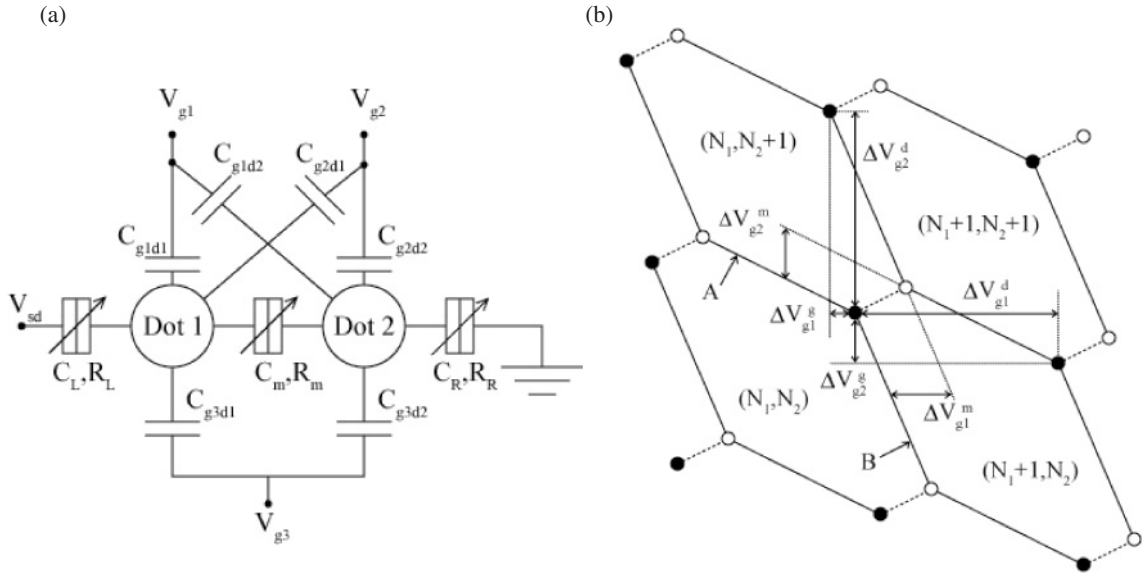


Fig. 5. (a) The equivalent circuit of the DQD structure. (b) The schematic stability diagram of the DQD system with the cross-coupling of the gate. The black and white points are charge triple points. (N_1, N_2) indicate the equilibrium charge number on each dot.

4. Equivalent Circuit Simulation

In order to confirm the validity of the argument presented in the previous section, we simulated the electron transport properties in the DQD structure by using an electron circuit simulator based on Monte Carlo technique. The tuning of the electrostatic potential of the DQD structure by the side gate voltage can be realized effectively by changing the tunneling capacitances. First, the gate capacitances should be estimated. Figure 5(a) shows the equivalent circuit of the DQD structures, which have the cross-coupling between Gate 1(2) and Dot 2(1). In this model, gate capacitances are calculated as follows (a full derivation is shown in Appendix):

$$C_{g1(2)d1(2)} = \frac{\Delta V_{g2(1)}^d}{\Delta V_{g1}^d \Delta V_{g2}^d - \Delta V_{g1}^g \Delta V_{g2}^g} |e|, \quad (1)$$

$$C_{g1(2)d2(1)} = \frac{\Delta V_{g2(1)}^g}{\Delta V_{g1}^d \Delta V_{g2}^d - \Delta V_{g1}^g \Delta V_{g2}^g} |e|, \quad (2)$$

where $\Delta V_{g1(2)}^d$ and $\Delta V_{g1(2)}^g$ are the spacings between the two adjacent charge triple points [see Fig. 5(b)]. In the case of Figs. 2(b) and 2(c), we estimate the gate capacitances of the DQD structures by using eqs. (1) and (2). From Fig. 2(b), the gate capacitances of the DQD structure are as follows: $C_{g1d1} = 4.15$ aF, $C_{g2d2} = 4.81$ aF, $C_{g1d2} = 0.87$ aF, and $C_{g2d1} = 2.84$ aF. Similarly, from Fig. 2(c), the gate capacitances of the DQD structure are as follows: $C_{g1d1} = 2.08$ aF, $C_{g2d2} = 2.70$ aF, $C_{g1d2} = 0.89$ aF, and $C_{g2d1} = 1.95$ aF. Since Fig. 2(a) shows the single dot property, we estimate the gate capacitances simply by using the current peak spacings in such way that the simulated data conform to the experimental data as follows: $C_{g1d1} = 1.20$ aF, $C_{g2d2} = 1.50$ aF, $C_{g1d2} = 0.30$ aF, and $C_{g2d1} = 0.30$ aF. Then the ratio between the total capacitance $C_{1(2)}$ (see Appendix) and interdot capacitance C_m is calculated as follows:

$$\frac{C_{1(2)}}{C_m} = \frac{|e|}{C_{g2(1)d2(1)} \Delta V_{g2(1)}^m} - \frac{C_{g2(1)d1(2)}}{C_{g2(1)d2(1)}} \quad (3)$$

where $\Delta V_{g1(2)}^m$ is the spacing shown in Fig. 5(b) (a full derivation is shown in Appendix). However, it is difficult to estimate the total capacitance from the experimental data because the thermal fluctuation smears the separation of the charge triple point. Therefore, we selected the reasonable value of the total capacitances (several tens of aF) from Coulomb blockade characteristics.

Figures 6(a)–6(c) show the simulation results that correspond to the DQD structure shown in Figs. 2(a)–2(c), respectively. By choosing the appropriate value of the total capacitances, the simulation data show good agreement with the experimental electron transport property. This indicates that our equivalent circuit model is reasonable, and our structures act as the DQD structure. The current level in the simulation data of Figs. 6(b) and 6(c) is larger than the experimental one. This is probably because the series resistances in the semiconductor leads are not taken into account in the simulation model. As shown in Fig. 4(b), the voltage of Gate 3 reduces the total capacitance of the left dot mainly, as stated above. To confirm this phenomenon, we reduce the total capacitance of the left dot more than the right dot. Figure 6(d) shows a similar simulation of Fig. 6(b), in which the only difference is the total capacitance of the DQD. The total capacitances of the left and the right dot are 51.9 and 50.7 aF as shown in Fig. 6(b), and 24.9 and 40.7 aF as shown in Fig. 6(d), respectively. The peak current of the boundaries successfully disappears. This is one evidence that the negative gate voltage of Gate 3 modulates the electrostatic coupling in the DQD structure.

5. Conclusions

We have demonstrated the modulation of electrostatic coupling in the silicon DQD structure as the change of tunneling current. The modulation of electrostatic coupling in the DQD expected to improve the qubit operation and the QCA switching. We realized the three regimes of interdot coupling (weak, intermediate, and strong coupling) in the

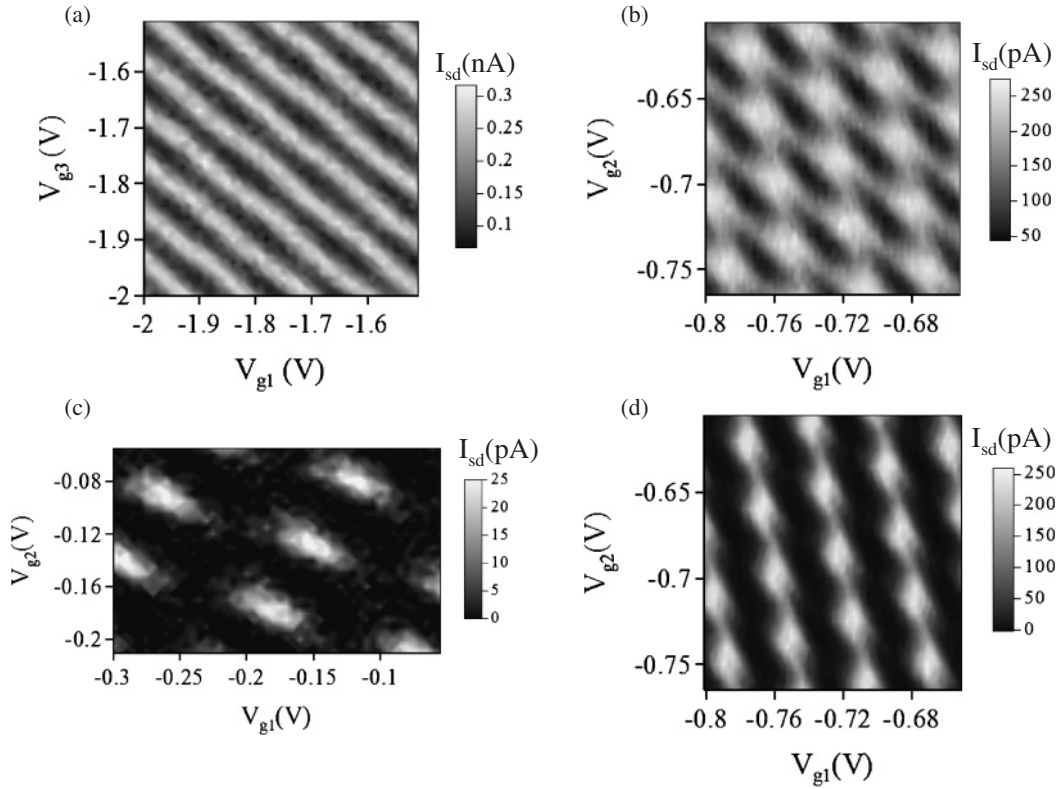


Fig. 6. The simulated I_{sd} vs V_{g1} and V_{g2} characteristics of the DQD structure. (a) The gate capacitances are as follows: $C_{g1d1} = 1.20$ aF, $C_{g2d2} = 1.50$ aF, $C_{g1d2} = 0.30$ aF, $C_{g2d1} = 0.30$ aF. The total capacitances are as follows: $C_1 = 91.5$ aF, $C_2 = 91.8$ aF. The interdot capacitance is 65.0 aF. (b) The gate capacitances are as follows: $C_{g1d1} = 4.15$ aF, $C_{g2d2} = 4.81$ aF, $C_{g1d2} = 0.87$ aF, $C_{g2d1} = 2.84$ aF. The total capacitances are as follows: $C_1 = 51.9$ aF, $C_2 = 50.7$ aF. The interdot capacitance is 18 aF. (c) The gate capacitances are as follows: $C_{g1d1} = 2.08$ aF, $C_{g2d2} = 2.70$ aF, $C_{g1d2} = 0.89$ aF, $C_{g2d1} = 1.95$ aF. The total capacitances are as follows: $C_1 = 23.8$ aF, $C_2 = 18.9$ aF. The interdot capacitance is 1.83 aF. (d) The gate capacitances are as follows: $C_{g1d1} = 4.15$ aF, $C_{g2d2} = 4.81$ aF, $C_{g1d2} = 0.87$ aF, $C_{g2d1} = 2.84$ aF. The total capacitances are as follows: $C_1 = 24.9$ aF, $C_2 = 40.7$ aF. The interdot capacitance is 8 aF.

DQD structure only by optimizing the DQD design and thermal oxidation condition. We then demonstrated electrostatic coupling in the DQD by applying a small voltage on the side gate such as -100 mV. Furthermore, our device has a compact DQD structure, and its fabrication process is compatible with the Si SOI CMOS process. This device is suitable for future integration with Si CMOS devices because of its low-power consumption and its compact design. In addition, we show the calculation of the DQDs' capacitances, and the theoretical electron transport property in the equivalent circuit simulation demonstrates good agreement with the experimental data. The simulation for the modulation of electrostatic coupling by the side gate voltage was also realized effectively by changing the tunneling capacitances.

Acknowledgement

The authors would like to acknowledge D. Williams of Hitachi Cambridge Laboratory for his insightful discussions. This work is partly supported by a Grant-in-Aid for Scientific Research (19206035) from the Japan Society for the Promotion of Science (JSPS). One of the authors, (G.Y.), is supported by the JSPS Research Fellowship for Young Scientists.

Appendix

First, we calculate the electrostatic energy $U(N_1, N_2)$ of the DQD system as shown in Fig. 5(a), which is the same method as that of ref. 13. Then the electrochemical potentials $\mu_{1(2)}(N_1, N_2)$ of dot 1(2) are given by

$$\begin{aligned}
 \mu_1(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1 - 1, N_2) \\
 &= \left(N_1 - \frac{1}{2}\right)E_{C1} + N_2E_{Cm} - \frac{1}{|e|} [(C_{g1d1}E_{C1} + C_{g1d2}E_{Cm})V_{g1} \\
 &\quad + (C_{g2d2}E_{Cm} + C_{g2d1}E_{C1})V_{g2} + (C_{g3d1}E_{C1} + C_{g3d2}E_{Cm})V_{g3}] \\
 \mu_2(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1, N_2 - 1) \\
 &= \left(N_2 - \frac{1}{2}\right)E_{C2} + N_1E_{Cm} - \frac{1}{|e|} [(C_{g1d1}E_{Cm} + C_{g1d2}E_{C2})V_{g1} \\
 &\quad + (C_{g2d2}E_{C2} + C_{g2d1}E_{Cm})V_{g2} + (C_{g3d1}E_{Cm} + C_{g3d2}E_{C2})V_{g3}]
 \end{aligned} \tag{A.1}$$

with

$$E_{C1} = e^2 \frac{C_2}{C_1 C_2 - C_m^2}; \quad E_{C2} = e^2 \frac{C_1}{C_1 C_2 - C_m^2}; \quad E_{Cm} = e^2 \frac{C_m}{C_1 C_2 - C_m^2} \quad (\text{A}\cdot 2)$$

and

$$\begin{aligned} C_1 &= C_L + C_m + C_{g1d1} + C_{g2d1} + C_{g3d1} \\ C_2 &= C_R + C_m + C_{g1d2} + C_{g2d2} + C_{g3d2} \end{aligned} \quad (\text{A}\cdot 3)$$

From the conditions of $\mu_1(N_1 + 1, N_2) = 0$ and $\mu_2(N_1, N_2 + 1) = 0$, we obtain the equations for the boundary of the hexagonal region as marks A and B in Fig. 5(b), respectively. The intersection of line A and line B [$V_{g1}(N_1, N_2)$, $V_{g2}(N_1, N_2)$] in Fig. 5(b) is calculated as follows:

$$V_{g1(2)}(N_1, N_2) = \frac{|e|}{C_{g1d1} C_{g2d2} - C_{g1d2} C_{g2d1}} (C_{g2(1)d2(1)} N_{1(2)} - C_{g2(1)d1(2)} N_{2(1)}) + \text{const.} \quad (\text{A}\cdot 4)$$

Considering that $C_{g1(2)d1(2)}$ is larger than $C_{g1(2)d2(1)}$, we can derive the separation between the adjacent triple point as follows:

$$\begin{aligned} \Delta V_{g1}^{(d)} &= V_{g1}(N_1 + 1, N_2) - V_{g1}(N_1, N_2) \\ \Delta V_{g1}^{(g)} &= V_{g1}(N_1, N_2) - V_{g1}(N_1, N_2 + 1) \\ \Delta V_{g2}^{(d)} &= V_{g2}(N_1, N_2 + 1) - V_{g2}(N_1, N_2) \\ \Delta V_{g2}^{(g)} &= V_{g2}(N_1, N_2) - V_{g2}(N_1 + 1, N_2) \end{aligned} \quad (\text{A}\cdot 5)$$

Solving eqs. (A-4) and (A-5), we obtain eqs. (1) and (2).

From

$$\begin{aligned} \mu_1(N_1, N_2; V_{g1}, V_{g2}) &= \mu_1(N_1, N_2 + 1; V_{g1} + \Delta V_{g1}^m, V_{g2}) \\ \mu_2(N_1, N_2; V_{g1}, V_{g2}) &= \mu_2(N_1 + 1, N_2; V_{g1}, V_{g2} + \Delta V_{g2}^m) \end{aligned} \quad (\text{A}\cdot 6)$$

we obtain eq. (3).

- 1) M. A. Nielsen and I. L. Chuang: *Quantum Computation and Quantum Information* (Cambridge University Press, Cambridge, U.K., 2000).
- 2) Y. Nakamura, Yu. A. Pashkin, and J. S. Tsai: *Nature* **398** (1999) 786.
- 3) I. Chiorescu, Y. Nakamura, C. J. P. M. Harmans, and J. E. Mooij: *Science* **299** (2003) 1869.
- 4) J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard: *Science* **309** (2005) 2180.
- 5) G. Yusa, K. Muraki, K. Takashina, K. Hashimoto, and Y. Hirayama: *Nature* **434** (2005) 1001.
- 6) T. Hayashi, T. Fujisawa, H. D. Cheong, Y. H. Jeong, and Y. Hirayama: *Phys. Rev. Lett.* **91** (2003) 226804.
- 7) J. Gorman, D. G. Hasko, and D. A. Williams: *Phys. Rev. Lett.* **95** (2005) 090502.
- 8) M. Mitic, M. C. Cassidy, K. D. Petersson, R. P. Starrett, E. Gauja, R. Brenner, R. G. Clark, A. S. Dzurak, C. Yang, and D. N. Jamieson: *Appl. Phys. Lett.* **89** (2006) 013503.
- 9) A. Fujiwara, H. Inokawa, K. Yamazaki, H. Namatsu, Y. Takahashi, N. M. Zimmerman, and S. B. Martin: *Appl. Phys. Lett.* **88** (2006) 053121.
- 10) Y. Hu, H. O. H. Churchill, D. J. Reilly, J. Xiang, C. M. Lieber, and C. M. Marcus: *Nat. Nanotechnol.* **2** (2007) 622.
- 11) Although the V_{sd} of 0.2 mV is too small to observe the single electron transport property at a temperature of 4.2 K, which corresponds to thermal fluctuation $k_B T \sim 0.36$ meV, the actual applied voltage may be more than 0.2 mV due to the offsetting of voltage in our measurement system.
- 12) In the current peaks at the boundary, which are relevant to the electron number in the right dot, Coulomb blockade in the right dot is lifted. If the charging energy of the left dot is large, which corresponds to the small total capacitance, the thermal current disappears.
- 13) W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven: *Rev. Mod. Phys.* **75** (2003) 1.