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Single-electron tunnelling via quantum dot cavities built on a silicon suspension nanobridge

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Abstract

This paper presents fabrication and characterization of novel nanoscale Si transistors with a suspended quantum dot cavity formed on a nanobridge channel. A 300-nm-long and 50-nm-wide nanobridge channel and quantum dot cavities were successfully fabricated on silicon-on-insulator (SOI) substrates and nanocrystalline silicon films by using the electron beam lithography combined with isotropic and anisotropic etching. We observed clear Coulomb oscillation for the fabricated nanobridge transistors at higher temperatures compared with transistors with a non-suspended channel.

Keywords: Si nanobridge; NEMS; Quantum dot; Single-electron tunnelling

1. Introduction

Recent advance on fabricating silicon nano electromechanical systems (NEMS) has enabled us to study single-electron tunnelling through nanometer-scale suspended structures with restrained coupling to the environment [1]. In particular, a suspended quantum dot (QD) cavity structure built on a Si nanobridge (NB) provides an ideal system to explore the interaction of single electrons with tailored phonon spectrum in the cavity which is acoustically isolated from the Si substrate. Such a system has recently become of great interest in terms of studying physics of decoherence mechanisms for quantum bits and also revealing ultimate energy dissipation process in Si nanostructures. We also expect for such systems a variety of new electromechanical phenomena to emerge, which include formation of phononic bandgaps and phonon confinement [2], a reduction of electron–phonon interaction [3], phonon blockade [4], metal-insulator transition, quantization of nanomechanical motion [5], and a strong coupling of nanomechanical and electron motions [6]. These phenomena may lead to novel functional Si nano information devices [7] which are not achieved by using the conventional bulk Si CMOS technologies. In this paper we report on fabrication of Si NB transistor with an integrated QD cavities and characterization of single-electron tunnelling properties for the first time.

2. Device design and basic fabrication process for the Si NB transistor

We designed the Si NB transistor as Fig. 1. A NB is suspended over the Si substrate and held by both side like a bridge. We make the Si NB transistor using the NB as a channel and locating side gates near the NB channel to modulate electrical potential in the NB channel.

The Si NB was fabricated on the silicon on insulator (SOI) wafer by using a buried oxide (BOX) layer as a

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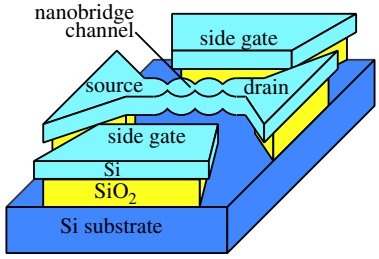

Fig. 1. Device structure of the Si NB transistor.

sacrificial layer. A Si nanowire channel and electrodes were patterned on a heavily-doped SOI layer by using electron beam lithography (EBL) and anisotropic electron cyclotron resonance reactive ion etching. After that, we isotropically etched the BOX layer under the nanowire channel with liquid HF, and a suspended NB channel was formed.

3. Dot integration

As for integration of QD cavities on a NB, we examined two ways. One is direct patterning the QD cavities with EBL, and the other is utilizing QDs naturally formed in the nanocrystalline Si (nc–Si) thin film.

Fig. 2a shows a NB in which multiple QD cavities were patterned by EBL and Fig. 2b shows a NB thermally oxidized after patterning the QDs. Here we first etched the NB in the wedged shape using EBL and made a potential barrier in thin regions of the NB by thermal oxidation. In this process we can locate the multiple QDs to specific places on the NB and the size of QDs can also be controlled to some extent via oxidation process.

In the second option, we can introduce a larger number of QDs with smaller dimensions by employing a nc–Si film [8], as shown in Fig. 2c. We use the heavily-doped nc–Si film grown by using low pressure chemical vapor deposition on a thermally grown oxide layer. We carried out thermal oxidation to convert grain boundaries into silicon suboxide [8], which can be applied to a high quality tunnel barrier.

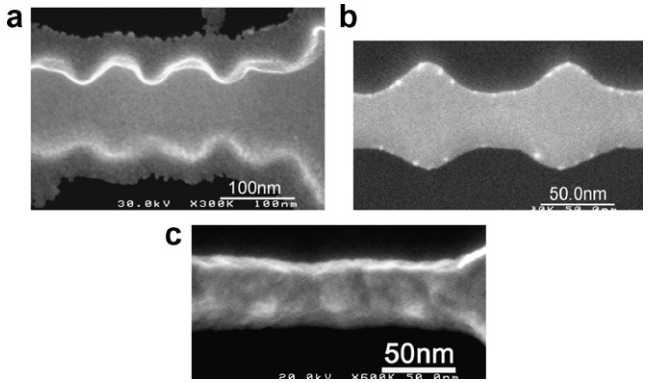

Fig. 2. Multiple QD cavities were embedded in the NB by (a) patterning with EBL, (b) oxidizing at 1100 °C for 24 min after EBL and (c) employing nc–Si film.

4. The characteristics of single electron transport

We performed electrical measurements of the fabricated Si NB transistors to characterize the Si NB on which single QD cavity was embedded (see inset of Fig. 3). We keep the Si NB transistor at low temperature with a low temperature prober "Nagase BCT-10MDC". Then we apply source drain voltage and side gate voltage and measure source drain current with a semiconductor device analyzer "Agilent B1500A". The Si NB transistor exhibited a clear Coulomb diamond at 20 K and the Coulomb oscillation persisted up to around 100 K, as shown in Fig. 3.

From the Coulomb diamond, we estimated that the gate capacitance C_g is 0.376 aF and the tunnel capacitances C_1 and C_2 are 2.70 aF and 2.02 aF, respectively, [9]. The total capacitance $C_\Sigma = C_g + C_1 + C_2$ is 5.10 aF. These values agree with the theoretical values obtained for the QD geometry by conducing numerical simulation. These results indicate the patterned QD cavity works as a charging island and responsible for the Coulomb oscillation. As a reference we also measured characteristics of a QD cavity embedded on a non-suspended channel, and observed the Coulomb oscillation only at lower temperatures, below 50 K. The estimated capacitances for the non-suspended QD C_g, C_1, C_2 and C_Σ are 0.138 aF, 9.99 aF, 5.60 aF and 15.7 aF, respectively.

The reason why the gate capacitance for the suspended QD is larger than that for the non-suspended QD is a difference in size of the QDs caused by fluctuation of EBL. On the other hand, the tunnel capacitances for the suspended QD are about three times smaller than those for the non-suspended QD. The tunnel capacitances are almost determined by the cross sections of the QDs which strongly depend on a thermal oxidation after EBL. The oxidation

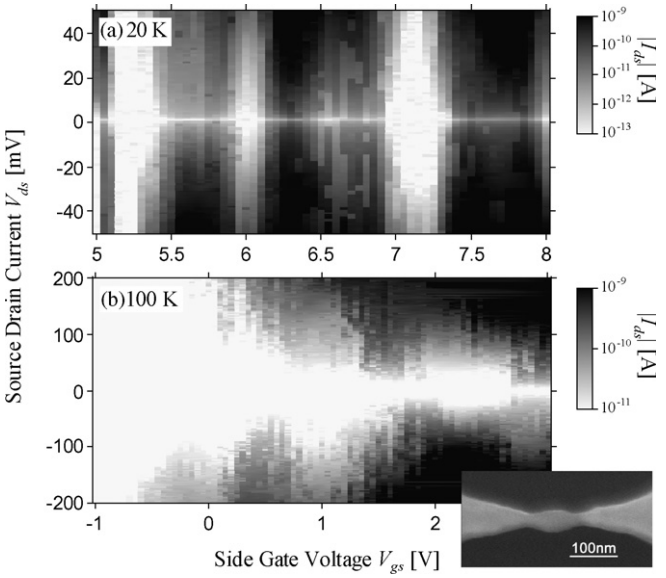

Fig. 3. Single electron transistor characteristics of a Si NB transistor in which a single QD cavity was embedded at temperature of (a) 20 K and (b) 100 K. Inset shows the SEM image of the Si NB.

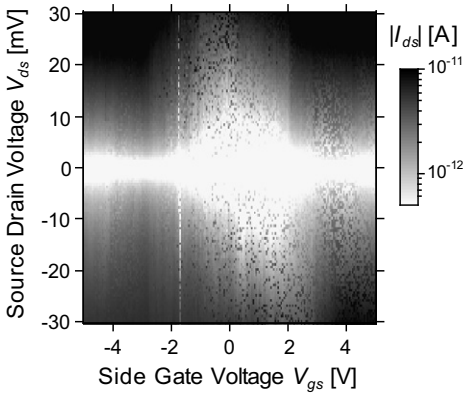

Fig. 4. A Coulomb diamond in a nc–Si bridge made of the nc–Si film.

proceeds from the all-around surfaces and therefore works to reduce the area of the tunnel junctions more effectively for the suspended device.

We also performed electrical measurement of a Si NB transistor made of the nc–Si film and observed a coulomb diamond at 20 K as shown in Fig. 4. We oxidized the nc–Si bridge at 750 °C for 20 min to grow tunnel barriers. This oxidation was insufficient for the Si NB transistor to work as a single electron transistor at high temperature [10]. However we could probably grow more homogeneous double tunnel barriers without using lithography techniques than those fabricated by using EBL, and observe the more symmetrical Coulomb diamond.

5. Conclusion

We could build fabrication method for QD cavities in NBs by using two ways. One is direct patterning QD cavities with EBL, and the other is utilizing QDs naturally-formed in the nc–Si thin film. We performed electrical measurement of the fabricated Si NB transistors and observed the Coulomb oscillation in the QD cavities built on the Si suspension NBs for the first time.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.mee.2008.01.068.

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