Stochastic Coulomb blockade in coupled asymmetric silicon dots formed by pattern-dependent oxidation

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This paper reports the observation of stochastic Coulomb blockade for the coupled silicon dots. The device was fabricated from the highly doped dual recess structured silicon channel by means of stress induced pattern-dependent oxidation. Sparsely placed Coulomb oscillation characteristics were observed from the transport characteristics at a low temperature and these irregularities decreased linearly as temperature increased. These characteristics were interpreted as the stochastic Coulomb blockade effect, which occurs due to the mismatch between individual dots in the energy spectrum ladder of the serially connected dots. © *2008 American Institute of Physics*.
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Silicon-based single electron devices (SEDs) have been studied for their practical applications. This is mainly due to their higher operating temperature[1] and larger potential for the circuit applications with a clear emphasis on silicon-on-insulator (SOI) substrates.[2] Most of these studies are based on single-dot devices but multiple-dot devices have been proposed as basic units for more stable single-electronic circuits due to the suppression of the inevitable quantum mechanical cotunneling process.[3] Many interesting phenomena have been reported in the GaAs-based double-dot system, which include stochastic Coulomb oscillation,[4] peak splitting, and quasiperiodic beating.[5]

Despite the silicon SEDs practical importance, even double-dot systems have not been studied extensively. Usually, a silicon double-dot system is realized by either a geometrically defined channel structure[6] or gate electrode controlled electrostatic potential barriers.[7] Most importantly, silicon SEDs fabricated by the pattern-dependent oxidation (PADOX) mechanism have been shown to operate quite stably in the long-term drift.[8] Recently, we reported strongly coupled symmetric dots characteristics based on PADOX dots formation in the dual recess structured silicon channel.[9] In this paper, coupled asymmetric dots fabricated by the same process was used to study the stochastic Coulomb blockade characteristics.[10] Previously, in the silicon dot system, stochastic Coulomb blockade has been referred to in the unintentionally formed dots.[11] However, no detailed stochastic Coulomb blockade oscillation experimental results have been reported in an intentionally formed silicon dot system.

The physical mechanism of stochastic Coulomb blockade oscillation, first reported by Ruzin *et al.*,[10] is as follows. In a double-dot system at a finite low temperature, conductance occurs if the energy spectrum rungs of two dots fall within the limits imposed by thermal smearing. This means that following two conditions have to be met simultaneously for a negligible cross gate coupling on the dots,

$$\left| eV_{g1} - \left(n_1 + \frac{1}{2} \right) \Delta_1 \right| \leq k_B T, \tag{1}$$

$$\left| eV_{g2} - \left(n_2 + \frac{1}{2} \right) \Delta_2 \right| \leq k_B T, \tag{2}$$

where n_1 (n_2) is the numbers of electrons on dot 1 (dot 2), and $\Delta_{1(2)} \equiv e^2 / C_{G1(2)}$. V_{G1} and V_{G2} are the gate voltages to dots 1 and 2, respectively. This condition is easily satisfied at a high temperature. However, with the decrease in temperature, the number of suppressed peaks increases linearly because $k_B T$ determines the allowable mismatch between the conductance ladders of dots 1 and 2. Thus, at a low temperature, the number of conductance peaks becomes sparsely placed. In this article, we report the observed stochastic Coulomb blockade in the coupled asymmetric silicon dots system.

Device fabrication process is as follows. SOI wafer with an original SOI thickness of 100 nm and a buried-oxide (BOX) layer thickness of 200 nm was used to fabricate this device. Initially, the substrate was thermally oxidized and phosphorus ion was implanted ($\sim 10^{19}$ cm^{-3}). Recess structure was patterned on the substrate by electron beam lithography and the pattern was transferred to the SOI layer by reactive ion etching. Again, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI layer. The scanning electron microscopy (SEM) image of the measured dual recess structured device is shown in Fig. 1(a). The bright regions indicate the SOI layer and the dark regions indicate the BOX layer of the substrate. Although oxidation mechanism is different for the doped silicon and the intrinsic silicon, atomic force microscopy measurement of our devices (which is doped silicon) indicated lower thickness in the narrow recess regions compared with the wider regions. This is attributed to the compressive stress build up in the narrow recess region[12] and consequent suppression of further oxidation, which is essential for PADOX dot formation.[1]

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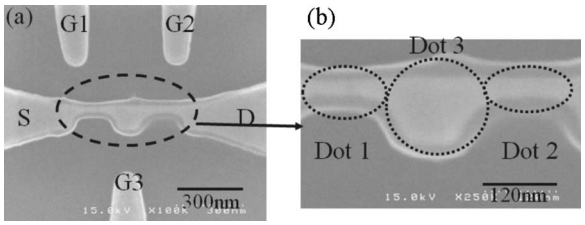

FIG. 1. (a) SEM image of the measured coupled silicon dots device. Scale bar is 300 nm. (b) Zoomed-in SEM image of the dual recess region and the possible locations of dots. Scale bar is 120 nm.

A proposed effective potential model[13] explains the tunnel barriers formation in PADOX device by considering the bandgap modulation due to the quantum confinement and the oxidation induced stress. The PADOX dot formation in the dual recess device is as follows. When the device is oxidized, narrow recess regions are immediately oxidized and surrounded by SiO_2. The newly grown oxide layer generates large compressive stress, which leads to self-limiting oxidation in the narrow regions.[12] It is reported that this compressive stress leads to bandgap reduction by more than 100 meV.[14] Also, the shear stress caused by the backside oxidation in the wide region leads to lower compressive stress around the ends of recess regions.[8] On the other hand, a single potential barrier is introduced in each narrow recess regions due to the quantum size effect.[13] As a combined result of quantum size caused potential barrier and stress induced bandgap reduction, a potential well is introduced at the center of each recess. This leads to double-tunnel-barrier potential formation in each recess region. The reported PADOX dots formation in a cross-shaped silicon wire[2] supports our scenario of dot formation very well. The possible locations of anticipated dots are marked in Fig. 1(b). Asymmetry in the expected dots 1 and 2 areas can also be noticed from the zoomed-in recess region SEM image [Fig. 1(b)]. Furthermore, it has to be noticed that the expected dot 3 is much larger than the other dots. Gate G3 and substrate were kept grounded throughout the measurement.

The measured gate G1 Coulomb oscillation characteristic with gate G2 grounded is shown in Fig. 2. From this contour plot, the presence of Coulomb diamonds with the different Coulomb gaps can be noticed. Clear Coulomb oscillations were observed with overlapping Coulomb diamonds for gate G2 sweep as well. The consistency of overlapping diamonds for both dot gates sweep over such a large

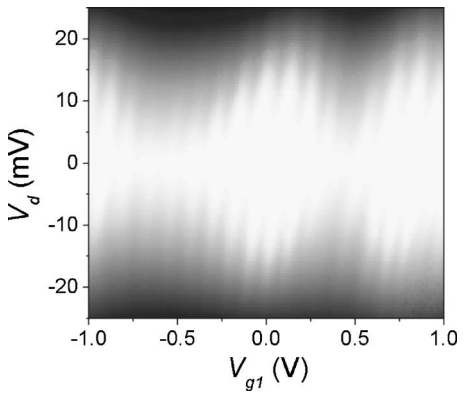

FIG. 2. Measured drain current magnitude as a function of gate G1 and drain voltages at 4.2 K. Gates G2 and G3 were kept grounded. The gray scale plot runs from the minimum current (white) 0 A to the maximum current (black) at 335 pA.

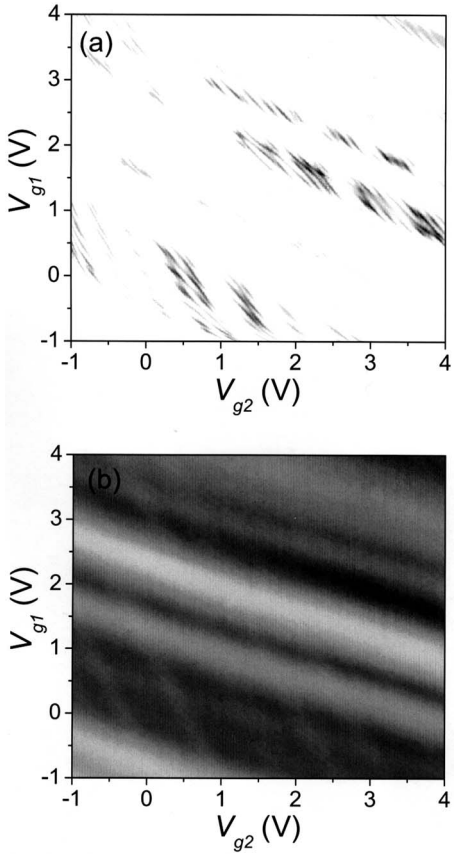

FIG. 3. (a) Contour plot of the drain current as a function of V_{G1} and V_{G2} at 4.2 K for the drain voltage value of 1 mV. The gray scale plot runs from the minimum current (white) 0 A to the maximum current (black) at 163 pA. (b) Contour plot of the drain current as a function of V_{G1} and V_{G2} at 25 K for the drain voltage value of 1 mV. The gray scale plot runs from the minimum current (white) 0 A to the maximum current (black) 1.36 nA.

gate voltage range confirms that this device contains more than one dot in the channel.[15] The contour plot of the measured drain current as a function of the gate voltages G1 and G2 is shown in Fig. 3(a) for the drain voltage value of 1 mV at 4.2 K. Anticrossing behavior and sparsely placed conductance maxima can be observed from this measurement result. Clear anticrossing characteristic indicates that the channel dots are strongly coupled.[16] Figure 3(b) shows the contour plot of the drain current at 25 K. It can be noticed from this contour plot that the Coulomb oscillation characteristics almost vary as a function of gate G1 voltage (V_{G1}). At this temperature, the discreteness of charge on dot 2 starts to vanish because of the larger dot size and the impression of dot 2 Coulomb blockade still remains in this plot. The most important characteristic to be noticed from the 4.2 K drain current plot is the absence of a large number of conductance maxima. However, at a high temperature [25 K, Fig. 3(b)], this stochastic behavior is absent. The observation of the irregular Coulomb oscillation at a low temperature [Fig. 3(a)] and the increase in the number of coulomb oscillation peaks with an increasing temperature is the key signature of the stochastic Coulomb blockade in coupled asymmetric dots.

In Figs 4(a) and 4(b), drain current measurement as a function of gate G2 voltage (V_{G2}) is shown for the temperatures of 2.5, 3.5, 8, 10, and 12 K, respectively. From this plot, it should be noticed that conductance peak positions do not vary with the temperature. This confirms the stable na-

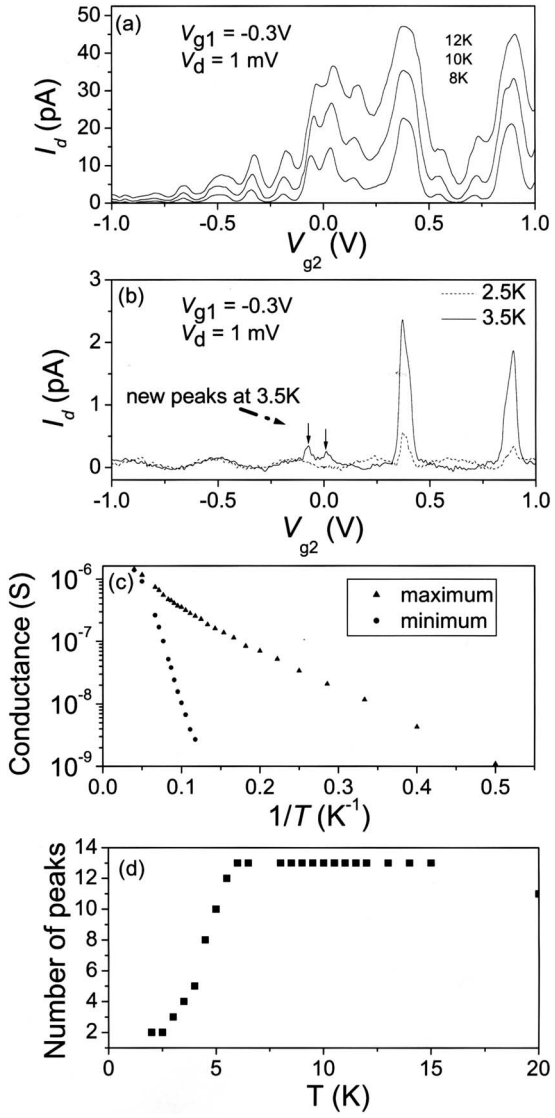

FIG. 4. [(a) and (b)] Drain current as a function of V_{G2} for various temperatures. (c) Conductance *Vs* T^{-1} for a maximum (V_d=0.1 mV, V_{G1}=−0.3 V and V_{G2}=0.38 V) and a minimum (V_d=0.1 mV, V_{G1}=−0.3 V and V_{G2} =0.63 V) in the transport characteristics on a semilogarithmic scale. (d) The number of peaks counts for various temperatures, V_d=0.1 mV, V_{G1}=−0.3 V, and V_{G2} from −1 to 1 V.

ture of the measured transport characteristics in the coupled dots, as indicated in Fig. 1(b), and not due to the disorder/surface roughness-induced multiple dots in the channel. Arrows in Fig. 4(b) mark the emergence of two new peaks at 3.5 K compared to 2.5 K. To further confirm the measured characteristics as stochastic Coulomb blockade, the measurement of the number of conductance peak variation with the temperature was carried out. The conductance minimum will occur due to either thermal activation or cotunneling mechanism. The background conductance activates exponentially with temperature for the thermally activated conductance.[17] In the case of cotunneling, background conductance increases quadratically with temperature.[18] In order to discriminate between the possible mechanisms of background conduction, temperature dependence measurement of the conductance maximum and minimum was performed. Conductance *Vs* T^{-1} for a maximum and a minimum is shown in Fig. 4(c) on a semilogarithmic scale. The exponential increase of conductance minima with temperature indicates the thermally activated conductance mechanism in the device transport characteristics. As conductance minima are thermally activated in this device, the entire conductance peaks were taken into account in the peak-counting procedure. The counted number of peaks as a function of temperature from 2 to 20 K is shown in Fig. 4(d) for the drain voltage of 0.1 mV, V_{G1}=−0.3 V and V_{G2} from −1 to 1 V. It can be noticed from this plot that the number peaks increase linearly with temperature from 2 to 6 K and then saturates. Peak count remains constant until dot 2 is in the Coulomb blockade condition, that is, about 20 K. Once dot 2 is out off its Coulomb blockade temperature range, the number of peaks starts to decrease. A similar change in the number of peaks was observed at the other gate voltage ranges as well. From these measurement results, it can be concluded that the transport in the coupled asymmetric dots indeed occurs in agreement with the predicted stochastic Coulomb blockade regime, as reported in Ref. 10.

In conclusion, we reported the experimental result of stochastic Coulomb blockade for the coupled asymmetric silicon dots in the dual recess structured silicon channel formed by PADOX process. The observed linear breakdown of sparsely placed Coulomb oscillations with the increase in temperature confirms the stochastic Coulomb blockade characteristics. The significant invariance of each peak position with the temperature validates the hypothesis of coupled dot formation and confirms that conductance is not due to the disordered nanowire.

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