Strongly coupled multiple-dot characteristics in dual recess structured silicon channel

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Silicon single electron transistors were fabricated by using the highly doped silicon channel with dual recess structure along with two recess gates and one central island gate as a pattern. The transition of Coulomb oscillation characteristics from a single dot to a strongly coupled multiple dot was demonstrated for the different oxidation times and recess dimensions. The multiple-dot characteristic in the longer post lithography oxidized sample is attributed to the formation of a single dot in each recess due to the stress induced pattern-dependent oxidation, which leads to multiple dot in the channel. The temperature variation measurement, which was performed after two thermal cycling of the same sample to 20 and 4.2 K with 1 month gap, revealed the highly stable nature of the multiple-dot device transport characteristics. The multiple-dot device can also be operated as a unique nonlinear tunable resistance single electron transistor. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2885343]

I. INTRODUCTION

Single electron devices (SEDs) have been studied widely for various applications due to their high charge sensitivity,[1,2] low power consumption, and multifunctionality.[3,4] Silicon based SEDs have attracted great attention because of their higher operating temperature[5] and larger potential for circuit applications with a clear emphasis on silicon-on-insulator (SOI) substrates.[6,7] Most importantly, stability against long-term drift of the single electron transistors (SETs) fabricated by metal-oxide-semiconductor processes on the SOI substrates has already been demonstrated for seven years.[8] Furthermore, silicon based Coulomb blockade devices are compatible with the current advances in the very large scale integrated technology.[9] Thus, it is also important to investigate these devices for future quantum information technology.

Radio-frequency SET (rf-SET) is a prime candidate for the quantum information device readout. Recent investigations have addressed the use of the rf-SET as a readout device for charge-based qubits[10] and a detector of single electron dynamics.[11] The crucial requirement to realize the rf-SET applications in silicon is low resistance silicon SET.[12] Usually, tunnel junction resistance of the silicon SETs is in order of megaohm. In order to control the SET resistance more effectively, extra gates can be utilized to tune the tunnel junction resistances. Toward this goal, dual recess structure was patterned on the silicon channel with two recess gates and a central dot gate. Recess gates can be utilized to control the SET resistance. Experiment results confirmed the SET resistance tunability using these recess gates. Interestingly, single-dot and strongly coupled multiple-dot characteristics were also observed in this structure when the oxidation time and recess dimensions were varied.

In this article, we report the measurement results of two different devices, which show a single-dot and multiple-dot characteristics, respectively. The single-dot characteristic, the device with short postlithography oxidation time, is ascribed to the formation of single dot in the central hump region. The multiple-dot characteristics in device with long postlithography oxidation time is attributed to the formation of a single dot in each recess due to the stress induced pattern-dependent oxidation (PADOX).[5] This structure can potentially be utilized as a candidate of strongly coupled quantum dots for the solid-state quantum bits. Multiple-dot characteristics device can also be operated as a unique SET with the tunnel junction resistance tunability using the recess gates. This unique property can be exploited to realize the tunable tunnel junction resistance SET for silicon rf-SET applications.

II. DEVICE FABRICATION AND DOT FORMATION MECHANISM

SOI wafer with the original SOI thickness of 100 nm and the buried-oxide (BOX) layer thickness of 200 nm was used to fabricate these devices. Initially, the substrate was thermal oxidized and phosphorus ion implanted (10^{19} cm^{-3}). After ion-implantation, drive-in process at the temperature of 1100 °C was conducted to activate the dopants. The implantation damage protective oxidize layer was removed after the

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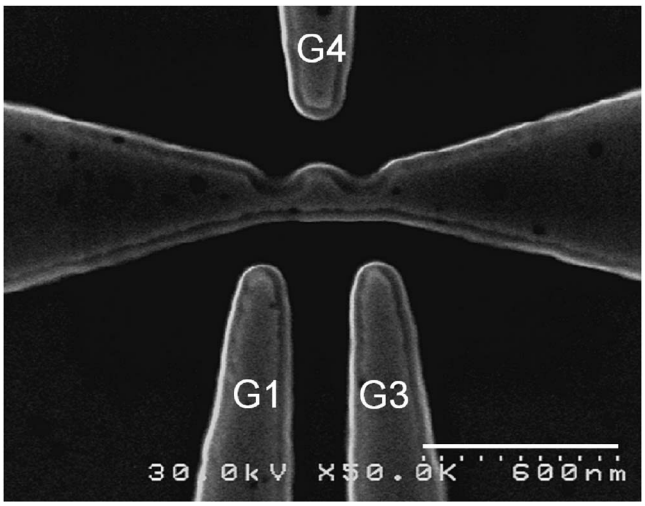

FIG. 1. SEM image of a typical fabricated recess structured silicon channel with PECVD deposited silicon dioxide.

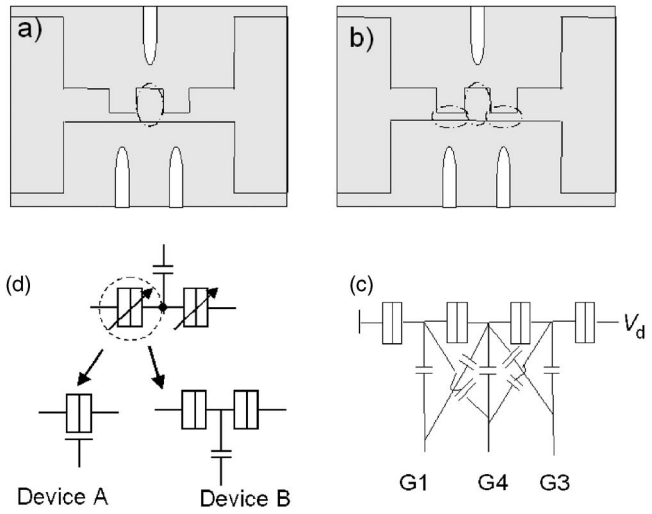

FIG. 2. Schematic diagrams for the possible location of (a) single-dot in device A (10 min oxidation) and (b) multiple-dot (dotted oval regions) in device B (25 min oxidation). (c) Simplified equivalent circuit of device B. (d) Schematic illustration of the evolution of individual recess into a single tunnel junction in device A and a single dot in device B.

drive-in process. The substrate was thermal oxidized again to reduce the thickness of the SOI to ~40 nm. Recess structure was patterned on the substrate using the high-resolution electron beam lithography. The electron cyclotron resonance-reactive ion etching was conducted to transfer the lithographically defined pattern to the SOI layer. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI. For device A, the lithographically defined recess length and width were 200 and 30 nm, respectively. The postlithography oxidation time was 10 min. For device B, the lithographically defined recess length and width were 150 and 30 nm, respectively. The postlithography oxidation time was 25 min (15 min longer than for device A). The lengths and widths of the central hump region were 100 nm for both the reported devices. Scanning electron microscopy (SEM) image of a typical fabricated recess structured SET is shown in Fig. 1. The bright regions indicate the SOI layer and the dark regions indicate the BOX layer of the substrate.

In device A with shorter postlithography oxidation, two recess regions evolved into tunnel junctions. This is caused by the lateral confinement of the channel in the recess areas, which gives rise to the bandgap enlargement. This naturally led to a single dot formation in the central hump region, as shown in Fig. 2(a). However, it is expected that longer oxidation conducted for device B converts two recess regions into the individual dots by means of PADOX process. A proposed effective potential model explains the tunnel barriers formation in PADOX device by considering the bandgap modulation due to the quantum confinement and the oxidation induced stress.[13] Tunnel barriers formation in device B is explained as follows. When the device is oxidized, narrow recess regions are immediately oxidized and surrounded by SiO_2. This leads to the compressive stress buildup[14] and consequent bandgap reduction in the narrow regions.[8] Furthermore, it is anticipated that shear stress caused by the difference in the oxidation rate between narrow recess regions and planer regions leads to lower compressive stress around the ends of recess regions.[8] A single potential barrier is introduced in each narrow recess regions due to the quantum size effect. As a combined result of quantum size caused potential barrier and stress induced bandgap reduction, a potential well is introduced at the center of each recess. This leads to double-tunnel-barrier potential formation in each recess region. Figures 2(b) and 2(c) illustrate locations of the formed multiple dots schematic diagram and the corresponding equivalent circuit, respectively. Owing to such extra dots formation, two recess channels with side gates in device B presumably work as two SETs, as depicted in Fig. 2(d). The PADOX dots formation reported for a cross-shaped silicon wire[6] supports our scenario of dots formation very well. In our device structures, the stress induced at the inner edge of the recess channel connected to the central dot is expected to be larger than that at the outer edge of the recess. The tunnel junction capacitances should, therefore, be larger at the inner edges than those at the outer ones should.

III. MEASUREMENT RESULTS AND DISCUSSION

SEM image of a typical fabricated dual recess structured silicon channel device is shown in Fig. 1. The recess gates G1 and G3 were used to control the potential distribution across the recess regions and the gate G4 was used to control the potential distribution across the central dot region. In this work, all the reported electrical measurements were performed at 4.2 K except the temperature variation measurement and the substrate was grounded throughout the measurements.

A. Demonstration of channel resistance tunability

The gates G1 and G3 can be employed to control the potential across the recess regions to control the SET resistance. The measurement results of the drain voltage sweep with different G1 and G3 voltages are shown Fig. 3 for one of the fabricated device. Total resistance of the device was calculated to be 914 kΩ for $V_{G1}=V_{G3}=0$ V, 695 kΩ for

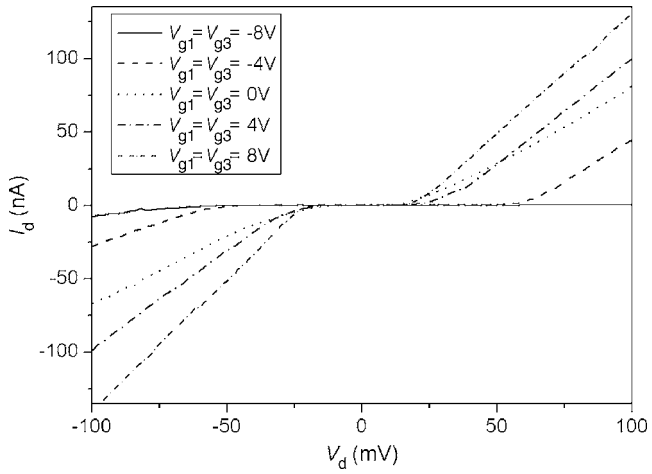

FIG. 3. Measured drain current versus drain voltage for the various voltages of V_{G1} and V_{G3} with $V_{G4}=0$ V at 4.2 K. Decrease in the device resistance due to the increase in the recess gates potential demonstrates the resistance controllability of the device.

$V_{G1}=V_{G3}=4$ V, and 618 kΩ for $V_{G1}=V_{G3}=8$ V. Total resistance of the device was calculated from the linear slope region of the I_{ds}-V_{ds} characteristics. Decrease in the device resistance with the increase in the recess gates voltage can be noticed from this measurement result. For negative gate voltages, the device resistance increased. This is clearly visible as the lower drain current for the gates voltages $V_{G1}=V_{G3}=-8$ V. It was also found that the decrease in the device resistance is small in PADOX based devices as well as for the values of recess gates voltage more than 10 V. This measurement results clearly indicate the ability to tune the device resistance by using the recess gates.

B. Single-dot SET measurement result

The contour plot of device A drain current (I_d) as a function of drain voltage (V_d) and gate G4 voltage (V_{G4}) is shown in Fig. 4 with other two gates kept grounded. A virtually uniform oscillation period manifests that a single charging dot is responsible for the Coulomb oscillation. Uniform Coulomb oscillation period was observed in the other two gates G3 and G4 Coulomb oscillation characteristics as well. This consistency of single oscillation period with all the three gates confirms the existence of a single dot in the channel. The contour plot of device A drain current as a function of V_{G1} and V_{G3} is shown in Fig. 5 for the gate G4 voltage of 0 V and drain voltage of 1 mV. The observed almost parallel current peak lines assure the existence of a single charging dot in the channel.

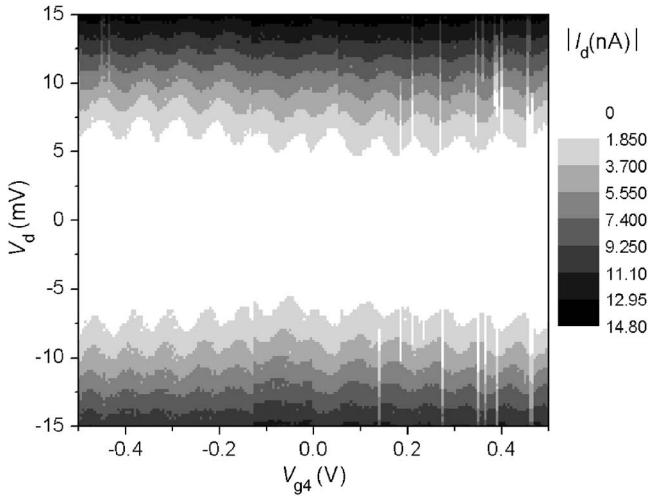

FIG. 4. Coulomb oscillation characteristics of device A for the gate G4 at 4.2 K. Gates G1 and G3 were grounded.

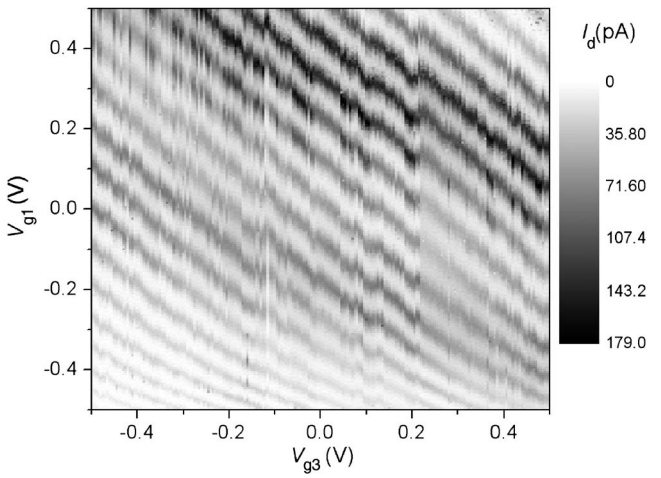

FIG. 5. Contour plot of the drain current as a function of V_{G1} and V_{G3} at 4.2 K of device A with $V_d=1$ mV and $V_{G4}=0$ V.

The gate capacitance C_G between each gate and the dot was evaluated from the conductance oscillation period ΔV_G, in the gate voltage according to $C=e/\Delta V_G$ for the individual gate sweep. The gate capacitances were extracted to be $C_{G1}=1.65$ aF, $C_{G3}=1.6$ aF, and $C_{G4}=1.95$ aF. As the gate G4 is nearer to the central dot, its capacitance is comparatively higher than the other two gates' capacitances. An almost same value of the recess gates capacitances indicates that the dot is located between the recess gates G1 and G3 symmetrically. Total dot capacitance, including three gates capacitances with tunnel junction capacitances, was extracted to be $C_{total}=25.06$ aF from the measured Coulomb blockade characteristics. If we assume the central dot to be a spherical in shape with a radius r embedded in a dielectric material, the capacitance is given by

$$C_{total}=4\pi\varepsilon_r\varepsilon_0 r, \tag{1}$$

where ε_r is the dielectric constant of the dielectric material. By substituting C_{total} and $\varepsilon_r=3.9$ for SiO_2, the dot diameter was calculated to be 115.5 nm. This dot diameter value is in good agreement with the lithographically defined dimensions of the region between the two recesses. From these data, it can be concluded that the formation a single dot as indicated in Fig. 2(a) in device A is responsible for the observed uniform Coulomb oscillation characteristics.

C. Strongly coupled multiple-dot SET measurement result

The measured gate G4 Coulomb oscillation characteristic of device B with the gates G1 and G3 grounded is shown in Fig. 6. From this contour plot, the presence of the Cou-

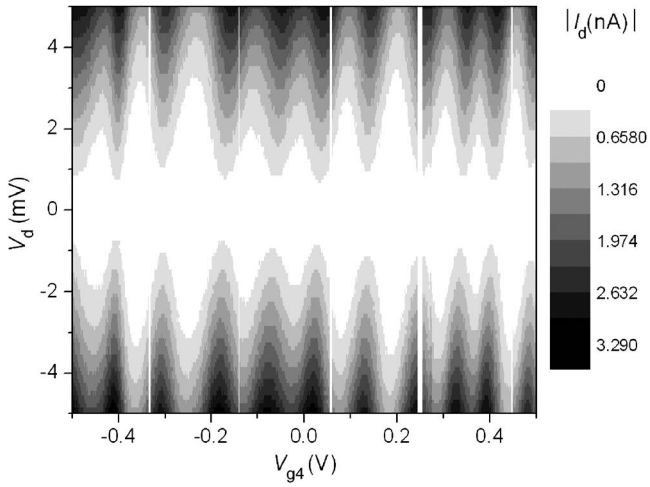

FIG. 6. Measured Coulomb oscillation characteristics of device B for the gate G4 at 4.2 K. Gates G1 and G3 were grounded.

lomb diamonds with the different Coulomb gaps can be noticed, indicating the existence of more than one charging dot in the channel. For the other two gates G1 and G3, clear Coulomb oscillations were observed with overlapping Coulomb diamonds. The consistency of overlapping diamonds for all three gates sweep over such a large gate voltage range confirms that this device contains more than one dot in the channel. The contour plot of device B measured drain current as a function of V_{G1} and V_{G3} is shown in Fig. 7(a) for the gate G4 voltage of 40 mV and drain voltage of 1 mV. In contrast to the results for device A (Fig. 5), clear anticrossing behaviors can be observed from this measurement result. If dots are coupled well, then conductance peak splitting will occur due to degeneracy in the energy parabolas of different dots where the electrons are no longer confined to individual dots.[15] Thus, the observed anticrossing characteristics indicate the strongly coupled nature of the dots present in the channel. This is attributed to the higher inner tunnel junctions capacitance as explained in Sec. II, which leads to the enhanced coupling[16] between the dots in the recesses.

To evaluate the effect of V_{G4} on the bias spectroscopy of V_{G1} and V_{G3}, the potential of the gate G4 was varied for the drain voltage of 1 mV. Figure 7(b) shows the variation of drain current as a function of V_{G3} for $V_{G1}=-0.2$ V [along the dotted line in the Fig. 7(a)] and the gate G4 voltage values of 40, 60, 80, 100, and 120 mV. Data are plotted with 400 pA offset for each V_{G4} voltage value for clarity. No extra conductance peak splitting for the different V_{G4} values was noticed in this measurement, which is clearly visible in this plot. Only a shift in the overall characteristics [as shown by the sloped dotted line in the Fig. 7(b)] was observed for other values of V_{G4} as well. Thus, stable conductance peak splitting characteristics with various V_{G4} values indicate the strongly coupled nature of the dots in the channel.

To evaluate the stability of device B transport characteristics, temperature variation measurements were carried out. The temperature dependence of device B drain current for the gate G1 voltages of $V_{G1}=-0.2$ V and $V_{G4}=0$ V is shown in Fig. 8. Increase in the drain current with the increase in temperature indicates that device is in classical Coulomb

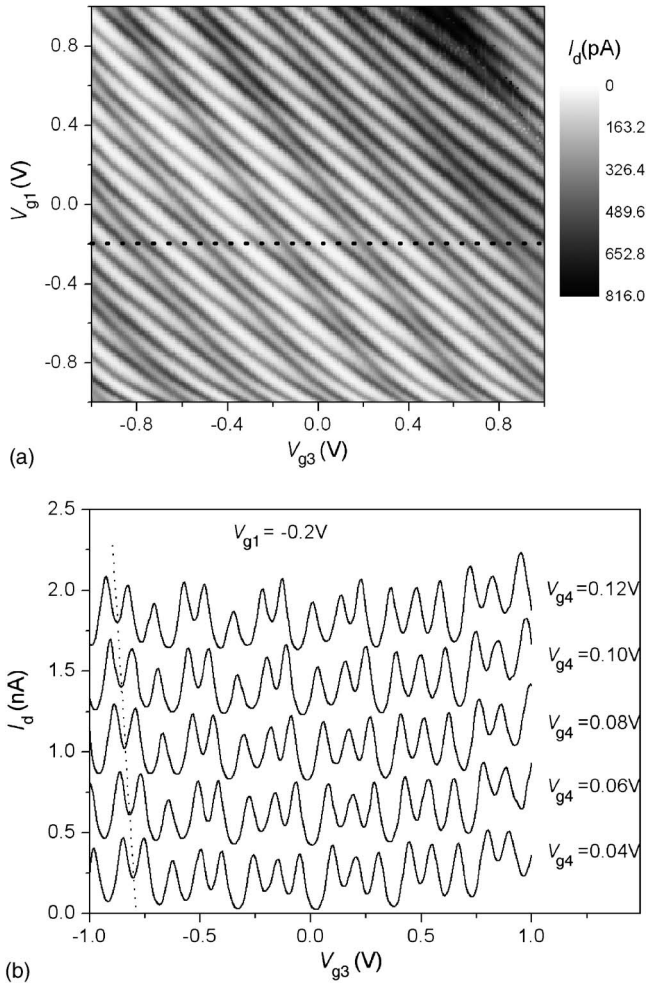

FIG. 7. (a) Measured drain current contour plot as a function of V_{G1} and V_{G3} at 4.2 K of device B. $V_d=1$ mV and $V_{g4}=40$ mV. (b) Drain current versus V_{G3} for various V_{G4} values at 4.2 K of device B along the dotted line shown in the Fig. 7(a), $V_d=1$ mV and $V_{g1}=-0.2$ V. Shift in the conductance peaks with V_{G4} is marked by the dotted line for the first peak splitting. Data were plotted with 400 pA drain current offset for the different V_{G4} voltages for clarity.

blockade regime.[17] This temperature variation measurement was done after two temperatures cycling to 20 and 4.2 K of the same sample with 1 month gap. During that period, the sample was kept at the room temperature and atmospheric pressure condition. It should be noticed that the drain current for the temperature of $T=4.5$ K was shown for the drain voltage value of 100 μV. For the temperature of 6 and 10 K measurements, drain voltage was kept at 1 mV. As shown by the vertical dotted lines in Fig. 8, conductance peak splitting positions have not been changed by the variation in drain voltage or temperature. Previously reported silicon nanowire result attributed the observed peak splitting to the additional tunnel barrier formation due to the dopant induced potential distribution.[18] However, the measurement characteristics of device B indicate that the dots characteristics are very stable, which is not possible in the case of the dopant-induced or surface roughness induced multiple dots in the doped silicon channel. From these measurement results, the observed multiple-dot characteristics in device B is attributed to the formation of a single dot in each recess due to the stress-

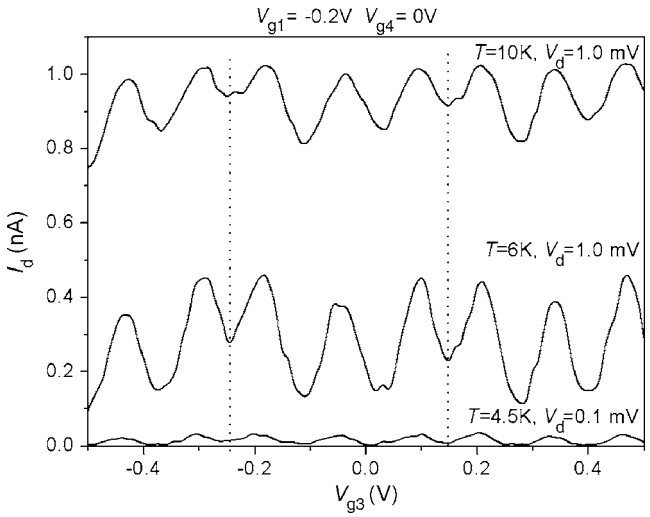

FIG. 8. Temperature depends of the drain current as a function of V_{G3} at 4.5 K (V_d=0.1 mV), 6 K (V_d=1 mV), and 10 K (V_d=1 mV) of device B [along the dotted line shown in the Fig. 7(a)] for V_{G1}=−0.2 V and V_{G4} =0 V during thermal cycle 3. Conductance characteristic (shown by dotted lines) is not affected by the different drain voltages or temperatures.

induced oxidation in the individual recess regions as a result of the narrower recess region and longer oxidation time. A schematic diagram in Fig. 2(b) illustrates locations of the formed multiple dots.

Figure 9 shows the gray scale plot of the simulated drain current as a function of V_{G1} and V_{G3} at 4.2 K, V_{G4}=0 V, and V_d=1 mV using the equivalent circuit shown in Fig. 2(d). In this simulation, symmetric outer and inner tunnel capacitances of 30 and 45 aF were used, respectively. Higher inner tunnel capacitances were utilized in the simulation in order to take the possible lower oxidation rate at the inner tunnel junctions into account. Direct capacitance of the gates G1 and G3 were extracted to be 0.264 and 0.585 aF from the measured drain current as a function of V_{G1} and V_{G3}. Although these capacitances still have to be optimized, the simulation result indicates that it is possible to observe the strongly coupled characteristics as per the proposed hypothesis of PADOX dots formation in dual recess structure. To

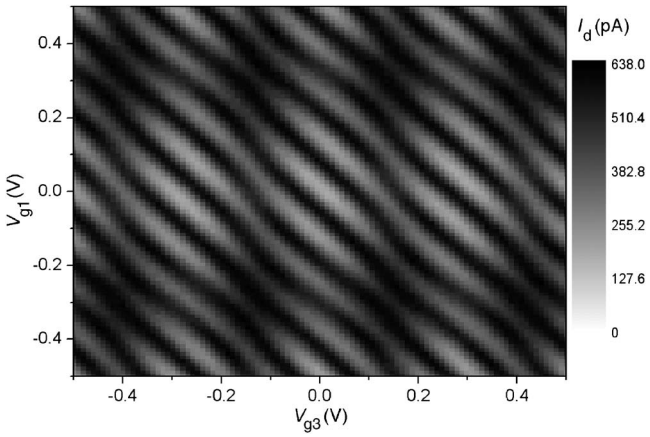

FIG. 9. Monte Carlo simulation drain current contour plot as a function V_{G1} and V_{G3} at 4.2 K, V_{G4}=0 V, and V_d=1 mV using the equivalent circuits shown in Fig. 2(c) with outer tunnel junction capacitances of 30 aF and inner tunnel junction capacitances of 45 aF.

confirm the repeatability of the observed strongly coupled characteristics in dual recess structured silicon channel, fabrication of the next set of devices was done with the same fabrication conditions. Clear anticrossing behaviors were observed in the second batch of devices as well.

In the multiple-dot characteristics device, the potential at each recess gate can be biased at a conductance maximum, and the gate G4 can be swept to realize tunable resistance SET, that is, device B can be considered as a unique SET with highly nonlinear tunable resistances. This operation can be explained as follows. From the drain current contour plot of the gates G1 and G3, conductance peak voltage values has to be chosen [peak position in Fig. 7(a)] and then the gate G4 voltage can be used to vary the central dot potential. The recess gates potential controls the conductance characteristics of the recess dots, which can be chosen to be at a resonance bias point. This operation is clearly visible in the Fig. 7(b), where for the fixed values of V_{G1} and V_{G3}, the drain current amplitude varies as a function of V_{G4} (along the V_{G4} variation in the vertical direction).

IV. CONCLUSION

Single-dot and strongly coupled multiple-dot characteristics were observed from the measured transport characteristics of dual recess structured highly doped silicon channel devices with different oxidation conditions. Single-dot characteristic is attributed to a dot formation in the central hump region due to the bandgap enlargement in the narrower recess regions, which naturally leads to the single dot formation in the central hump region. In the device with longer postlithography oxidation, formation of a dot in each recess is ascribed to the observed strongly coupled characteristics due to the stress-induced oxidation in the narrow recess regions. From the temperature variation and various gate potential measurements, it was shown that observed characteristics were not due to the dopant induced or surface roughness induced multiple dots. As the thermal oxidation is a very stable and controlled process, this recess structure can be utilized as a candidate of strongly coupled quantum dots for solid-state quantum bits. Unique nonlinear tunable resistance SET operation can be realized using this multiple-dot characteristics device.

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[1]M. H. Devoret and R. J. Schoelkopf, Nature (London) **406**, 1039 (2000).
[2]R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science **280**, 1238 (1998).
[3]Y. Ono, A. Fujiwara, K. Nishiguchi, H. Inokawa, and Y. Takahashi, J. Appl. Phys. **97**, 031101 (2005).
[4]G. Lientschnig, I. Weymann, and P. Hadley, Jpn. J. Appl. Phys., Part 1 **42**, 6467 (2003).
[5]Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwdate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Electron. Lett. **31**, 136 (1995).
[6]A. Fujiwara, Y. Takahashi, K. Murase, and M. Tabe, Appl. Phys. Lett. **67**, 2957 (1995).
[7]R. A. Smith and H. Ahmed, J. Appl. Phys. **81**, 2699 (1997).

[8]Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, Phys. Rev. E **19**, 95 (2003).
[9]Z. A. K. Durrani, Phys. Rev. E **17**, 572 (2003).
[10]A. Aassime, G. Johansson, G. Wendin, R. J. Schoelkopf, and P. Delsing, Phys. Rev. Lett. **86**, 3376 (2001).
[11]W. Lu, Z. Ji, L. Pfeiffer, K. W. West, and A. J. Rimberg, Nature (London) **423**, 422 (2003).
[12]M. Manoharan, H. Mizuta, and S. Oda, Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, 2006 (unpublished), p. 736.
[13]S. Horiguchi, M. Nagase, K. Shiraishi, H. Kageshima, Y. Takahashi, and K. Murase, Jpn. J. Appl. Phys., Part 2 **40**, L29 (2001).
[14]H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, Appl. Phys. Lett. **64**, 1383 (1994).
[15]F. R. Waugh, M. J. Berry, D. J. Mar, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Phys. Rev. Lett. **75**, 705 (1995).
[16]W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, Rev. Mod. Phys. **75**, 1 (2003).
[17]L. P. Kouwenhoven, C. M. Markus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, in *Mesoscopic Electron Transfer*, edited by L. Sohn, L. P. Kouwenhoven, and G. Schoen (Kluwer, Dordrecht, 1997), pp. 105–215.
[18]T. Altebaeumer and H. Ahmed, Jpn. J. Appl. Phys., Part 1 **42**, 414 (2003).