3-D Design and Analysis of Functional NEMS-gate MOSFETs and SETs

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***Abstract*—Nanoelectromechanical system (NEMS)-gate metal-oxide-semiconductor field effect transistor (MOSFET) and single-electron transistor (SET) structures are investigated by combining 3-D design and SPICE simulation. First, the metal gate is simulated by using a 3-D simulator, which enables to design realistic 3-D device structures, and its movement is studied for different design parameters. It is demonstrated that a low stiffness design of the structure is essential for a low-voltage actuation. Results are compared with theoretical numerical simulation and a tunable capacitor model is then embedded in a SPICE simulator and coupled either with a transistor model for MOS-NEMS or with a newly developed SET analytical model for SET-NEMS. It is shown that the use of NEMS membrane can add new functionalities to conventional MOSFET and SET, such as very abrupt switching of the current, which can break theoretical limits of MOSFET, or modulation of Coulomb oscillations governing SET characteristics.**

***Index Terms*—Analytical modeling, metal-oxide-semiconductor field effect transistor (MOSFET), movable gate, nanoelectromechanical system (NEMS), single-electron transistor (SET), 3-D modeling.**

I. Introduction

A. Hybrid Circuits Emergence

HYBRID circuits featuring single-electron transistors (SETs), metal-oxide-semiconductor field-electron-transistors (MOSFETs) and microelectromechanical systems/nanoelectromechanical systems (MEMS/NEMS) are getting increasing interest as very attractive candidates for future low-power and multifunctional nanoscale ICs. Introduction of nanoelectromechanical structures into conventional MOSFETs and SETs may provide superb performance and numerous new functionalities that are not achieved using present devices. In this way, a combination of MEMS and solid-state MOS transistor, which could act as a current switch or as a tunable capacitor, was investigated based on numerical simulation and analytical modeling [1], [2], and a very recent report experimentally demonstrated its virtues [3]. Another recent report also proposed a design combining a nanoscale movable gate and a transistor, which could lower the threshold voltage and enhance the drive current [4]. Similarly, it has also been suggested that variable NEMS capacitor could add new functionalities to conventional SETs such as tunable capacitance [5]. Therefore, the design of the movable gate is essential to achieve the performance predicted by the numerical simulation. However, it cannot be investigated in an efficient manner if not modeled in a 3-D context. In this work, we present different designs of movable electrodes and report expected results based on 3-D calculation and analytical modeling for both MOS-NEMS and SET-NEMS architectures.

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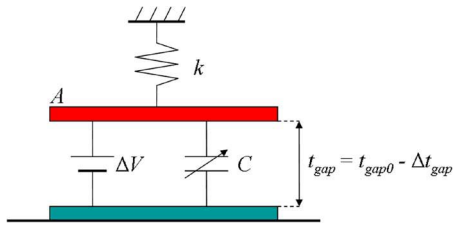

Fig. 1. Schematic of a conventional metal–metal capacitor.

B. NEMS-Gate Devices Principle

The NEMS-gate devices operation is based on the principle of the conventional metal–metal capacitor, i.e., a movable top plate suspended by hinges over a fixed bottom plate, as it is depicted in Fig. 1. By applying a voltage across these two plates, the suspended plate starts to continuously move downwards under the influence of the attractive electrostatic force which is in equilibrium with the elastic force

$$\sum F_{ext} = \frac{\epsilon_0 A \Delta V^2}{2(t_{\mathrm{gap0}} - \Delta t_{\mathrm{gap}})^2} - k\Delta t_{\mathrm{gap}} = 0 \qquad (1)$$

where Δt_{gap} is the plate displacement, t_{gap0} the initial air-gap, A the overlap area, and ΔV the applied voltage between the plates.

Thus, as the top plate deflects vertically, that is as Δt_{gap} increases, the capacitance increases according to

$$C = \frac{\epsilon_0 A}{t_{\mathrm{gap0}} - \Delta t_{\mathrm{gap}}}. \qquad (2)$$

If Δt_{gap} is increased to more than $t_{\mathrm{gap0}}/3$, the equilibrium is broken because of the overwhelming electrostatic force,

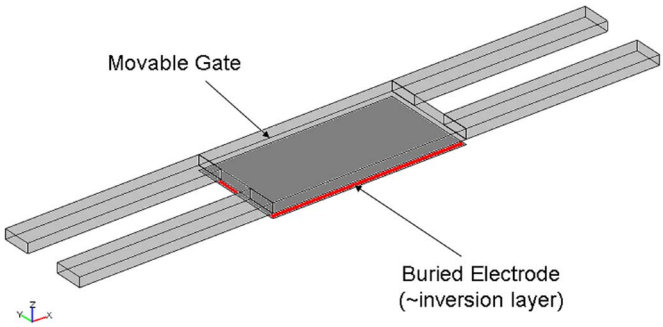

Fig. 2. 3-D simulation of a MOS-NEMS membrane with COMSOL [6].

resulting in the snap of the two plates, the theoretical pull-in voltage being

$$V_{PI} = \sqrt{\frac{8kt_{\text{gap0}}^3}{27\epsilon_0 A}}. \tag{3}$$

II. MOSFETS With a NEMS-Gate

MOS-NEMS devices combine a MOS transistor and a metal membrane suspended over its channel. One of the unique characteristics of these devices is their superexponential dependence of the inversion charge Q_{inv} versus the gate voltage V_g in the subthreshold region, resulting of the ultra-abrupt movement of the metal membrane. Such devices are expected to break theoretical limits of the solid-state MOSFET such as its subthreshold slope ideal limit of 60 mV/decade. Furthermore, as well as abrupt current switch, applications as molecular or high sensitive DNA sensors are imaginable.

A. 3-D Modeling

The model used to perform 3-D simulation in the Comsol software [6] is depicted in Fig. 2. The gate is made of aluminium and is anchored by four arms on either side of the channel. Each arm is 20 μm long and 3 μm large. The inversion layer, which plays the role of the bottom plate of the conventional capacitor switch, is modeled by a simple closed polyline inside of which a constant potential is applied, and has the same area as the metal membrane does.

Fig. 3 shows the movement of the gate electrode for various device parameters: initial air gap, gate area, and gate thickness. It is important to note that since COMSOL does not perform contact analysis, the simulation is stopped just before the pull-in effect occurs. As expected by the theoretical formula (3), the pull-in voltage decreases as the initial air-gap and the gate thickness decrease, and as the gate area increases. One can notably notice that the gate thickness has a very important effect on the membrane behavior. This result cannot be quantitatively provided by the 2-D theoretical model because the spring constant k is supposed to represent both the hinges design and the gate stiffness at the same time. It suggests that to achieve

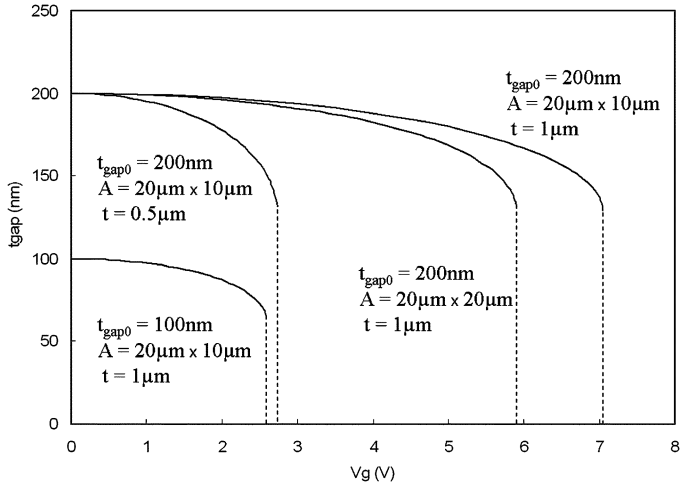

Fig. 3. MOS-NEMS membrane actuation for various parameters: initial air-gap t_{gap0}, area A, thickness t.

a low enough pull-in voltage, it may be more efficient to lower the global stiffness of the structure (e.g., by designing appropriate hinges or by decreasing the gate thickness), rather than increasing the gate area, which would be conveyed by space waste and gate leakage.

B. Implementation in a Circuit Simulation

Electric behavior of the MOS-NEMS device can then be studied by embedding these results in professional simulator SmartSpice [7] by using its Verilog-A interface that allows us to describe one's own model. The device is divided in two parts: the NEMS part, which describes the movable gate behavior, and the MOS part, which describes the electrical characteristics of the transistor itself.

However, 3-D calculated results are not significant as things are in the MOS-NEMS case, since the potential of the inversion layer is considered as constant in this simulation, whereas in reality, the capacitive divider created by the air-gap and the channel oxide means the inversion layer has a feedback on the gate movement according to the following equation:

$$V_{gint} = \frac{V_g}{1 + \frac{C_{gc}}{C_{\text{gap}}}} \tag{4}$$

where V_g and V_{gint} are, respectively, the gate voltage and the intrinsic gate voltage, and C_{gc} and C_{gap} are the gate-to-channel capacitance and the air-gap capacitance. This effect results in an increase in the pull-in voltage.

Nevertheless, 3-D calculated results are used to reflect the mechanical behavior of the gate. One can indeed calculate from these results an equivalent spring constant k that will take into account not only the hinges design but also the structure stiffness, and embed this constant k in the theoretical 2-D model already mentioned. 3-D dependence of the equivalent spring constant is shown in Fig. 4. Fig. 5 shows how the theoretical model using the equivalent spring constant k fits to the 3-D calculated

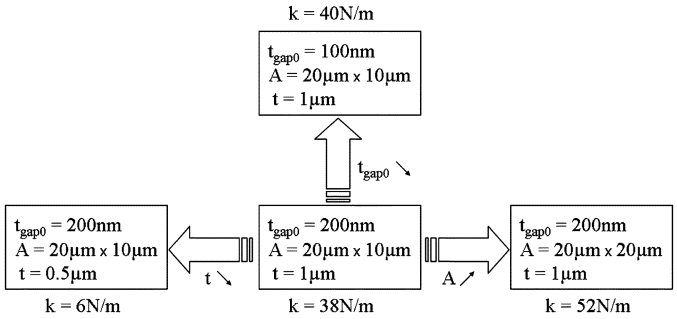

Fig. 4. 3-D dependence of the equivalent spring constant k with initial air-gap t_{gap0}, area A, and thickness t.

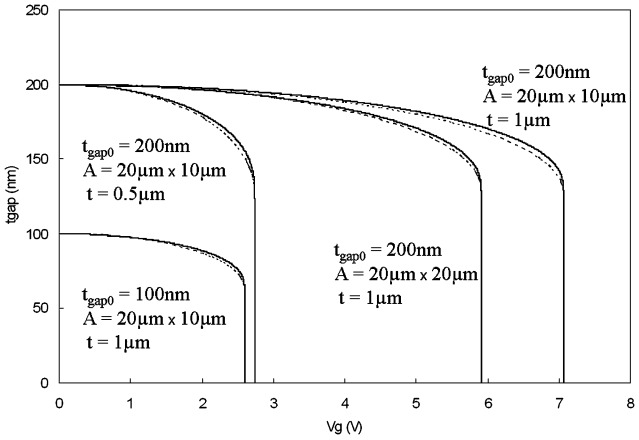

Fig. 5. Reproduction of the theoretical model using the equivalent spring constant (solid line) with the initial 3-D simulated results (dotted line).

results. The reproduction is quite good because the gate design is very similar to the theoretical parallel-plate model.

Finally, the continuous expression of the gate-to-channel capacitance proposed in [1] is also used

$$C_{gc} = \frac{\frac{\sqrt{2}}{2}\frac{\eta-1}{\eta}\exp\left(\frac{V_{gint}-V_T}{\eta V_{th}}\right)C_{ox}}{\frac{\sqrt{2}}{2}\frac{\eta-1}{\eta}\exp\left(\frac{V_{gint}-V_T}{\eta V_{th}}\right)+1} \tag{5}$$

where $\eta = 1 + C_d/C_{ox}$, C_{ox}, and C_d, respectively, the oxide and depletion capacitance, V_T the intrisic threshold voltage, and V_{th} the thermal voltage.

Concerning the MOS part, BSIM model [8], available in SmartSpice library, is used to describe the electrical characteristics of the transistor. Note that the oxide thickness is supposed to be equal to 40 nm.

The two parts are then combined in an usual SPICE netlist, and the simulation is performed at low drain voltage ($V_D = 50\ \mathrm{mV}$).

Fig. 6 shows that the abrupt movement of the gate results in a switching of the MOSFET drain current. This suggests that the steepest transition between on and off states of a conventional MOSFET (60 mV/decade) can be improved by the use of the NEMS-gate. However, it is important to note that the experimentally observed transition may strongly differ from the one depicted in the figures since the SPICE electrical simulation does not take into account the mechanical limitations inherent

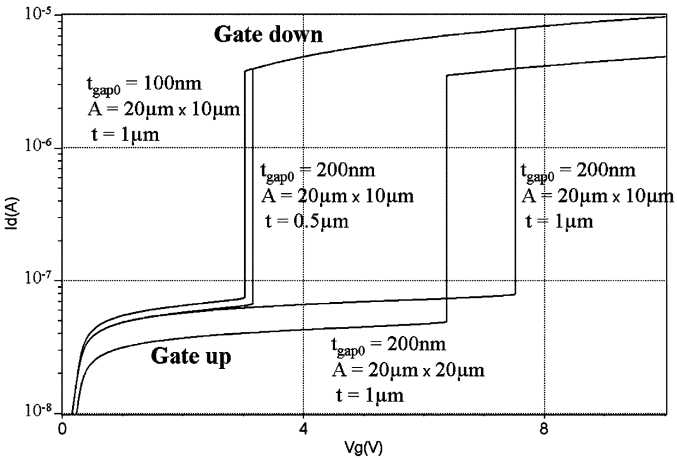

Fig. 6. MOS-NEMS drain current I_D versus gate voltage V_G (in log-lin scale) at low drain voltage $V_D = 50\ \mathrm{mV}$ for different structures.

to the displacement of the metal gate. As already mentioned, the 3-D simulation is stopped just before the pull-in effect occurs, preventing us to investigate the speed of the gate movement. Nevertheless, according to simple mechanical considerations, we can easily affirm that the lower the stiffness of the structure, the speediest the switching and as already told, the lower the pull-in voltage. Thus, it is essential to achieve a structure as supple as possible for switching application. Another handicap is the friction due to the air-gap between the gate and the channel. One possible solution is to operate the device in vacuum.

III. Single-Electron Transistors With a NEMS-Gate

The concept of a movable gate can be extended to the case of the SET, as it was suggested in [5]. By tuning the gate capacitance of the SET, one can change the total island capacitance and, hence, control the periodicity and the level of the current. NEMS-gate architectures could also enrich conventional SETs with new functionalities such as threshold gate behavior or abrupt current switching, and in a general manner, further control of the device's behavior.

A. Set Analytical Model

Simulation of hybrid circuits featuring SETs in a SPICE environment is fairly difficult because of the electrical characteristics of SET that result from the Coulomb blockade phenomenon. Accurate but time-consuming Monte Carlo simulations are not adapted to design realistic circuits featuring a large number of components. Therefore, accurate SET analytical models are required to allow faster simulations. We propose a physically based compact SET analytical model for hybrid simulation. This model is based on the "orthodox" theory of single charge tunneling and the master equation method [10], [11]. The model is verified against the simulated data from Monte Carlo simulator CAMSET [9]. It describes accurately SET characteristics for a wide range of drain to source voltages ($|V_{DS}| < 4e/C_\Sigma$, where C_Σ is the total island capacitance) and temperatures ($T < e^2/(10k_BC_\Sigma)$). The proposed model can also take the background charges effect into account. Fig. 7 shows the accuracy of our model for different values of drain

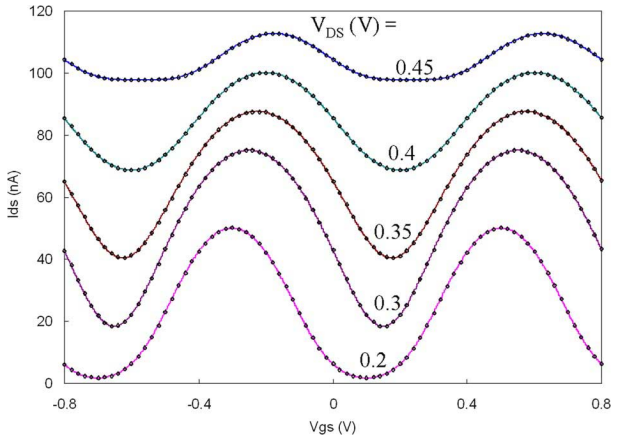

Fig. 7. $I_{DS} - V_{GS}$ verification of our model for symmetric device with $C_G = 0.2$ aF, $C_D = C_S = 0.15$ aF, and $R_D = R_S = 1\ \mathrm{M}\Omega$ at $T = 173$ K. Here, the dotted line represents master equation simulation (CAMSET) [9] and solid line represents our model.

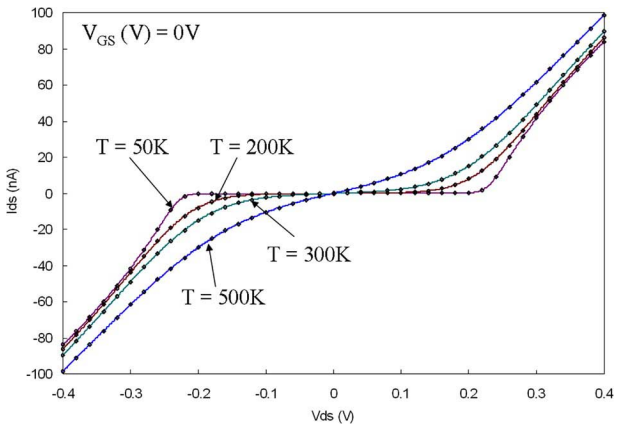

Fig. 8. $I_{DS} - V_{DS}$ verification of our model at different temperature levels for symmetric device with $C_G = 2$ aF, $C_D = C_S = 1$ aF, and $R_D = R_S = 1\ \mathrm{M}\Omega$. Here, the dotted line represents master equation simulation (CAMSET) [9] and solid line represents our model.

to source voltages. Fig. 8 shows several drain currents I_{DS} obtained at different temperature levels (from 50 to 500 K), with $V_{GS} = 0$ V and without background charge. Impact of temperature on the Coulomb blockade can be clearly seen: it disappears when the temperature increases. It can be noted that our model is in perfect accordance with CAMSET simulation. Actually, the domain of validity of our model does not depend on the temperature (until 500 K). We also verified it for several capacitances values, and the same performances were observed. Our model has been validated until $T < e^2/(10k_BC_\Sigma)$. To the best of our knowledge, the best analytical model reported until now is the MIB model [5] which is valid for $|V_{DS}| < 3e/C_\Sigma$ but only for low temperatures $T < e^2/(40k_BC_\Sigma)$.

B. 3-D Modeling

Fig. 9 shows the beam structure used to simulate the gate. It is made of aluminium and is suspended over the substrate. A nanowire SET (70 nm $\times 2\ \mu$m) is designed under the beam, but for simplification, its potential is considered as constant. It is worth noting that, contrary to the case of MOS-NEMS, the

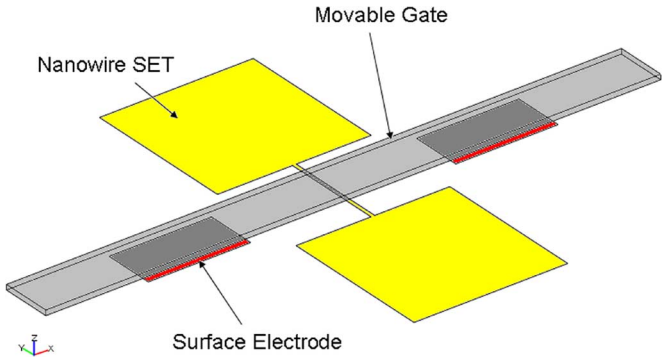

Fig. 9. 3-D simulation of a SET-NEMS beam with COMSOL [6].

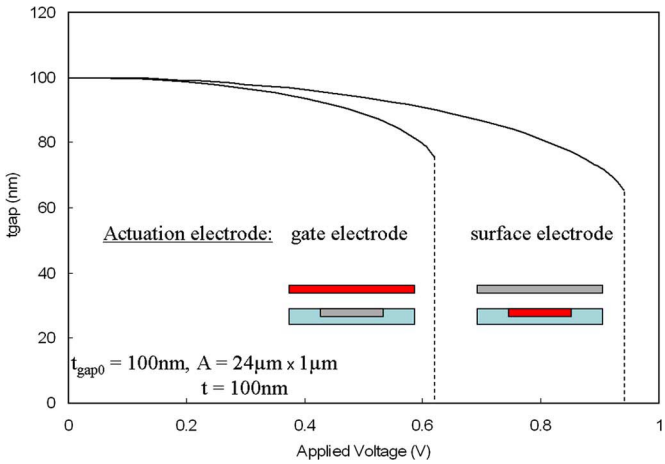

Fig. 10. SET-NEMS gate actuation according to the actuated electrode.

two facing actuation electrodes, i.e., the gate electrode and the buried electrode, do not have the same area. Because of this dissymmetry, the gate behavior will be different according to the electrode which is chosen as actuation electrode, as shown in Fig. 10. It can be assumed that a lower pull-in voltage is needed when the movable gate is actuated because of its wider area which contributes more to the electrostatic force. Fig. 11 shows electrostatic actuations for different parameters: initial air-gap, gate length, gate thickness, and gate material (one layer Al, or two layers Al/SiO_2). As predicted by the theoretical formula (3), the pull-in voltage decreased as the initial air-gap or the thickness decreases and as the length increases. It is worth noting that the equilibrium region can be extended beyond the theoretical $t_{\mathrm{gap0}}/3$ value by the use of a SiO_2 layer underneath a thin conductive layer (in this case, a 50-nm-thin aluminium layer), to the price of a substantial increase in the pull-in voltage, due to the in-series connection of the oxide and gap capacitances.

Another studied structure, similar to the one originally proposed in [12], is depicted in Fig. 12. In order to compare with the previous beam structure, hinge width is taken as half of the beam width, so that the contribution of the hinges to the stiffness of the structure remains approximately the same as in the case of the beam. The total overlap area is then doubled or quadrupled, and the simulation is performed by actuating the buried electrode, the movable gate remaining grounded. Results are shown in Fig. 13. It is interesting to notice that in this case, the pull-in voltage decreases in a quasi-inversely proportional manner with

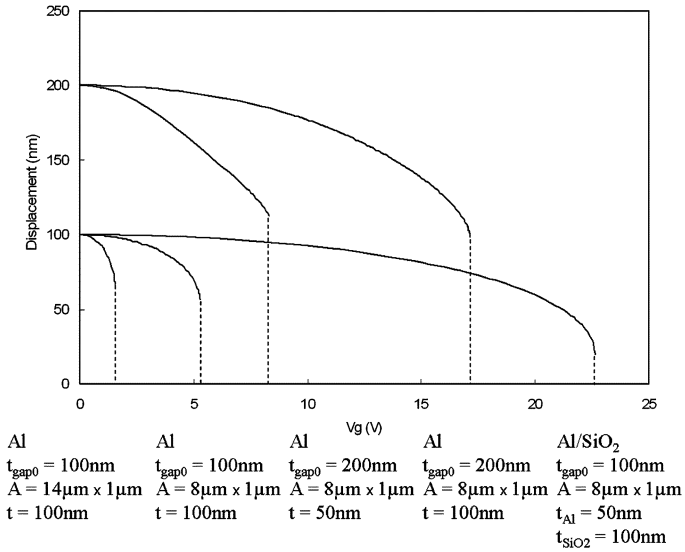

Fig. 11. SET-NEMS gate actuation for various parameters: initial air-gap t_{gap0}, gate area A, thickness t, and material.

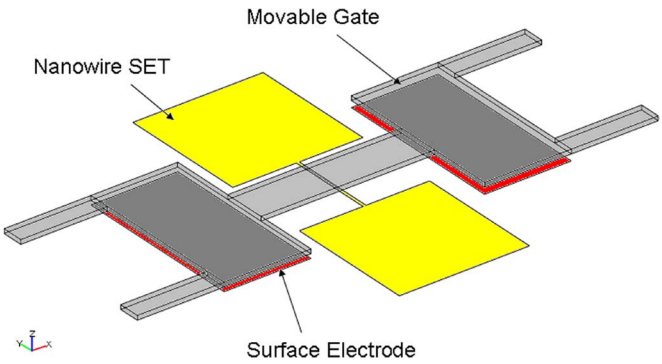

Fig. 12. 3-D simulation of a SET-NEMS movable gate with COMSOL [6].

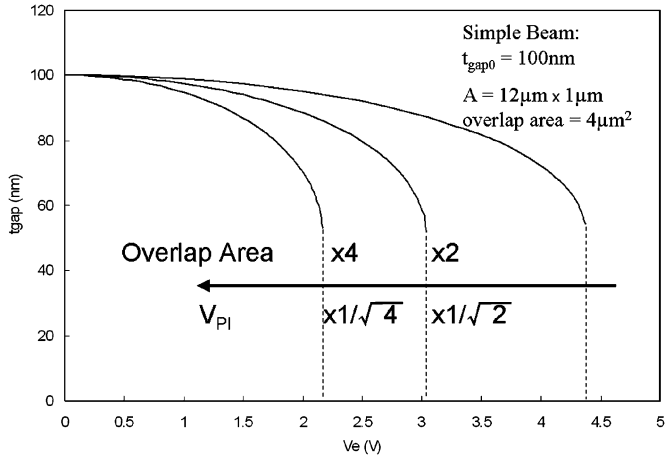

Fig. 13. SET-NEMS gate actuation for different overlap areas.

the square root of the gate area, as suggested by the theoretical formula (3), even though the design of the structure differs from the parallel-plate theory. It can be assumed that the surface of the gate not *vis-a-vis* the buried electrode (i.e., the bridge and the hinges) has only little influence on the evolution when increasing the area in this manner. Moreover, it also suggests that an unreasonable increase in area is not efficient to achieve

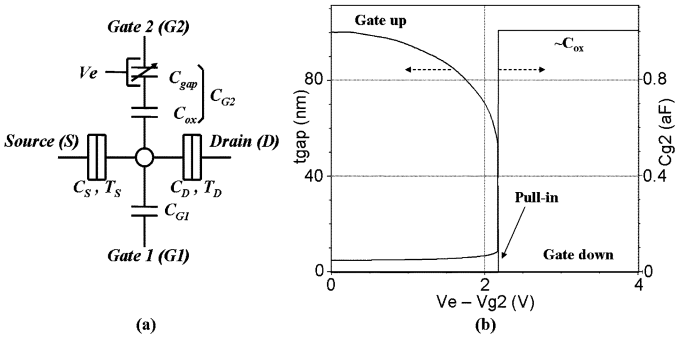

Fig. 14. (a) Electrical equivalent circuit of SET-NEMS device. (b) Displacement of the movable gate $(G2)$ (left axis) and corresponding capacitance C_{G2} (right axis) versus actuation voltage $V_e - V_{G2}$.

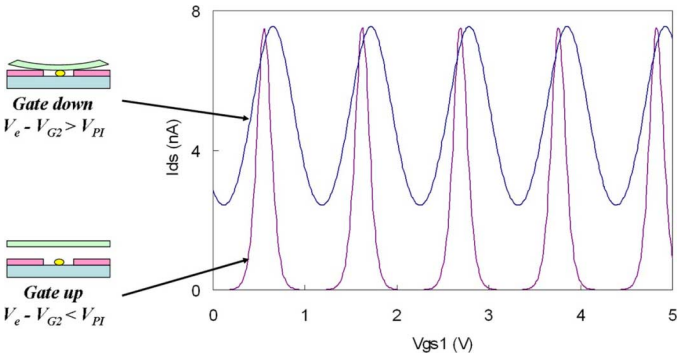

Fig. 15. SET-NEMS drain to source current I_{DS} versus gate 1 voltage V_{G1}. SET device parameters are $C_{G1} = 0.15$ aF, $C_D = C_S = 0.1$ aF and $R_D = R_S = 1\ \mathrm{M}\Omega$, $V_{G2} = 0$ V, $V_{DS} = 0.03$ V at $T = 173$ K.

a pull-in voltage less than ≤ 1 V, since an area of 80 $\mu\mathrm{m}^2$, i.e., 20 times larger than the initial one, would be needed in this configuration.

C. Implementation in a Circuit Simulation

Electrical behavior of the device is then investigated by coupling the 3-D calculated results and the proposed analytical model in SmartSpice. The device corresponding to the electrical equivalent circuit depicted in Fig. 14(a) is studied. It possesses two gates: a buried gate $(G1)$, that acts as a normal gate, and a movable gate $(G2)$, which is the one depicted in Fig. 12. This gate has a total overlap area of 16 $\mu\mathrm{m}^2$ with the buried electrode (E) and enables it to tune the total island capacitance of the SET. Its displacement is modeled by using an empirical polynomial and embedded thanks to Verilog-A. The displacement of the gate and the corresponding capacitance C_{G2} is shown in Fig. 14(b). C_{G2} is simply calculated as equal to the in-series connection of C_{gap} and C_{ox}, respectively, corresponding to the air-gap capacitance and to the oxide capacitance of a supposed 20-nm-thin layer covering the region underneath the movable gate.

As shown in Figs. 15 and 16, the drain current oscillations can be modulated either in periodicity or in level by switching the gate. When considering the evolution of the drain current versus the buried gate $(G1)$ voltage, only the level of the drain current is changed when the gate is switched as depicted in Fig. 15, the periodicity of the oscillations remains the same. This is due to

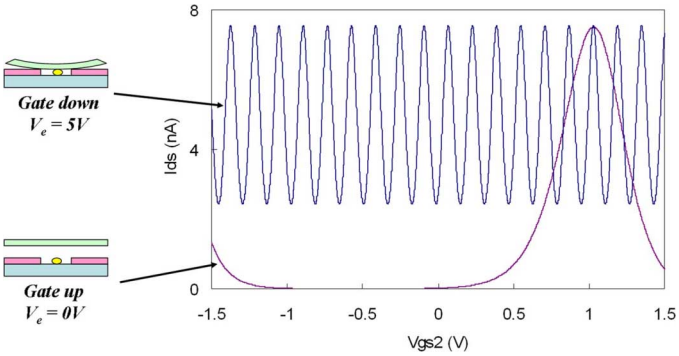

Fig. 16. SET-NEMS drain to source current I_{DS} versus gate 2 voltage, V_{G2}. SET device parameters are $C_{G1} = 0.15$ aF, $C_D = C_S = 0.1$ aF and $R_D = R_S = 1\ \mathrm{M\Omega}$, $V_{GS} = 0.2$ V at $T = 173$ K.

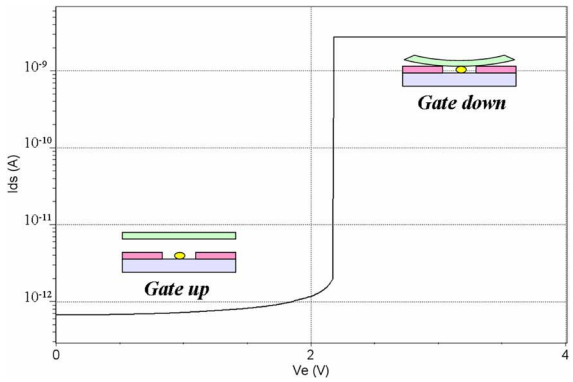

Fig. 17. SET-NEMS drain to source current I_{DS} versus buried electrode voltage V_e (in log-lin scale). SET device parameters are $C_{G1} = 0.15$ aF, $C_D = C_S = 0.1$ aF and $R_D = R_S = 1\ \mathrm{M\Omega}$, $V_{G1} = 0.03$ V, $V_{G2} = 0$ V, $V_{DS} = 0.03$ V at $T = 173$ K.

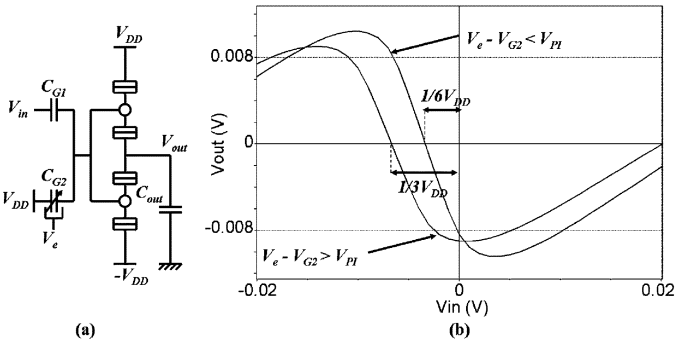

Fig. 18. (a) Schematic of a SET-NEMS inverter whose inversion threshold can be switched between two values. (b) Switching of the inversion threshold. Here, parameters of SET devices are $C_{G1} = 3$ aF, $C_D = C_S = 1$ aF and $R_D = R_S = 1\ \mathrm{M\Omega}$, C_{G2} can be switched between 0.5 aF and 1 aF (i.e., $1/6C_{G1}$ and $1/3C_{G1}$), $V_{DD} = 0.02$ V, $C_{out2} = 1$ fF at $T = 10$ K.

the fact that the period is equal to e/C_{G1} in this case. However, if the movable gate $(G2)$ is activated, the periodicity of the oscillations, then equal to e/C_{G2}, can be switched between two different values. Such periodicity encoding of the current could be used in a communication system to get rid of the unwanted background charge effect. Another interesting feature of this device is that the current level can also be controlled as shown in Fig. 17, so that the device can also be used as a current switch when the electrode (E) is actuated. However, the current capability remains low, inherently to the SET characteristics.

Design of logic circuits of a new type could also be thought up. For example, threshold voltage adjustable inverters can be designed, as shown in Fig. 18(a). According to the voltage applied to the buried electrode (E), the capacitance C_{G2} can be switched between two values, $1/6C_{G1}$ and $1/3C_{G1}$, so that the inversion threshold of the inverter consequently switches between $-1/6V_{DD}$ and $-1/3V_{DD}$ [Fig. 18(b)]. Generally, SET-NEMS could be integrated in multifunctional neuron cells able to involve only very few devices, and neural networks inheriting at the same time the SET ultra-low power consumption.

IV. Conclusion

We have studied both NEMS-gate MOSFET and SET structures by combining 3-D design and a newly developed SET analytical model. Our hybrid simulation has enabled us to investigate new functionalities that could be added to conventional MOSFET and SET such as very abrupt current switching, and in a general manner further control of the device's behavior.

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