Japanese Journal of Applied Physics
Vol. 46, No. 7A, 2007, pp. 4386–4389

Integration of Tunnel-Coupled Double Nanocrystalline Silicon Quantum Dots with a Multiple-Gate Single-Electron Transistor

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(Received January 22, 2007; accepted April 7, 2007; published online July 4, 2007)

We report on integration of double nanocrystalline silicon quantum dots (nc-Si QDs) of approximately 10 nm in diameter onto the multiple-gate single-electron transistor (SET) used as a highly-sensitive charge polarization detector. The SET with a single charging island is first patterned lithographically on silicon-on-insulator, and the multiple-gate bias dependence of the Coulomb current oscillation is characterized at 4.2 K. The coupling capacitance parameters between the SET charging island and the multiple-gate are estimated and compared with those obtained by using the three-dimensional capacitance simulation. Double nc-Si QDs are then deposited in the immediate vicinity of the charging island of the SET by using the very-high frequency plasma deposition technique. We perform the single-electron circuit simulations and demonstrate that only $\pm e$ charge polarization of the double QDs can be sensed as a shift of the Coulomb oscillation peaks.
[DOI: 10.1143/JJAP.46.4386]

KEYWORDS: double quantum dots, nanocrystalline-silicon quantum dots, qubit, three-dimensional capacitance simulation, single-electron transistor

1. Introduction

The double quantum dots (DQD) structure has recently been studied as a charge qubit to realize the solid-state quantum computer. DQDs have been fabricated in GaAs:AlGaAs heterostructures, where DQDs are realized through the depletion of a two-dimensional electron gas using surface gates.[1)] In these devices large numbers of surface gates are used to define the QDs and the barriers, which lead to shallow potentials confinement and cross capacitance problems. DQDs have also been fabricated in the Si-based materials by using the electron beam lithography and the reactive ion etching (RIE) techniques, which results in a "trench-isolated" structure.[2,3)] Charge polarizations in the DQDs are measured using a single-electron transistor (SET). The theoretical limit of charge sensitivity for a SET is about $1 \times 10^{-6}\, e\mathrm{Hz}^{-1/2}$.[4)] This ultra high charge sensitivity property makes the possibility of detecting the quite small changes in the distribution of charge within a capacitively-coupled structure.

To realize the practical quantum computer, computation steps (= decoherence time/coherent period) must be increased at least by 10^4 times. To meet this computational requirement, increasing the decoherence time and the coherent oscillation frequency is the necessary condition. One of the solutions is using the smaller sized quantum dots which show enhanced quantum effect. In the present work, we succeeded in integrating the lithographically patterned SET and nanocrystalline-Si quantum dots (nc-Si QDs). The nc-Si QDs are fabricated by the pulsed-gas very-high-frequency (VHF) plasma process and approximately 10 nm in size, spherical in shape, and highly pure in nature.[5–7)] These unique properties will help to realize the long decoherence time charge qubits. Integration of nc-Si QDs with patterned substrate has been carried out by atomic force microscope (AFM) or dots solution techniques.[8,9)] But position control for all dots using AFM technique is laborious work. The nc-Si QDs assembly technique has recently been applied for the pre-patterned nanostructures, but position control of individual nc-Si QDs is not realized yet. In this work we report *in-situ* deposition technique to locate double nc-Si QDs in a nanoscale window patterned in the immediate vicinity of the SET charging island by using high-resolution electron beam lithography. We carried out the differential current measurement to estimate the capacitance coupling parameters and compared them with three-dimensional capacitance simulations. To investigate the effects of the charge polarizations on the SET characteristics, we performed the equivalent circuit simulation.

2. SET Fabrication

SETs were fabricated using separation by implantation of oxygen (SIMOX) silicon substrates with initial silicon-on-insulator (SOI) thickness of 100 nm and buried-oxide (BOX) thickness of 200 nm. Negative resist RD-2000N was used for electron-beam (EB) direct writing. Although primarily developed as a deep ultraviolet resist, RD-2000N shows good sensitivity to EB exposure.[10)] This resist offers good etching resistance and simple resist handling. The initial SOI layer thickness was reduced to 40 nm by repeated thermal oxidation and wet etching. The fabricated SET is structured with single dot and four side gates. The schematic top-view of the SET is shown in Fig. 1. The top colored regions indicate SOI with phosphorus doping level at $10^{19}\,\mathrm{cm}^{-3}$, the bottom colored region indicates silicon substrate with boron doping of $10^{15}\,\mathrm{cm}^{-3}$, and the white region indicates the BOX layer, where the SOI regions has been etched away using the electron cyclotron resonance RIE (ECR-RIE) technique.

The fabrication process is as follows. At first 60 nm thickness of negative resist RD-2000N was coated on the SOI layer and single dot structured SET (Fig. 1) was patterned using the high-resolution electron beam lithography with a lithographically defined diameter of approximately 90 nm for the island. The adjacent constrictions that act as tunnel barriers connecting the charging island to the source and drain electrodes are of 70 nm in width. The pattern was etched using ECR-RIE technique and was

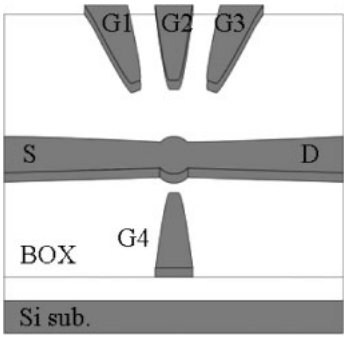

Fig. 1. (a) Schematic top-view of the lithographically fabricated single dot structured SET with four gates.

thermally oxidized at 1000 °C to passivate the surface states and reduce the effective thickness of the SOI down to approximately 30 nm. This final oxidation leads to resulting overall dot diameter of approximately 70 nm.

3. Measurements and Three-Dimensional Capacitances Simulation

To characterize the fabricated SET, electrical measurements were carried out at the temperature of 4.2 K. The gate voltage dependence of the device was obtained by sweeping the V_{G4} at the differential values of V_{G1}, V_{G2}, and V_{G3} as shown in the Figs. 2(a), 2(b), and 2(c) respectively. These plots show the measured differential conductance through the SET $\partial I_D/\partial V_{G4}$. In these measurements, drain to source bias voltage was kept at 1 mV. The coupling capacitances between G1, G2, G3, and G4, and the SET island extracted from the differential conductance characteristics are $C_{G1} = 0.27\,\mathrm{aF}$, $C_{G2} = 0.38\,\mathrm{aF}$, $C_{G3} = 0.33\,\mathrm{aF}$, and $C_{G4} = 1.0\,\mathrm{aF}$, respectively. The total capacitance of the island is estimated to be $C_{\sum} \approx 16\,\mathrm{aF}$ from the measured coulomb blockade voltage $V_{gap} \approx 10\,\mathrm{mV}$.

In order to demonstrate the correctness of the extracted gate capacitances values which were obtained from the measurement characteristics, three dimensional capacitance simulations was performed. In the simulation, electric field distribution in the three-dimensional structure is calculated by solving the three-dimensional Poisson's equations for the applied electric potential to the electrodes and electric charge distribution in the device with the specified boundary conditions. From this potential distribution, the capacitance matrix is estimated by computing the electric flux flowing into the SET island. Figure 3 shows the simulated potential distributions in the device for the applied 1 V to the gates G1, G2, and G4 respectively. The simulated capacitance values between the gates and island are found to be $C_{G1} = 0.30613\,\mathrm{aF}$, $C_{G2} = 0.41108\,\mathrm{aF}$, $C_{G3} = 0.30613\,\mathrm{aF}$, and $C_{G4} = 0.97107\,\mathrm{aF}$. It is found that these simulated capacitance values agree with the extracted capacitances from the measurements. This capacitance agreement confirms the geometrical defined nature of the fabricated SET.

4. Integration of nc-Si QDs with the SET

Fabrication equipment of the nc-Si QD consists of a VHF plasma cell and an ultrahigh-vacuum (UHV) chamber. The nc-Si QD with a diameter of ~10 nm is formed in the gas phase of a SiH_4 plasma cell by the decomposition of pulsed

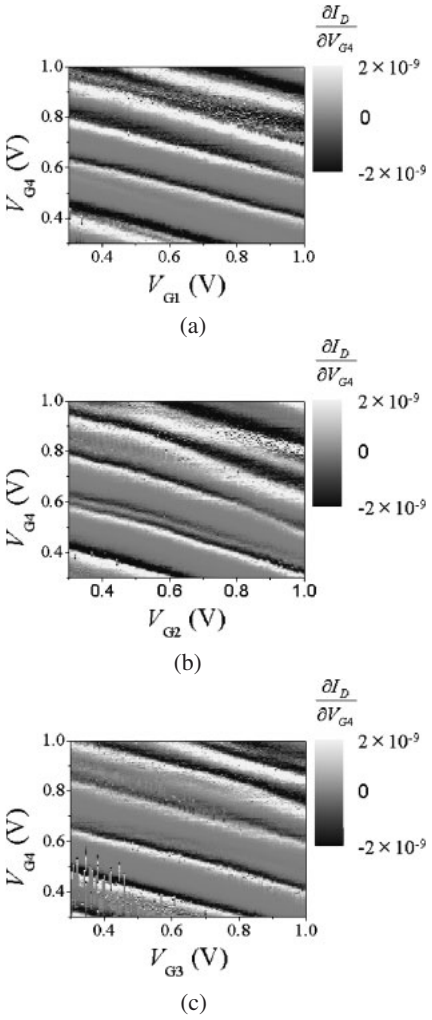

Fig. 2. The gate depended conductance $\partial I_D/\partial V_{G4}$ for the different values of (a) V_{G1}, (b) V_{G2}, and (c) V_{G3}.

SiH_4 gas supply by VHF plasma and deposited on the substrate randomly. Experimental process and formation of nc-Si QD is discussed in detail in refs. 5–7. Integration of size-controlled nc-Si QDs with the SET was done by depositing nc-Si QDs on fabricated SET in the UHV chamber. After fabricating the SET [Fig. 4(a)], a resist hole was prepared in the narrow region between the SET island and three gate electrodes (G1, G2, and G3) using the electron beam lithography as shown in Fig. 4(b). After that, nc-Si QDs were deposited on the SET patterned substrate [Fig. 4(c)]. In the resist hole area nc-Si QDs contacted directly to the substrate. The unwanted nc-Si QDs on the substrate are removed by lift-off process [Fig. 4(d)].

To study the effects of the charge polarizations in the double nc-Si QDs on SET, we carried out three-dimensional capacitance simulation and the equivalent circuit simulation. To estimate the various capacitances in the nc-Si QDs integrated SET [Fig. 5(a)], three-dimensional capacitance simulation was done as explained in measurement and three-dimensional capacitance simulation section for the structure shown in Fig. 3. The simplified equivalent circuit of the SET with nc-Si QDs is shown in Fig. 5(b). QD1 is the nc-Si QD nearer to the SET and QD2 is the nc-Si QD nearer to the triple-gate, and C_{QD1QD2} is capacitance between QD1

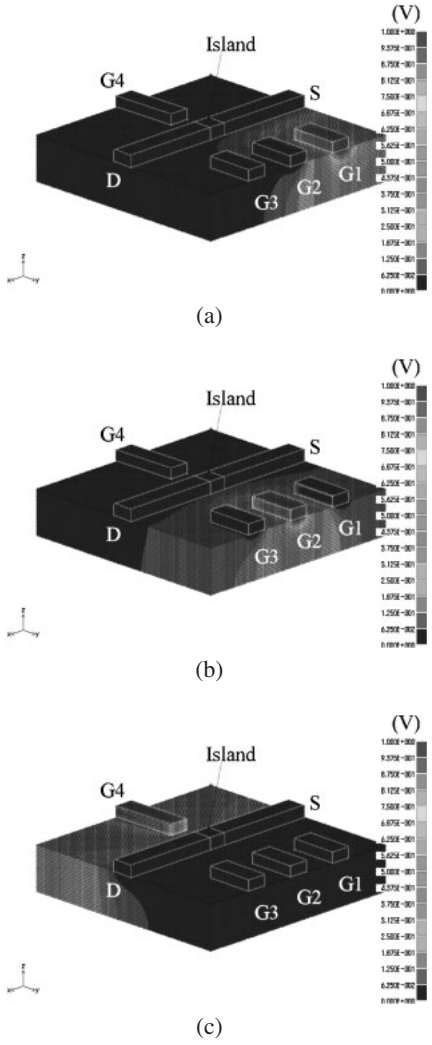

Fig. 3. Potential distributions in the device for the applied 1 V to the gates (a) G1, (b) G2, and (c) G4 respectively.

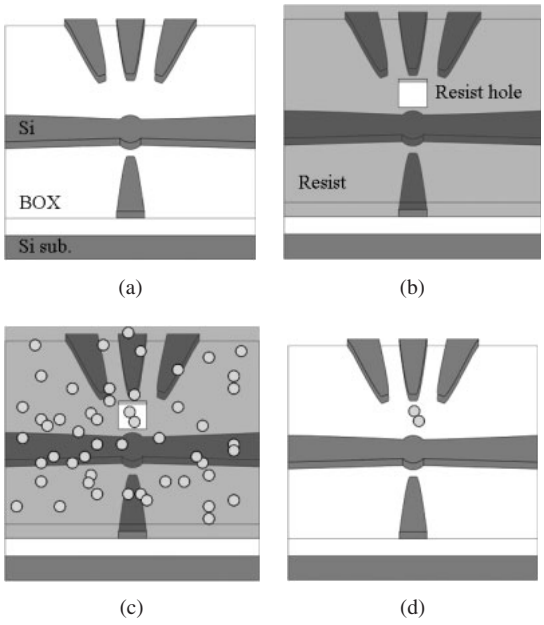

Fig. 4. Schematic diagrams outlining steps involved in the fabrication process: (a) SET with four side-gate; (b) spin coating the surface with a resist material and a resist hole prepared through electron beam lithography; (c) deposition of nc-Si QDs; (d) removing the unwanted nc-Si QDs on the substrate.

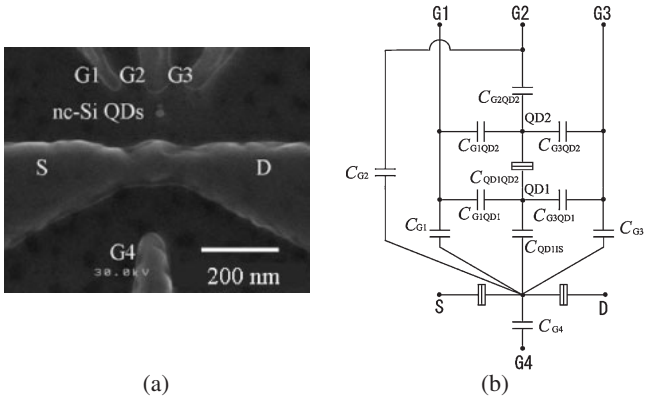

Fig. 5. (a) SEM image of the nc-Si QDs integrated SET. (b) The simplified equivalent circuit of the device shown in (a). QD1 is the nc-Si QD nearer to the SET and QD2 is the nc-Si QD nearer to the triple-gate, and C_{QD1QD2} is capacitance between QD1 and QD2. On the simulations, capacitance C_{G2QD1} between G2 and QD1, and capacitance C_{QD2IS} between QD2 and the SET island were included, and capacitance C_{QD1QD2} between the nc-Si QDs was treated as a normal capacitor to estimate the effects of charge polarizations.

and QD2 in Fig. 5(b). On the simulation, the capacitance between G2 and QD1, and the capacitance between the QD2 and the SET island were included, and C_{QD1QD2} was treated as a normal capacitor to estimate the effects of charge polarizations. Figure 6 shows differential SET current simulated at 4.2 K and 1 mV drain bias in the condition of: (a) $-e$ in the top nc-Si QD and $+e$ in the bottom nc-Si QD ($Q_{QD1} = -e$, $Q_{QD2} = +e$); (b) no charge polarizations in the nc-Si QDs ($Q_{QD1} = Q_{QD2} = 0$); (c) $+e$ in the top nc-Si QD and $-e$ in the bottom nc-Si QD ($Q_{QD1} = +e$, $Q_{QD2} = -e$). I_D–V_{G4} curves at $V_{G2} = 3.2$ V along with dotted lines in 6(a)–6(c) for the three different charge polarizations are shown in 6(d). These results indicate that charge polarization with the magnitude of as small as a fraction of $\pm e$ can be sensed as their remarkable shifts.

5. Conclusions

The single-electron transistor with multiple side gates has been fabricated in the SOI substrate as a highly-sensitive charge detector. We have extracted the coupling capacitance values from the observed Coulomb oscillation characteristics and have shown good agreement with the theoretical estimates obtained using three-dimensional capacitance simulation. Integration of the tunnel-coupled nc-Si DQDs onto the fabricated SET have been carried out for the first time by using *in-situ* deposition. The equivalent circuit analysis of the nc-Si DQD integrated SET has shown that charge polarization with the magnitude of as small as a fraction of $\pm e$ in double nc-Si QDs with diameter of $\sim$10 nm can be sensed with finite shift of the Coulomb oscillation peaks.

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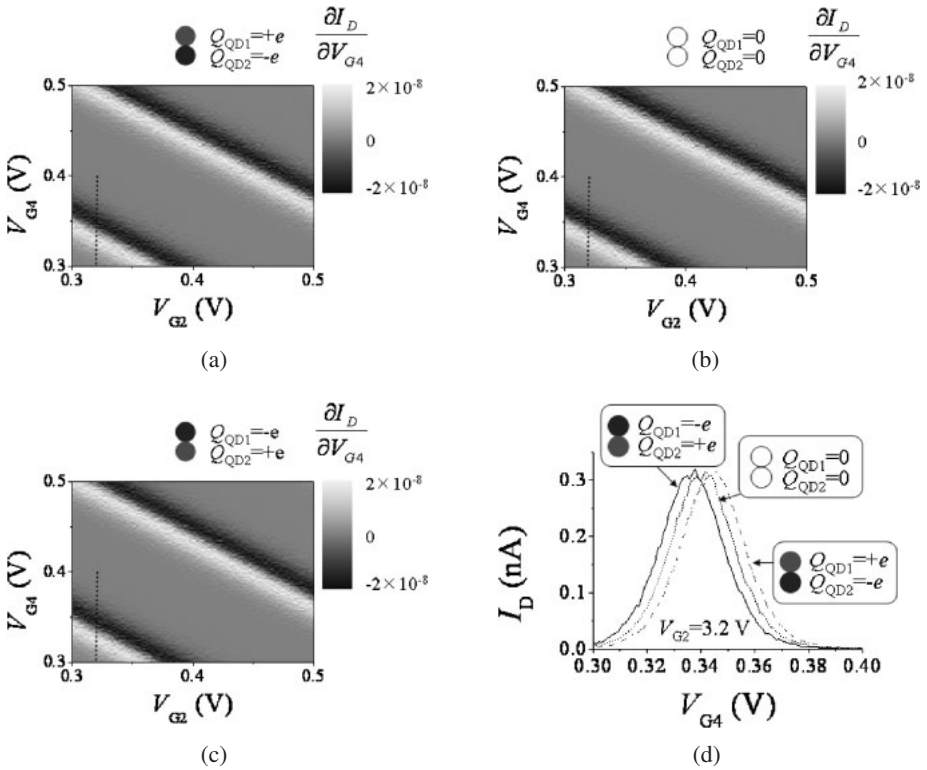

Fig. 6. Differential SET current simulated at 4.2 K and 1 mV drain bias in the condition of: (a) $-e$ in the top nc-Si QD and $+e$ in the bottom nc-Si QD ($Q_{QD1} = -e$, $Q_{QD2} = +e$); (b) no charge polarizations in the nc-Si QDs ($Q_{QD1} = Q_{QD2} = 0$); (c) $+e$ in the top nc-Si QD and $-e$ in the bottom nc-Si QD ($Q_{QD1} = +e$, $Q_{QD2} = -e$). I_D–V_{G4} curves at $V_{G2} = 3.2$ V along with dotted lines in (a)–(c) for the three different charge polarizations are shown in (d).

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