Nanoelectromechanical nonvolatile memory device incorporating nanocrystalline Si dots

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A nanoelectromechanical device incorporating the nanocrystalline silicon (nc-Si) dots is proposed for use as a high-speed and nonvolatile memory. The nc-Si dots are embedded as charge storage in a mechanically bistable floating gate. Position of the floating gate can therefore be switched between two stable states by applying gate bias. Superior on-off characteristics are demonstrated by using an equivalent circuit model which takes account of the variable capacitance due to the mechanical displacement of the floating gate. Mechanical property analysis conducted by using the finite element method shows that introduction of nc-Si dot array into the movable floating gate results in reduction of switching power. High switching frequency over 1 GHz is achieved by decreasing the length of the floating gate to the submicron regime. We also report on experimental observation of the mechanical bistability of the SiO_2 beam fabricated by using the conventional silicon etching processes. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2360143]

I. INTRODUCTION

Various bistable natures observed for nonsilicon materials have been explored intensively for developing nonvolatile and random access memory (RAM) in order to achieve high operating speed and long data-retention time simultaneously. For example, ferroelectric RAM, magnetic RAM, and phase-change RAM are currently investigated as serious candidates. However, all those memory devices require introduction of an unconventional material into silicon device fabrication processes. An alternative bistability mechanism is therefore worth exploring only by using the conventional silicon based materials.

Application of silicon micromachining technologies to the nonvolatile memory device by using mechanical bistability of the object was proposed by Peterson[1] and developed by Hälg.[2] Silicon mechanical objects have a clear advantage of future integration with advanced silicon circuits because they can be fabricated with conventional silicon technology consisting of oxidation, thin film deposition, lithography, and etching.[3] The operating speed of the electromechanical systems depends on the size of the mechanical object and it is generally slower than the electrical switching speed on the scale of micrometer range. However, significant progress of silicon nanofabrication techniques has also enabled to realize the silicon nanoelectromechanical systems (NEMS) with sizes of below 1 μm along with the rapid scaling down of the metal-oxide-semiconductor field-effect transistor (MOSFET) device. Since the operation frequency of electromechanical systems increases with decreasing size, an extremely high-speed operation is expected in the downsized NEMS. Recently, Huang *et al.* reported about 1 GHz oscillation of the SiC beam, the dimension of which was 1.1 μm long, 120 nm wide, and 75 nm thick.[4] One order improvements were made in a decade for both of the beam size and the oscillation frequency.[5] Such high-speed motion in the gigahertz range was also predicted on the multiwall carbon nanotube with the length of 100 nm.[6,7]

All these results could give us an idea that the bistable nature of the NEMS has the possibility to realize a high-speed nonvolatile memory device with the operation speed of several gigahertz or higher. In this paper, we discuss silicon nanoelectromechanical nonvolatile memory device incorporating nanocrystalline-Si (nc-Si) dots. We used nc-Si dots as charge storage in the mechanically movable object with bistable nature. The operation principle of the NEMS memory device in detail is described in the following section. The movable floating gate is a key building block of the NEMS memory device. We studied fundamental mechanical properties of the movable floating gate theoretically in Sec. III. We also mention about switching speed of the nanoscale movable floating gate estimated by transient analysis. Fabrication of a single beam structure and experimental observation of mechanical bistability of the beam is shown in Sec. IV. Section V is dedicated to the summary of this paper. Part of this work has already been reported elsewhere.[8,9]

II. NONVOLATILE NANODOT NEMS MEMORY DEVICE

Figure 1 shows a schematic cross-sectional view of the nanodot NEMS memory device. The NEMS memory features a suspended floating gate beam in the cavity placed

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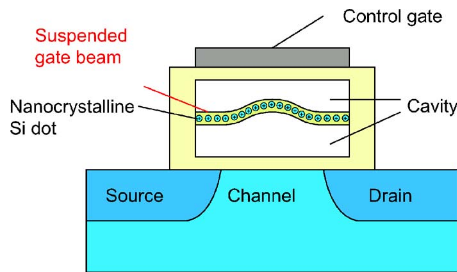

FIG. 1. (Color online) A schematic illustration of a NEMS memory device incorporating nanocrystalline-Si dots.

under the gate electrode, which contains the nc-Si dots as charge storage. The floating gate is bent naturally, either upward or downward. Its ends are clamped at the cavity side walls. When the gate voltage is applied, the floating gate beam moves via electrostatic interactions between the gate electrode and the charge in the nc-Si dots. A positional displacement of the floating gate may be sensed via a change in the drain current of the MOSFET underneath. Mechanical bistability of the beam is therefore essential for achieving our nonvolatile NEMS memory, and a higher switching speed is expected with reducing their dimensions down to the nanometer regime. While the conventional flash memory has big issues of tunnel oxide degradation caused by repeated charge tunneling and low write and erase speed, our NEMS memory device has the advantages of no charge tunneling and the high-speed write and erase operation. In addition, fabrication process of the NEMS is compatible with conventional Si process without introducing any other strange materials. We can estimate the on-off ratio of this device simply from the difference of surface potential change induced by applied gate bias between upward- and downward-bent beams. We assume the substrate is p-type Si, and the positive charge is stored in the beam. The upward- and downward-bent states correspond to "0" or "off" state and "1" or "on" state, respectively. Structural parameters used for the present calculations are shown in Fig. 2(a), where the cavity height is 200 nm and the initial displacement of the beam is assumed to be 50 nm. Figure 2(b) shows an equivalent circuit we use in this estimation. In Fig. 2(b), C_U is the capacitance between the metal gate and the floating gate, C_L is the capacitance between the floating gate and the substrate surface, and Q is the charge stored and confined in the floating gate. Applied gate bias V_g is given as

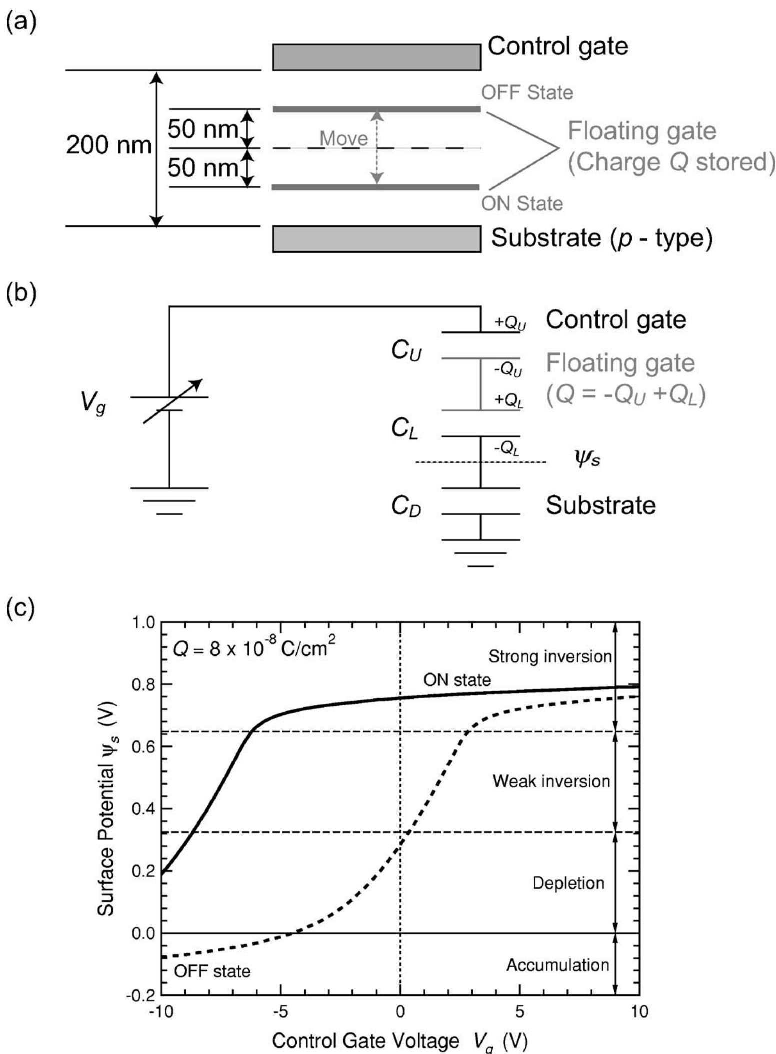

FIG. 2. (a) A schematic illustration of the NEMS memory cell model used in the on-off ratio calculation. The position of the beam in "On" and "Off" states is 50 nm lower or higher than the center between surfaces of control gate and substrate in the cavity. (b) Equivalent circuit of the NEMS memory cell. The dashed line shows the position of the surface of the substrate. C_D is the capacitance of the depletion layer. (c) Calculated surface potential ψ_s as a function of applied gate voltage V_g. The solid and dashed lines correspond to the On and Off states, respectively. Cases at the semiconductor surface in a certain ψ_s range are depicted on the right hand side with arrows.

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$$V_g = \frac{Q_U}{C_U} + \frac{Q_L}{C_L} + \psi_s, \tag{1}$$

where Q_U and Q_L are charges that emerge from the capacitor surfaces and ψ_s is the surface potential on the silicon substrate. The stored charge,

$$Q = -Q_U + Q_L, \tag{2}$$

is assumed to be maintained in the beam. The positional change of the floating gate induces the change in C_U and C_L, and then varies Q_U and Q_L. Q_L is equal to the absolute value of the surface charge $|Q_s|$, which is related to ψ_s as

$$Q_L = |Q_s| = \frac{\sqrt{2}kT}{qL_D} F\left(\psi_s, \frac{n_{p0}}{p_{p0}}\right), \tag{3}$$

where L_D is the Debye length, and n_{p0} and p_{p0} are the electron and hole densities in the p-type substrate.[10] Figure 2(c) shows surface potential curves for the on and off states calculated from Eqs. (1)–(3) as a function of gate voltage. We found large on-off ratio of 10^{10} from the difference between ψ_s's of on and off states at $V_g=0$ in the case with Q of 8×10^{-8} C/cm^2, which corresponds to n_s of 5×10^{11} cm^{-2}, where n_s is the number density of charge storage in a unit area. Note that the on-off ratio at $V_g=0$ was reduced to 10 in the case with Q of 1.6×10^{-7} C/cm^2, which corresponds to n_s of 1.0×10^{12} cm^{-2}, and is not sufficient for switching devices. The above analysis shows that device operation is quite sensitive to the amount of charge in the beam. If we use a beam incorporating nc-Si of several nanometers in diameter, we can easily control the area density of the charge in the beam. Once an electron is stored in such a small Si nanodot, another electron transfer probability into the dot is strongly reduced due to the Coulomb blockade effect even at room temperature.[11] The amount of charge in the beam can therefore be determined by the number of Si nanodots. We used a very-high-frequency digital plasma process for nc-Si deposition that facilitates deposition of nc-Si dots of 8 ± 1 nm in diameter.[12,13] Density of the 8 nm nc-Si dots is typically about 10^{11}–10^{12} cm^{-2} in a monolayer, which are the same order with n_s required for the large on-off ratio operation. We can control the amount of the nc-Si dots precisely by adjusting the deposition condition, therefore, we believe that this technique is suitable for fabricating the charged beam.

III. THEORETICAL STUDIES OF BASIC DEVICE CHARACTERISTICS

In this section, we discuss the basic device characteristics theoretically. Mechanical properties of the movable floating gate beam are closely related to the fundamental characteristics of the memory operation, such as the switching speed and the operation voltage. We therefore estimate several basic device characteristics by using the finite element method (FEM) simulation, which is frequently used in the analysis of mechanical properties of materials in terms of elastic continuum approximation.

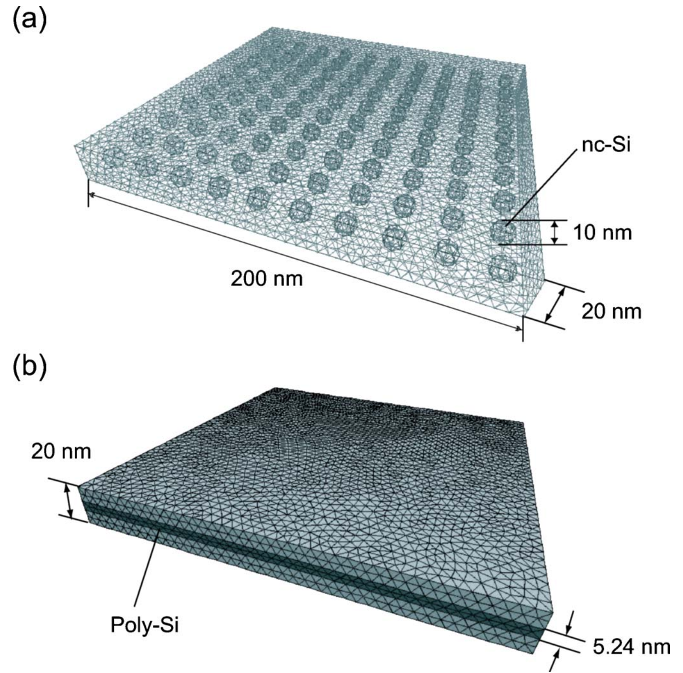

FIG. 3. (Color online) (a) A 3D image of a nc-Si beam model used in this calculation. The 2D array of spheres (nc-Si dots) is clearly identified in the sheet (SiO_2). (b) An image of a poly-Si beam model in which a thin sheet (Si) is placed between two SiO_2 layers. The fine lines in the figures show the boundary of the mesh used in this study.

A. Effect of nc-Si incorporation on the mechanical properties

First we study the effects of nc-Si incorporation on the mechanical properties of the movable beam. Mechanical properties of the beam were analyzed by using ADVENTURE system,[14] a parallel three-dimensional (3D) FEM simulator. Here we focus on the nc-Si beam structure, in which a two-dimensional array of nc-Si dots with the diameter of 10 nm is embedded in a SiO_2 film [Fig. 3(a)]. We also investigated a simple poly-Si beam structure, in which a thin Si sheet of 5.24 nm in thickness is placed between SiO_2 layers [Fig. 3(b)] as a reference. The size of both beams is $200 \times 200 \times 20$ nm^3, and the ratio of volume of Si to that of SiO_2 is the same for both beams. Young's modulus and Poisson's ratio are 190 GPa and 0.27 for Si, and 70 GPa and 0.175 for SiO_2, respectively.[15,16] Figure 4 shows a calculated 3D image of the beam deformed under a constant homogeneous pressure with 5.0×10^{-10} N/nm^2 parallel to the z axis, where the z axis is perpendicular to the initial beam plane. We found the

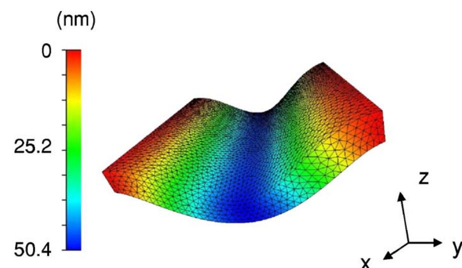

FIG. 4. (Color online) A calculated 3D image of the nc-Si beam model deformed under a constant homogeneous load parallel to the z axis. Dark area around the center of the beam was largely deformed.

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maximum central displacement of 50.4 nm for the nc-Si-dot beam, which is larger than that of 48.5 nm for the poly-Si beam with the same pressure. The result suggests that the nc-Si-dot beam has an advantage for low power consumption, because the relatively larger displacement was obtained against the same applied force, which corresponds to the applied gate voltage in terms of the NEMS memory operation.

B. Mechanical bistability

Next, we study mechanical bistability of the beam by using NE/NASTRAN,[17] which takes account of the nonlinearity in the load-displacement relationship. The buckling of the beam should be introduced in the nonlinear analysis properly because it is an essential phenomenon to realize the bistability in the NEMS memory. Dimensions of the nc-Si-dot beam are 400 nm in length, 200 nm in width, and 20 nm in thickness. The initial buckled state was formed from the plane beam as follows. First we introduce the internal stress by loading a small force of 0.1 μN along the x axis parallel to the longest dimension of the beam. After we apply a light load along $-z$ direction, the initial downward-bent buckled state was formed with the initial displacement of about 24 nm. With increasing the load along the $+z$ direction gradually, a sudden change of the displacement took place due to the buckling of the beam at a point where the load strength was about 0.5 μN. We also observed a similar sudden change during gradual loading along $-z$ direction. Figure 5 shows the maximum central displacement of the beam from $z=0$ as a function of applied force, together with beam shapes of the upward- and downward-bent states, respectively. The hysteresis observed in Fig. 5 is a direct evidence of bistability.

In estimation of elastic potential U, first we shall evaluate the restoring elastic force f against the beam deformation as a function of the beam displacement. U can be calculated from f by the following integration; $U=-\int f dz$. Figure 6 displays U as a function of the beam displacement. We can clearly identify a double minimum structure which is characteristic of the bistable system. Note that the height of the potential at zero displacement corresponds to the potential barrier of switching between two bistable states. The value is directly related to the magnitude of switching voltage. Although the current result shows rather higher value about 10 kV, we can reduce this bias voltage down to several tenth volts by choosing appropriate structural parameters of the beam-in-cavity memory cell. Details will be described elsewhere.[18]

C. Estimation of write and erase operation speed

In this section, we estimate the write and erase operation speed. Here, we have to consider the frequency of the oscillation between two bistable states, which corresponds to write and erase operation speed of the nonvolatile NEMS memory device. Note that this frequency is different from the resonance frequency of the beam. First, we briefly mention the result of a quite simple model based on the equation of motion, $md^2Z/dt^2=F\mp f$, where Z is the maximum displacement of the beam, m is the total mass of the beam, and F is the external force applied to the beam along the z axis. The elastic force f is represented as $f=kS\Delta V/V$, where k is the elastic volume constant, S is the loading area, V is the volume of the beam, and ΔV is the volume change of the deformed beam. If Z is positive, where f is acting against F, we use the minus sign in the equation of motion; if Z is negative, the plus sign is used. We roughly estimated the oscillation frequencies of about 2 GHz for the SiO_2 beam with the size of $1\times1\times0.1$ μm^3 and of about 20 GHz with the size of

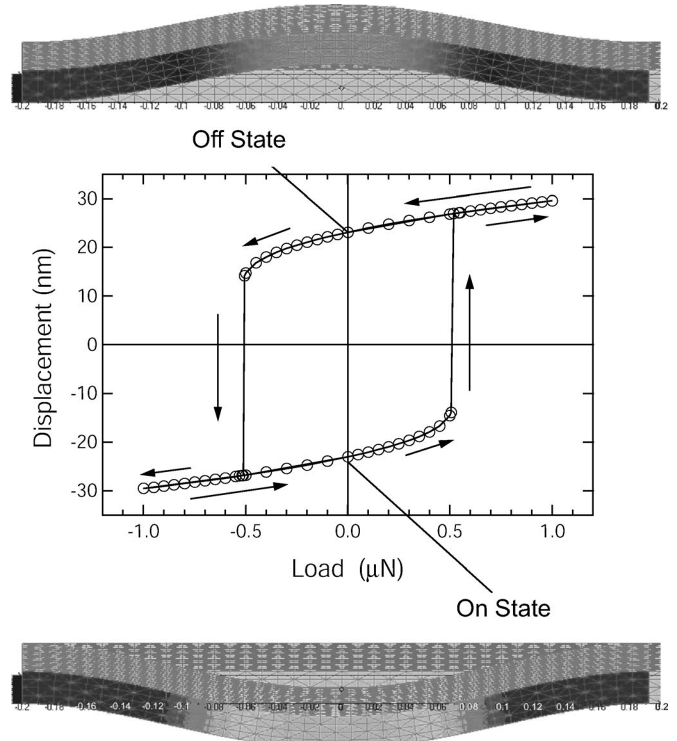

FIG. 5. A displacement of the beam was plotted as a function of applied load parallel to the z axis. Abrupt change of the displacement of the beam and clear hysteresis were observed, which are due to the mechanical bistable nature of the beam. The images above and below the figure are the shape of upward-bent beam at the Off state and that of downward-bent beam at the On state, respectively.

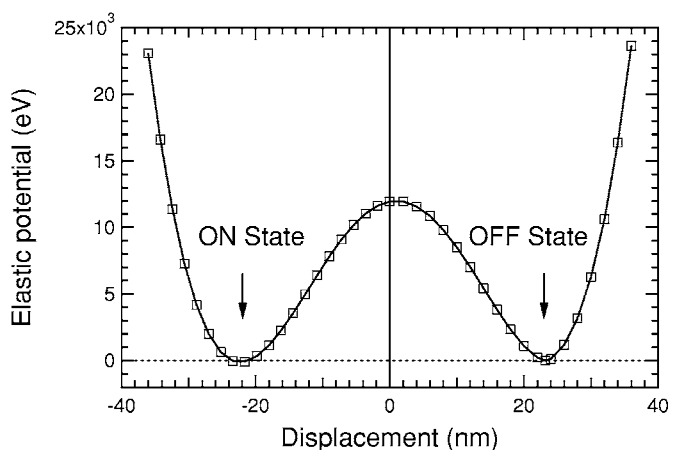

FIG. 6. Elastic potential as a function of the displacement of the beam. Double minimum structure which is characteristic of the system bistability is clearly observed.

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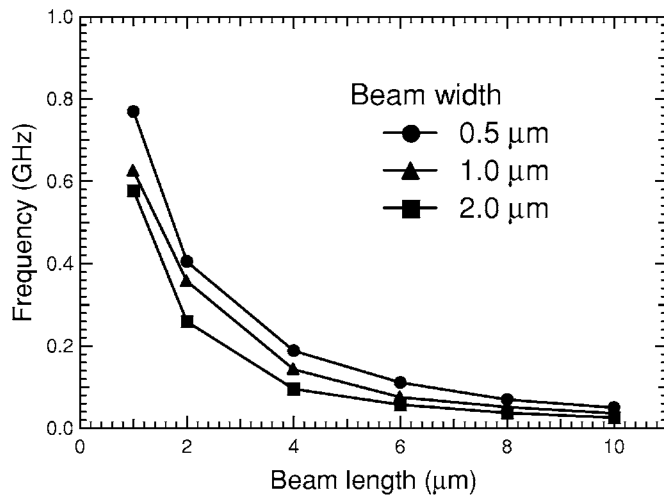

FIG. 7. The oscillation frequencies of the beam as a function of the beam length are shown for beams with three different widths; 0.5, 1.0, and 2.0 μm.

$0.1 \times 0.1 \times 0.01\ \mu m^3$ from this calculation. The speed of the write/erase operation in the NEMS memory was therefore more than 10^3 times higher than that of the conventional current flash memory.

In order to investigate the size dependence of switching speed further, we used transient analysis algorithm in the nonlinear FEM simulator.[17] The damping of the motion was ignored in this estimation. First we made a model shape of the beam with an initial displacement of 100 nm. Then the concentrated load of 300 μN was applied to the beam for 0.1 s. An oscillation was clearly identified in the time evolution of the beam displacement. The oscillation frequency calculation was performed for various beams with different dimensions. Figure 7 shows the estimated oscillation frequency as a function of beam length at three different beamwidths. The frequency increases with decreasing beam length and beamwidth and increases rapidly below 4 μm of the beam length. About 0.8 GHz was achieved for the beam with the size of 1 μm length and 0.5 μm width. Furthermore, rapid increase up to gigahertz range is expected with further reduction of the beam length. These estimations show that the NEMS memory is promising for nonvolatile memory, where the high-speed write and erase operation is realized.

IV. EXPERIMENTAL STUDIES OF THE DEVICE FABRICATION

In the following section, we show results of a single beam structure fabrication which is considered as a step towards the beam-in-cavity structure fabrication. The single beam structure fabrication is also suitable for observing the basic mechanical properties of the beam with a size below several micrometers. We also show the result of nanoindentor test for the single beam structure.

A. Fabrication of single beam structure

Schematic illustration of the single beam structure is shown in Fig. 8(a), and the fabrication process is as follows.

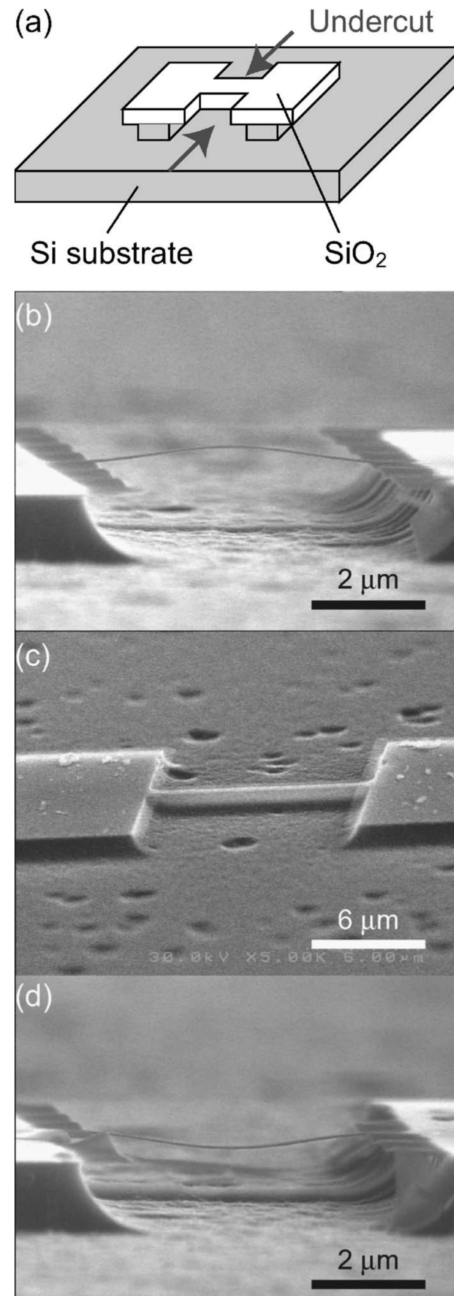

FIG. 8. (a) A schematic illustration of a SiO_2 single layer structure fabricated by etching of Si underneath using CF_4/O_2 plasma. The SEM images of (b) an upward-bent thermally grown SiO_2 beam, (c) a PECVD-grown SiO_2 beam with no bending, and (d) a downward-bent thermally grown SiO_2 beam. Only thermally grown SiO_2 beams show bending after undercutting.

After wafer cleaning, 170-nm-thick SiO_2 was formed by dry oxidation followed by patterning with the help of photolithography or electron-beam lithography. The pattern was copied to SiO_2 by using anisotropic dry etching with CF_4 gas. A 2 μm undercut was realized by the following isotropic plasma dry etching using CF_4/O_2 chemistry with a Si/SiO_2 etching selectivity ratio of over 100.

The scanning electron microscope (SEM) images in Figs. 8(b)–8(d) are beams after undercutting silicon underneath. Most beams bend upward naturally as shown in Fig. 8(b), which was considered as a result of the release of mechanical stress stored in SiO_2 during thermal oxidation. In

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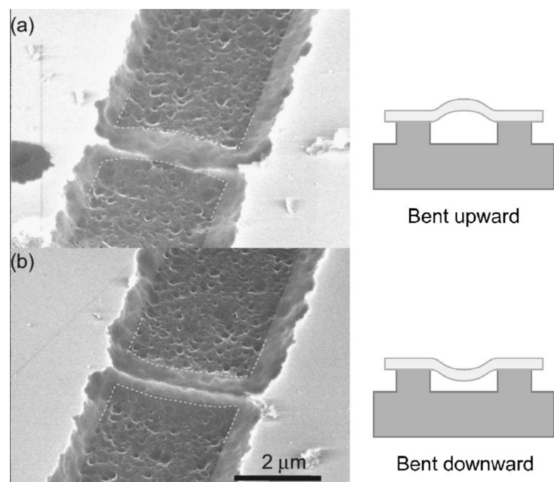

FIG. 9. The SEM images of beams (a) before and (b) after being loaded with the tip of the nanoindenter around the center of the beam. The schematic cross-sectional illustrations are shown together. The dashed lines along the edges of the SiO_2 beams are the guides to the eyes.

the case of SiO_2 formed by plasma enhanced chemical vapor deposition (PECVD), no bent beam was observed as shown in Fig. 8(c). Note that several downward-bent beams were also observed as shown in Fig. 8(d). We also observed various deformation modes in the longer beams. All of these results showed that thermal stress induced during oxidation plays an important role to form initially bent beam, which is a crucial building block for the nonvolatile memory operation in the NEMS memory device. Control of the internal stress in the SiO_2 beam is therefore an important issue for further process optimization.

B. Direct observation of mechanical bistability

In order to investigate the bistable nature of the beam more directly, we applied the nanoindenter type loading system[19] to our single SiO_2 beams. As was already mentioned, most of the fabricated beams bend upward. Figure 9(a) shows a typical SEM image of the upward-bent beam in the test chip. We loaded around the center of the beams with the tip of the nanoindenter. Figure 9(b) shows a SEM image of a single beam taken after loading. We observed clear downward-bent beam, which was the direct observation of the bistable nature of the beam. This result also suggests that the bistable states can be switched by applying an external force. It is important to estimate a value of external force required for switching the beam. No anomaly was, however, observed on the load-displacement curve, which means the force necessary to switch the beam is below $\sim 10\ \mu N$, the resolution limit of the nanoindenter. This result is quantitatively consistent with the calculation results in Fig. 5, where the buckling took place at $\sim 0.5\ \mu N$.

V. SUMMARY

We proposed the nanodot NEMS memory device which can realize the high-speed and nonvolatile memory operation and can be fabricated with well-compatible processes with current silicon technologies. Sufficient on-off ratio was estimated from the analysis of the equivalent circuit model. We also suggested that the nc-Si dot incorporation into the movable floating gate beam had the advantage of low power operation. We clearly observed the mechanical bistability of the movable floating gate beam both experimentally and theoretically. About 1 GHz switching speed was estimated by FEM simulation, which is applicable to future high-speed and nonvolatile memory device.

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