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Simulation Study of the Dependence of Submicron Polysilicon Thin-Film Transistor Output Characteristics on Grain Boundary Position

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We investigate the impact of varying the grain boundary (GB) position on the output (I_d–V_d) characteristics of submicron single GB polysilicon thin film transistors (TFTs), by two-dimensional (2D), drift-diffusion based, device simulation. We employ a localized GB trapping model with a distribution of both donor-like and acceptor-like trap states over the forbidden energy gap of the GB region. We show that for devices with channel lengths in the deep submicron regime, significant variations in output conductance (g_d) occur as the GB position is varied. Specifically, we find that output conductance increases as the GB approaches the drain edge. Furthermore, the sensitivity of output conductance to the GB position increases as channel length decreases. The findings have important implications for any future analogue three-dimensional (3D) IC design that uses polysilicon as a device material. [DOI: 10.1143/JJAP.44.8322]

KEYWORDS: polysilicon, short channel effects, grain boundary, thin-film transistor, device simulation

1. Introduction

The polysilicon thin-film transistor (TFT) has gained attention in recent years as an attractive device for use in flat panel active matrix displays (AMLCDs)[1,2] and as a transistor element in static random access memories (SRAM) cells.[3] It has also been suggested as a candidate for future applications in three-dimensional (3D) IC designs.[4] Polysilicon is attractive as a device material because it is cheap and easy to deposit and offers a higher carrier mobility than amorphous silicon (a-Si), thus enabling the realization of better device characteristics. However, polysilicon is granular in structure, with the crystalline grains separated by highly disordered grain boundary (GB) regions. This results in an average carrier mobility that is still significantly lower than that for a single crystal silicon device.

A well established method of forming polysilicon films is the solid phase crystallisation (SPC) of deposited a-Si. This technique provides good uniformity of grain size; however, the grains themselves are small—in the order of hundreds of nanometres or less.[5]

As a consequence, long channel devices contain many GBs. However, if we scale the transistor down to the submicron regime, channel length approaches the grain size, and only a small number of GBs will be present in the device.[6,7] Despite the recent advances in the fabrication of polysilicon films, the exact control of the position of GBs in conventional SPC polysilicon films is not possible. The random nature of the location of GBs in the TFT channel may introduce significant variations in the electrical characteristics of devices fabricated on the same substrate. Therefore, if SPC polysilicon is to be used as a device material for submicron TFTs, we must investigate the impact of the location of individual GBs on TFT characteristics.

Previous studies examined threshold voltage fluctuations, as the number and position of GBs were varied in the channel of a TFT.[8–11] However, in these studies the GB positional dependence of the output characteristics of the TFT was not thoroughly investigated. Furthermore, only TFTs with channel lengths equal to or greater than one micron were studied.

The transistor operating point for analog applications typically lies in the saturation region and therefore any variation in output characteristics due to GBs would have important implications for analogue VLSI design.

A parameter of importance in characterising the TFT in this regime is the output conductance $g_d = \partial I_d/\partial V_d$. The purpose of this work is to investigate how the position of a single perpendicular GB present in the channel region effects the output conductance g_d of short-channel TFTs. By varying the position of the GB relative to the source in our simulation model we aim to observe any variation in output characteristics.

2. Description of Simulation Method

2.1 Drift-diffusion model

For our simulation study, a commercially available device simulator, "ATLAS", was used.[12] We used a drift-diffusion (DD) simulation model in which the basic equations used are similar to those used for a single-crystal device except that trapped charges are included in Poisson's equation, and a modified Shockley–Read–Hall (SRH) recombination term[13,14] is used in the carrier continuity equations. We are modelling devices, in which only a small number of GBs exist in the channel and therefore, using a model where the traps are spread uniformly across the channel region would be unrealistic. A more appropriate modelling approach is to localize trap states at GB regions that are explicitly introduced in the device model.

Due to the high electric fields that exist in short-channel devices, the velocity of carriers will begin to saturate. To take into account velocity saturation, a mobility model dependant on the electric field in the direction of current flow is used. This is based on the Caughey and Thomas expression,[15] which also includes the modelling of mobility dependence on carrier concentration.

It should be noted that a model for impact ionization is not included in the present simulation. The results of this study therefore cannot be explained by the so called "kink" effect.[16]

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2.2 *Modelling of GB trap states*

To model the inclusion of trap states in the forbidden gap, the space charge term on the right-hand side of Poisson's equation is modified by including an additional charge term, Q_T, representing trapped charge. This is given by

$$-\rho = q(p - n + N_D^+ - N_A^-) + Q_T \tag{2.1}$$

$$Q_T = q(p_T - n_T), \tag{2.2}$$

where N_D^+ and N_A^- are the ionized donor and acceptor concentrations and p_T and n_T are the trapped hole and electron concentrations respectively.

We assume that the trap states consist of both donor-like and acceptor-like states distributed across the forbidden energy gap, where the donor-like states act as hole traps and the acceptor-like traps as electron traps. Therefore, the total density of states is given by

$$g(E) = g_D(E) + g_A(E), \tag{2.3}$$

where $g_D(E)$ is the total density of donor-like trap states and $g_A(E)$ is the total density of acceptor-like trap states. To calculate the trapped charge, we perform a numerical integration of the product of trap density and its occupation probability over the forbidden energy gap. This gives

$$n_T = \int_{E_V}^{E_C} g_A(E) f_A(E, n, p)\, dE \tag{2.4}$$

$$p_T = \int_{E_V}^{E_C} g_D(E) f_D(E, n, p)\, dE \tag{2.5}$$

for trapped electrons and holes where f_A and f_D are the occupation probability for acceptor-like and donor-like traps respectively.

The occupation probabilities are then given by

$$f_A = \frac{\upsilon_n \sigma_{ae} n + \upsilon_p \sigma_{ah} p_t}{\upsilon_n \sigma_{ae}(n + n_t) + \upsilon_p \sigma_{ah}(p + p_t)} \tag{2.6}$$

$$f_D = \frac{\upsilon_n \sigma_{de} n + \upsilon_p \sigma_{dh} p_t}{\upsilon_n \sigma_{de}(n + n_t) + \upsilon_p \sigma_{dh}(p + p_t)}, \tag{2.7}$$

where σ_{ae}, σ_{ah} and σ_{de}, σ_{dh} are the electron and hole capture cross sections for acceptor-like and donor-like traps, respectively. The effective electron and hole concentrations n_t and p_t are defined as

$$p_t = n_i \exp\left[\frac{E_i - E}{kT}\right] \tag{2.8}$$

$$n_t = n_i \exp\left[\frac{E - E_i}{kT}\right], \tag{2.9}$$

where n_i is the intrinsic carrier concentration, E is the trap energy level, E_i is the intrinsic Fermi level and T is the lattice temperature.

The SRH recombination/generation rate[13,14] per unit time is modified to include multiple trap levels and is given by

$$U_{n,p} = \int_{E_V}^{E_C} \left[\frac{\upsilon_n \upsilon_p \sigma_{ae} \sigma_{ah}(np - n_i^2) g_A(E)}{\upsilon_n \sigma_{ae}(n + n_t) + \upsilon_p \sigma_{ah}(p + p_t)} + \frac{\upsilon_n \upsilon_p \sigma_{de} \sigma_{dh}(np - n_i^2) g_D(E)}{\upsilon_n \sigma_{de}(n + n_t) + \upsilon_p \sigma_{dh}(p + p_t)} \right] dE \tag{2.10}$$

2.3 *Trap state distribution model*

The device simulation package ATLAS allows us to define a density of defect states as a combination of four bands. Two tail bands are specified to contain large numbers of defect states at the conduction band (acceptor-like traps) and valence band (donor-like traps) edges, respectively. These decay rapidly as we move towards the center of the forbidden energy gap. In addition, two deep-level bands are defined (acceptor-like and donor-like), which are modelled using a Gaussian distribution, with a peak close to the middle of the forbidden energy gap. The equations describing these terms are given in ref. 12. It should be noted that we assume that there is no difference between the capture cross sections of the tail and Gaussian traps. This assumption is made throughout the derivation of the SRH recombination/generation rate presented in the previous section.

However, many different trap density distributions have been proposed to describe the position and density of traps within the polysilicon forbidden energy gap. These have consisted of single energy level models,[17,18] models with single[19] or double[20–22] exponential tail states, Gaussian shaped distributions[1,23,24] or both.[25,26] It has been suggested that while tail states dominate the above-threshold behavior, mid-gap states primarily effect the subthreshold behaviour.[19,20] Although in this study we are only concerned with the above-threshold region, to ensure a realistic model we choose to include both mid-gap and tail states. The trap density distributions used in our simulation study are plotted in Fig. 1 as a function of energy.

As it is widely accepted that the trap density distribution contains exponential band tails at the valence and conduction band edges, when deciding on a suitable distribution the main qualitative choice is whether to include mid gap states as additional exponential terms such as in refs. 20–22 or as Gaussian terms used in refs. 26–28. We chose to use Gaussian terms because the studies dealing with SPC films suggest a peak in trap states near the mid gap and we are considering SPC films in this work. The values chosen are in the range suggested in ref. 27 and are shown in Table I.

3. Simulation of a 400 nm TFT

3.1 *Device structure*

Figure 2 shows the basic device structure we used in the device modelling. In this simple structure we assumed a thin polysilicon layer of 25 nm, which according to scaling theory[29] is needed for satisfactory performance of a short

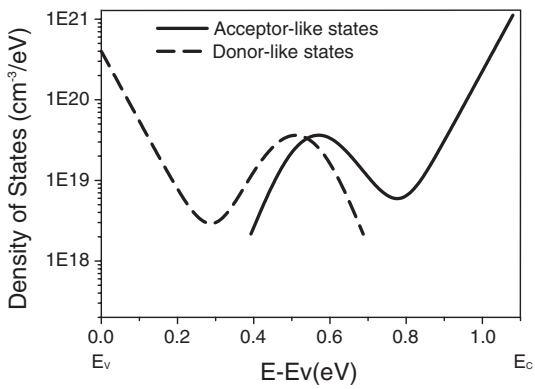

Fig. 1. Distribution of acceptor/donor-like trap states across the forbidden energy gap used in the simulation study.

Table I. Device Parameters used in Simulations.

Device parameter	Value
Channel length L (nm)	400
Channel width L (μm)	1
Gate oxide thickness t_{ox} (nm)	10
Polysilicon thickness t_{si} (nm)	25
Buried oxide thickness (BOX) t_{box} (nm)	25
Source and drain dopant density n^+ (cm^{-3})	1×10^{21}
Width of grain boundary W_{gb} (nm)	4
Capture cross section of electrons in acceptor-like states σ_{ae} (cm^2)	1×10^{-16}
Capture cross section of holes in acceptor-like states σ_{ah} (cm^2)	1×10^{-14}
Capture cross section of electrons in donor-like states σ_{de} (cm^2)	1×10^{-14}
Capture cross section of holes in donor-like states σ_{dh} (cm^2)	1×10^{-16}
Density of acceptor-like tail states N_{TA} ($cm^{-3}\,eV^{-1}$)	1×10^{21}
Density of donor-like tail states N_{TD} ($cm^{-3}\,eV^{-1}$)	4×10^{20}
Density of acceptor-like Gaussian states N_{GA} ($cm^{-3}\,eV^{-1}$)	5×10^{19}
Density of donor-like Gaussian states N_{GD} ($cm^{-3}\,eV^{-1}$)	5×10^{19}
Decay energy for acceptor-like tail states W_{TA} (eV)	0.05
Decay energy for donor-like tail states W_{TD} (eV)	0.05
Decay energy for acceptor-like Gaussian W_{GA} (eV)	0.1
Decay energy for donor-like Gaussian W_{GD} (eV)	0.1
Energy of Gaussian for acceptor-like states E_{GA} (eV)	0.51
Energy of Gaussian for donor-like states E_{GD} (eV)	0.51

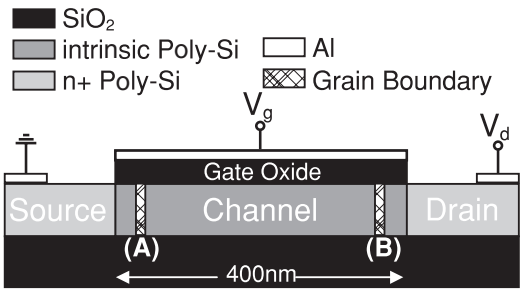

Fig. 2. Device structure used in simulation study. The GB was placed either (a) 40 nm from the source or (b) 40 nm from the drain.

channel device. A gate oxide of 10 nm is chosen, which we estimate to be near the limit of thickness that is possible in polysilicon due to surface roughness at the oxide–polysilicon interface.[30] The source and drain regions are heavily doped n-type materials with a density of $1 \times 10^{21}\,cm^{-3}$, while the channel region is intrinsic. In our model there are no trap states located in the grain regions, only in the GB region. In previous simulation studies the GB width was assumed to be within 1–5 nm, in our simulation it is 4 nm, which is within this range.[8,9] It is assumed that the GB lies perpendicular to the channel. In this orientation it will have the maximum effect on the carrier transport, although in a real film the orientation of the GB would of course be random.

In order to investigate the effect of GB position on TFT output characteristics we chose to firstly simulate a short channel device with a channel length of $L = 400$ nm. We chose 400 nm as this is near the upper limit of the size of grains that can be obtained by SPC of deposited a-Si.

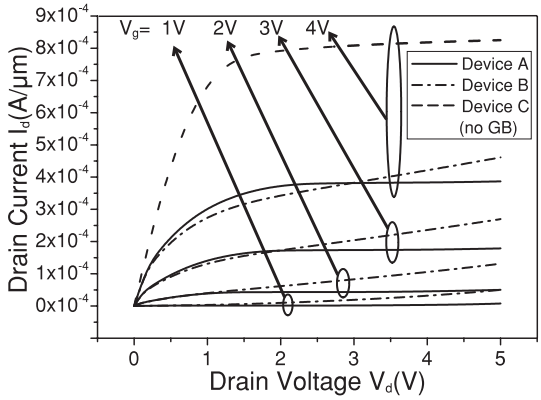

Fig. 3. Comparison of simulated output characteristics of a 400 nm TFT when GB is 40 nm from source (Device A) or drain (Device B) or with no GB (Device C).

The grains of polysilicon were assumed to be columnar. In the channel of the modelled device only a single GB was included and oriented so that it was perpendicular to the semiconductor interface.

The GB position was varied so that it was either close to the source edge or near the drain edge of the channel. The I_d–V_d characteristics were then simulated and compared to study any variations due to the position of the GB.

3.2 Electrical characteristics

In Fig. 3 we show an overlay of the I_d–V_d characteristics of a 400 nm device with a GB positioned 40 nm from the source edge (device A) and 40 nm from the drain edge (device B). It can be seen that there is a clear difference between the two sets of results. It is observed that, in device B the drain current does not saturate and instead increases with drain voltage V_d. However, for device A, where the GB is proximate to the source, there is good saturation of the output current. The characteristics are qualitatively similar to those measured in an experimental study,[31] for a TFT where a large density of GBs were positioned either at the source or drain.

To further investigate the effect of the GBs, we also include an overlay of a device with no GB (device C) at a gate voltage of $V_g = 4$ V. In both devices A and B, the drain current is significantly lower than in device C. It is also noted that—similar to device A, device C also has good current saturation.

3.3 Physical origin of 400 nm TFT output characteristics

Two effects are observed when we compare the TFT characteristics (devices A and B) with those of the single-crystal device (device C). Firstly, there is the decrease in drain current (both devices A and B) and secondly there is the lack of saturation when the GB is close to the drain (device B only).

The reduction in drain current can be explained in terms of the classic model proposed by Seto.[32] It tells us that when carriers become trapped at the GB, potential barriers can form to impede carrier transport. When all the traps at the GB become full any additional carriers act to reduce the depletion width at either side of the barrier. This then causes the barrier height to recede. In a TFT, when the gate bias is

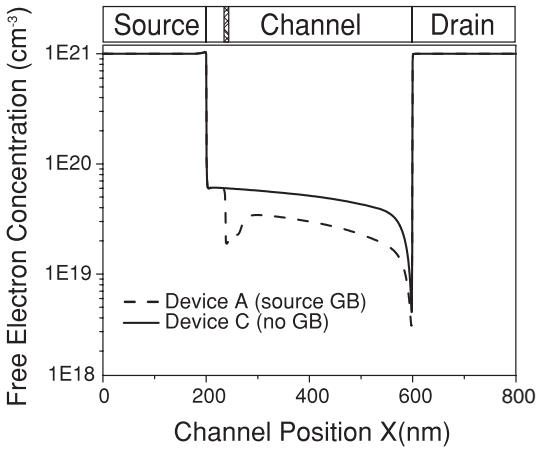

Fig. 4. Cross section of the free electron concentration close to the semiconductor interface for a device with a GB 40 nm from the source edge (Device A) and with no GB (Device C).

increased, the carriers induced in the inversion layer become trapped at the GBs. The traps begin to fill and the potential barrier increases in height. If we continue to increase the gate bias the traps will become full, and then any additional carriers will reduce the depletion width at either side of the GB and therefore lower the potential barrier. The need to lower the GB potential barrier is the cause of an increase in threshold voltage, relative to an equivalent SOI device.[18] In terms of the carrier concentration of the inversion layer, the TFT will have a lower number of carriers than an SOI equivalent device under the same gate bias. To illustrate the reduced concentration of carriers in the inversion layer, in Fig. 4, we plot a cross section of free electron concentration a few nanometres from the semiconductor/oxide interface. Under the same bias conditions $V_d = V_g = 4\,V$, device A shows a free electron concentration that is clearly much lower than device C.

To investigate the physical origins of the second effect—increasing output conductance as the GB approaches the drain—we examined the conduction band profile across the surface of the device as shown in Fig. 5. The bias conditions were ($V_d = V_g = 4\,V$) and we plot for devices where the GB was (a) near the source, (b) drain, and for comparison purposes (c), when there was no GB in the channel. For further clarity, in Fig. 6, we also plot a cross section of conduction band potential a few nanometres from the semiconductor/oxide interface. Figure 6 also highlights the relative height of the GB potential barrier of the devices.

The comparison of the conduction band diagram when the GB is close to the source (device A) with that for a device with no GB present (device C) shows that a large potential drop occurs at the GB region in device A. After the GB, the potential drops smoothly across the rest of the channel, in much the same manner as for a device with no GB. It seems that the GB in this case acts as a very large series resistance. In addition, there is still a small potential barrier at the GB of approximately 0.038 eV in height, which would also impede carriers.

Now if we consider the case when the GB is close to the drain (device B) we can observe that, compared with the device with no GB (device C), there is a small potential drop across the channel, until the GB is reached, at which point all

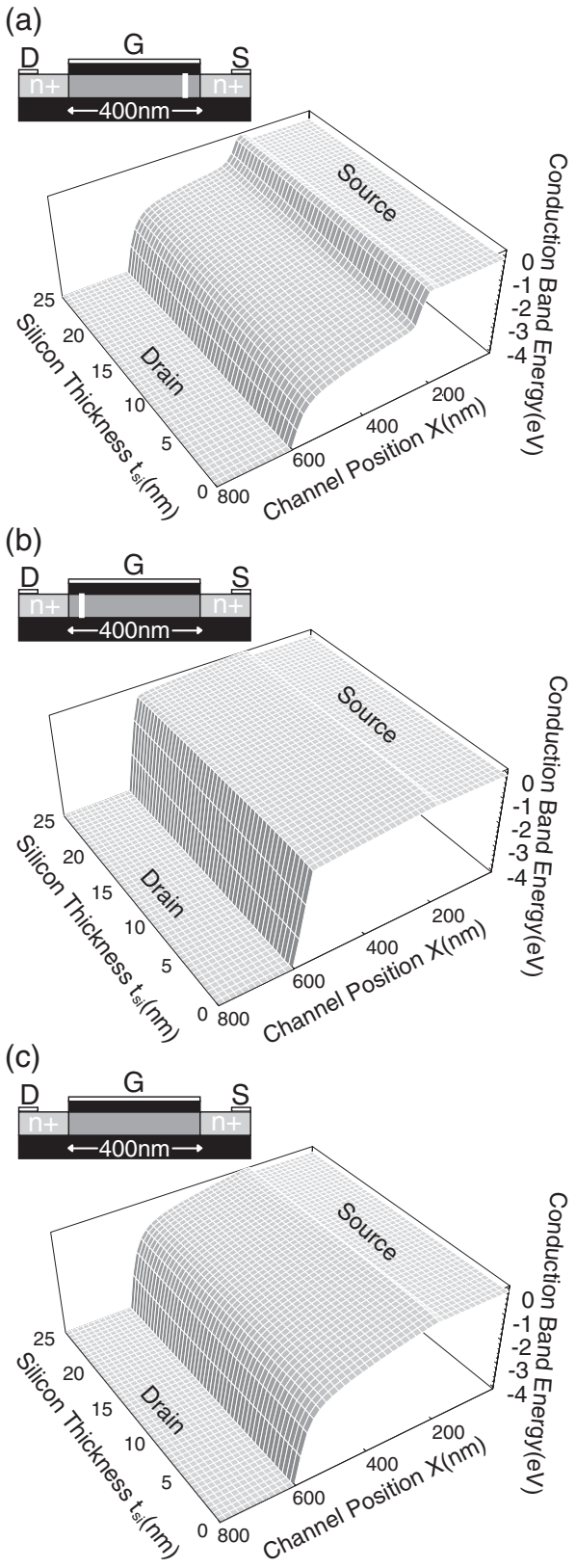

Fig. 5. 2D conduction band profiles at $V_g = V_d = 4\,V$, for a 400 nm TFT with a GB 40 nm from the source (Device A), GB 40 nm from the drain (Device B) and no GB (Device C).

the remaining potential drops across the distance between the GB and the drain.

As most of the potential drops across a small 40 nm region of the channel, we can say that the "effective" channel length has been reduced to approximately this length. The

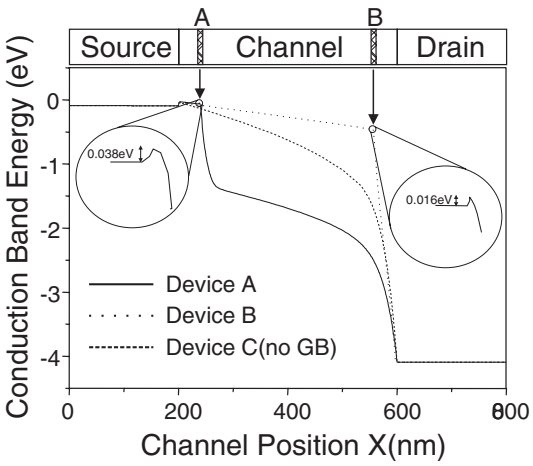

Fig. 6. Cross section of conduction band energy close to the semiconductor interface for a device with a GB 40 nm from the source (Device A), 40 nm from the drain (Device B) and with no GB (Device C).

potential barrier at the GB is much lower (≈ 0.016 eV) than the potential barrier in device A. This can be attributed to the drain induced grain barrier lowering (DIGBL) effect described by Kimura *et al.*[23] Continuing to increase the drain bias will result in a further lowering of the potential barrier on the drain side. This is similar to the DIBL effect in bulk MOSFETs where the drain field extends far enough in the channel that it lowers the barrier to conduction. The effect of lowering the GB barrier is to decrease the threshold voltage which in turn leads to a drain current dependence on drain bias V_d. Both these effects contribute to an enhanced short channel effect, which is the cause of the lack of saturation in the output characteristics.

4. Channel Length Dependence of Output Characteristics

4.1 Sensitivity to GB position

To quantify the lack of saturation when the GB approaches the drain edge, we can use the device parameter output conductance, which is defined as $g_d = \partial I_d/\partial V_d$, where I_d and V_d are the drain current and drain voltage in the "saturation" region respectively. When $V_d > V_{d_{sat}}$ and the device current is saturated, then g_d is equal to zero. Our previous result indicates that we can expect g_d to increase above zero as the GB gets closer to the drain. We plot g_d against the normalized GB position for devices of channel length 400, 200, 100, and 50 nm. Figure 7 shows that, for the 400 nm device, the output conductance only begins to increase as we get very close to its drain edge. However, for shorter channel lengths, g_d increases earlier as it moves towards the drain and to a higher value. Critically, this demonstrates that for deep submicron devices, the output characteristics have a greater sensitivity to the GB position.

4.2 Statistical Fluctuation of g_d with GB position

As discussed in §1 the position of GBs in SPC polysilicon films is not highly controllable and their position in the channel is essentially random. The random nature of the GB position manifests itself as a statistical fluctuation in device parameters and this means that the characteristics can vary from device to device.

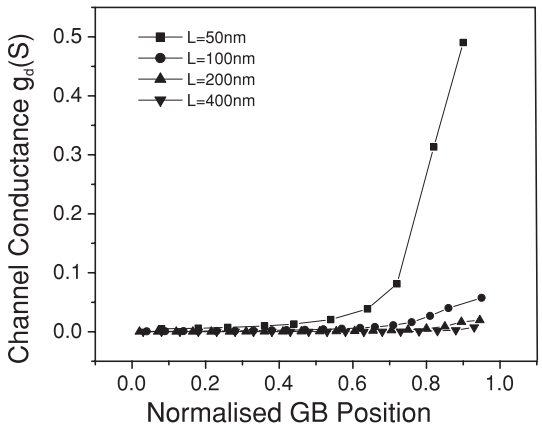

Fig. 7. Output conductance plotted against normalized grain boundary position for channel lengths of 50, 100, 200, and 400 nm.

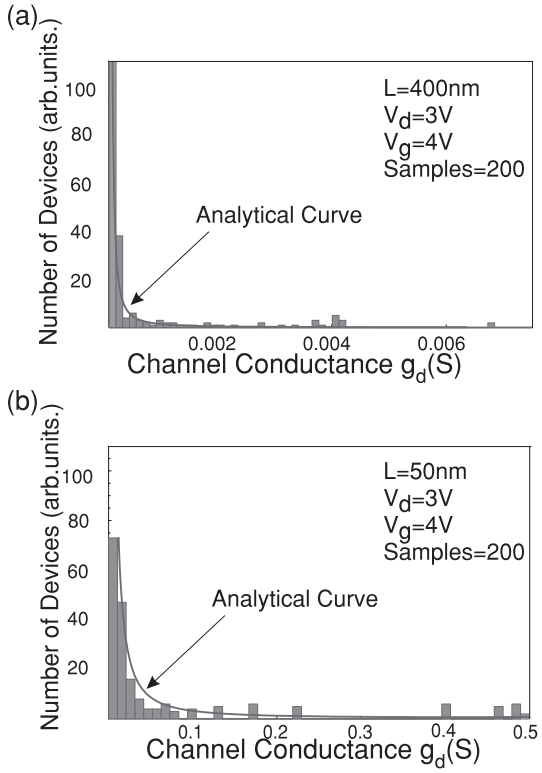

Fig. 8. Overlay of histogram of g_d for 200 samples and analytical distribution curve, for devices of channel lengths of 50 and 400 nm. The spread of the distribution of output conductance is larger for the 50 nm device.

To measure the significance of the fluctuations of output conductance, we set up a series of simulations where the GB position in the channel was random. For each simulated device we extracted g_d at a fixed bias point ($V_d = 3$ V, $V_g = 4$ V). The results for a sample size of 200 devices are shown in Fig. 8 for (a) $L = 400$ nm and (b) $L = 50$ nm. We also derived an analytical expression for the probability density function $p(g_d)$ using a fitting function for g_d against GB position:

$$p(g_d) = \frac{1}{L}\frac{dx(g_d)}{dg_d}, \tag{4.1}$$

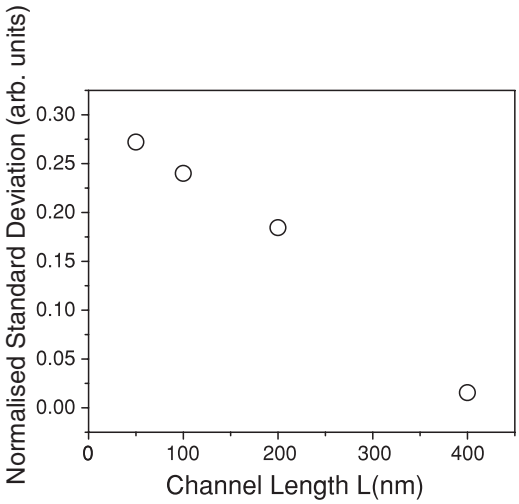

Fig. 9. Normalized standard deviation of output conductance of a sample set of 200 devices plotted against channel length. The standard deviation increases as we decrease L; therefore, devices with shorter channel lengths are more susceptible to statistical variations of g_d.

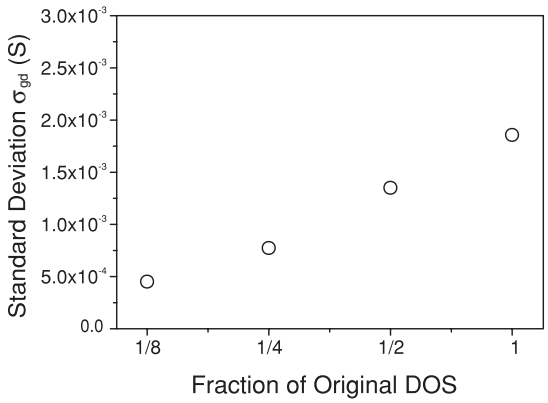

Fig. 10. Normalized standard deviation of output conductance of a sample set of 200 devices plotted against fraction of original density of states. The standard deviation decreases as we reduce the DOS; therefore, devices fabricated in films with a high density of traps at the GB are more susceptible to statistical variations of g_d.

where x is the GB position and L is the transistor length. It was then possible to use eq. (4.1) to calculate an analytical continuous distribution. We show both the derived analytical curve and the histogram from our simulation results in Fig. 8.

Figure 8 shows that for the 50 nm device the spread of the g_d distribution is larger than that for the 400 nm device. This indicates that the size of the device fluctuations are larger in the 50 nm TFT. To quantify this we use the descriptive statistical measure of standard deviation. In Fig. 9 we show a plot of normalized standard deviation vs channel length. It can be noted that the standard deviation increases as channel length decreases. Thereby demonstrating that the statistical fluctuations in output conductance become larger the shorter the channel length.

4.3 Dependence of statistical fluctuation of g_d on density of trap states

As discussed in §2.3, when evaluating the trap density distribution there is still some debate on both the spread and density of trap states. A detailed study is necessary to consider all the distributions that have been suggested in the literature. However, in our study, to give some indication of the dependence of our results on the density of trap states (DOS) we simulated the standard deviation of g_d for a TFT with $L = 400$ nm and then calculated how the standard deviation of g_d changed as we uniformly varied the values of N_{TA}, N_{TD}, N_{GA}, and N_{GD} in our original DOS (Fig. 1). The size of the sample set used in evaluating the standard deviation of g_d was, as used previously, 200 devices.

The simulation result is shown in Fig. 10 and suggests that the sensitivity of g_d to GB position decreases with reduced trap density. This is most likely due the smaller amount of charge trapped at the GB which in turn means less potential dropped across the GB. This indicates that when the trap density is low the reduction in the "effective" channel length would be less severe. Furthermore, it will also limit the maximum barrier height at the GB and therefore limit the DIGBL effect.

5. Conclusions

The dependence of polysilicon TFT output characteristics on GB position has been investigated using two-dimensional (2D) device simulation. We have found that in single GB submicron TFTs, when the GB is close to the drain edge, output current does not saturate; furthermore, the output conductance depends on how close the GB is to the drain.

The effect of positioning the GB close to the drain is two fold. Firstly, the GB potential barrier is lowered by the DIGBL effect; therefore, the drain current is proportional to the drain voltage in the saturation regime. Secondly, as the GB is highly resistive the majority of the potential difference between the source and drain drops across the small distance between the GB and the drain edge. This has the effect of reducing the effective channel length and therefore enhancing short channel effects, that is, reducing the threshold voltage V_T as we increase V_d. Therefore, the closer the GB is to the drain, the smaller the effective channel length and the larger the DIGBL effect.

A further key finding was that as we decreased the channel length, the sensitivity of output conductance to the GB position increased. However, the sensitivity decreased when we reduced the density of traps at the GB. The magnitude of output conductance fluctuations was quantified by calculating the normalised standard deviation as a measure of variations in g_d.

In conclusion, we find that the output characteristics of submicron polysilicon TFTs with a single GB in the channel have a strong dependence on the GB position. The implication for TFT device design is that, as we approach the deca-nanometer regime, it is desirable to control the GB position so that it is not near the drain edge if good output characteristics are to be obtained. If the GB position is not controlled, the fluctuations in g_d will become too large for effective use in three dimensional analog VLSI circuit designs and therefore limit the use of SPC polysilicon as a device material for this application.

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