Charge injection and trapping in silicon nanocrystals

M. A. Rafiq
Microelectronics Research Centre, Cavendish Laboratory, University of Cambridge, Madingley Road, Cambridge CB3 0HE, United Kingdom

Y. Tsuchiya, H. Mizuta, and S. Oda
Department of Physical Electronics, Tokyo Institute of Technology, O-Okayama, Meguro-ku, Tokyo 152-8552, Japan and SORST Japan Science and Technology, Japan

Shigeyasu Uno
Hitachi Cambridge Laboratory, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, United Kingdom

Z. A. K. Durrani[a] and W. I. Milne
Electronic Devices and Materials Group, Engineering Department, University of Cambridge, Trumpington Street, Cambridge CB2 1PZ, United Kingdom and SORST Japan Science and Technology, Japan

(Received 28 March 2005; accepted 21 September 2005; published online 24 October 2005)

The temperature dependence of the conduction mechanism in thin films of ~8 nm diameter silicon nanocrystals is investigated using Al/Si nanocrystal/*p*-Si/Al diodes. A film thickness of 300 nm is used. From 300 to 200 K, space charge limited current, in the presence of an exponential distribution of trapping states, dominates the conduction mechanism. Using this model, a trap density $N_t = 2.3 \times 10^{17}$ cm^{-3} and a characteristic trap temperature $T_t = 1670$ K can be extracted. The trap density is within an order of magnitude of the nanocrystal number density, suggesting that most nanocrystals trap single or a few carriers at most. © *2005 American Institute of Physics*.
[DOI: 10.1063/1.2119431]

In recent years, there has been great interest in silicon nanocrystals prepared by various growth techniques.[1–4] The nanometer-scale size of these crystals leads to novel electronic and optical properties associated with quantum confinement and single-electron charging effects. These properties have been exploited for the fabrication of single-electron transistors and memories,[1,5] electron emitters,[6] and silicon light emitting devices.[7] The possibility of precise control of the nanocrystal size and separation, e.g., by plasma decomposition of SiH_4,[3,7] raises the possibility of large numbers of nanocrystal devices with well defined electrical and optical characteristics.

At present, there are only limited investigations of the macroscopic electronic conduction mechanism across Si nanocrystal films. While electronic transport through single nanocrystals shows strong single-electron charging effects at low temperatures,[8] it is not clear if this occurs in large numbers of nanocrystals. At high bias, it is possible to observe electron emission from thin films of nanocrystals.[6] In investigations of the electrical and electroluminescence characteristics of Si nanocrystals prepared by pulsed laser ablation, a space charge limited current[9] (SCLC) and tunneling conduction mechanism has been suggested.[10] In contrast, there are detailed investigations of carrier transport in porous Si films (which may contain silicon nanocrystals), and in other systems such as CdSe nanocrystals, where SCLC electron transport has been demonstrated explicitly.[11–14]

This letter investigates the macroscopic electronic conduction mechanism across 300-nm-thick Si nanocrystal films with ~8 nm diameter nanocrystals. We measure the temperature dependence of the *I-V* characteristics of Al/Si nanocrystal/*p*-Si/Al diodes from 300 to 40 K. From 300 to 200 K, the conduction mechanism is dominated by SCLC transport, in the presence of an exponential distribution of trapping states. Using this model, we extract a trap density $N_t = 2.3 \times 10^{17}$ cm^{-3} and a characteristic trap temperature $T_t = 1670$ K. The trap density was within an order of magnitude of the nanocrystal number density, suggesting that most nanocrystals trap single or a few carriers at most.

Figure 1(a) shows a schematic diagram of our device. The device uses a ~300 nm thick Si nanocrystal film, deposited by plasma decomposition of SiH_4 (Ref. 1) on a *p*-Si substrate (resistivity: 10 Ω cm). The nanocrystals are 8 nm±1 nm in diameter and undoped, with a ~1.5-nm-thick surface SiO_2 layer, at least for nanocrystals near the film surface. Figure 1(b) shows a scanning electron micrograph of

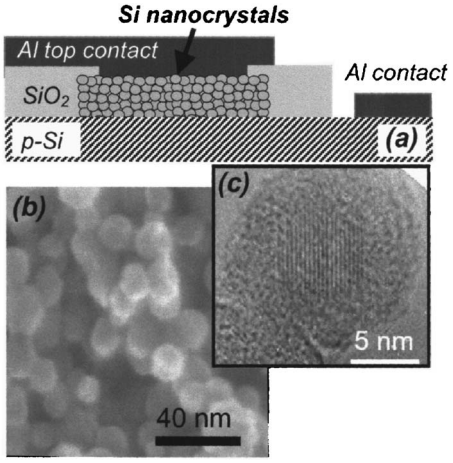

FIG. 1. (a) Schematic of the Al/Si nanocrystal/*p*-Si/Al diode. (b) Scanning electron micrograph of the Si nanocrystal film. (c). Transmission electron micrograph of a Si nanocrystal.

[a]Electronic mail: zakd100@cam.ac.uk

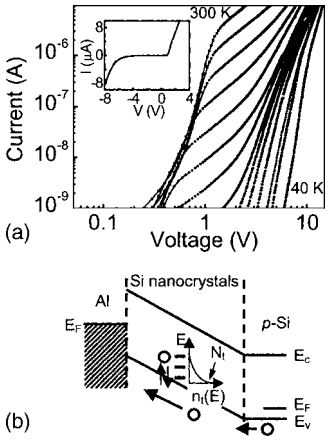

FIG. 2. (a) *I-V* characteristics of a 35 μm$\times$35 μm diode from 300 to 40 K, on a log-log plot. The temperature step is 20 K. The inset shows the *I-V* characteristics at 300 K, from −8 to 4 V, on a linear scale. (b) Schematic diagram of SCLC transport. The SiO_2 potential barriers in the Si nanocrystal film are omitted for clarity. Carriers (holes) are injected from the *p*-Si substrate into the film. An exponential distribution of traps $n_t(E)$ exists in the film.

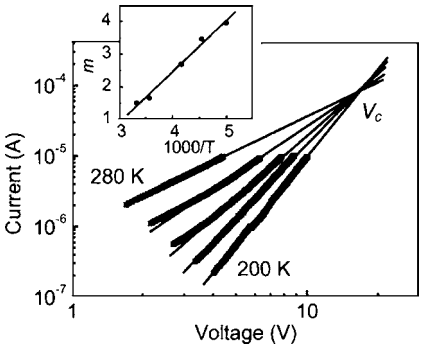

FIG. 3. Power law fits to the data of Fig. 2 from 280 to 200 K, with a temperature step of 20 K. The fits meet at cross over voltage V_c=17 V. The inset shows m as a function of inverse temperature.

our film. Figure 1(c) shows a transmission electron micrograph of a nanocrystal with ~3 nm oxide due to thermal processing (1 h oxidation) before microscopy. The film is nonuniform, with a nanocrystal coverage ~60% per layer and a number density, $N_{nc}\sim 1.2\times 10^{18}/cm^3$. Our film thickness of ~300 nm avoids pinholes across the film. The diodes were defined using "mesas", fabricated by electron-beam lithography and reactive ion etching. A ~150-nm-thick sputtered SiO_2 layer, wet-etched over the mesa to expose the nanocrystals, was used to support an Al top contact. The substrate contact was also in Al. The diode area, determined by the top Al–Si nanocrystal contact area, was varied from 35 μm$\times$35 μm to 200 μm$\times$200 μm. The diode current is seen to scale with device area.

The *I-V* characteristics of a 35 μm$\times$35 μm diode from 300 to 40 K, measured using a cryogenic temperature needle prober (BCT-43MDC, Nagase & Co. Ltd.) and a Hewlett Packard 4156A parameter analyzer, are shown in Fig. 2(a) on a log-log plot. The inset shows the room temperature *I-V* characteristics of the device from −8 to 4 V (linear scale). Here, positive bias is applied to the substrate contact, corresponding to a forward biased substrate. The *I-V* characteristics are asymmetric with voltage [Fig. 2(a), inset]. The rectifying ratio at room temperature, I_F/I_R=450 at $|V|$=2.5 V, and the turn-on voltages for forward and reverse bias are $V_F\sim 0.9$ V and $V_R\sim -6$ V, respectively. We note that the *I-V* characteristic between two substrate contacts is linear at 300 K, with a substrate contact resistance ~100 kΩ. The rectifying nature of the *I-V* characteristics of our device is then due to the *p*-Si/Si nanocrystal/top Al layers. The total resistance at 300 K of the device is ~430 kΩ, above V_F. This includes the ~100 kΩ substrate-contact resistance.

At 300 K, the current above a voltage threshold ~1.2 V increases along a straight line in our log-log plot, corresponding to an $I\propto V^m$ dependence, where $m\approx 1.8$. This behavior persists to ~200 K, but with increasing m from ~1.8 to 4, and increasing voltage threshold, from ~1.2 to ~4 V. The increase in m leads to convergence of the *I-V* characteristics from 300 to 200 K, such that the different curves can be extrapolated to meet at a single point (see Fig. 3). Below 200 K, the curves do not converge towards a single point, and instead tend to a constant slope. For low voltages, e.g., below ~1.2 V at 300 K, the current can be shown to increase exponentially. In order to confirm that the behavior of Fig. 2(a) is due to the Si nanocrystal layer and not due to the *p*-Si substrate, we have also measured the temperature dependence of the *I-V* characteristics between two Al substrate contacts, from 300 to 40 K. These curves show an exponential *I-V* dependence and do not show the dependence of Fig. 2(a). The current in these curves also remains larger than in Fig. 2(a), implying that in our Al/Si nanocrystal/*p*-Si/Al structure, there is a lower resistance for the *p*-Si substrate/Al substrate-contact part than for the top Al contact/Si nanocrystal part. Therefore, the dependence of Fig. 2(a) can be associated with the top Al contact/nanocrystal film.

The characteristics from 300 to 200 K can be explained using a SCLC model with an exponential density of traps.[9,15] Our free carriers are injected from the substrate into transport states in the film [Fig. 2(b)]. An exponential distribution of traps above these states reduces the number of free carriers. With increasing voltage, the Fermi level fall through the distribution, filling the traps and causing a rapid increase in free carriers. Assuming a constant mobility, a free carrier concentration much less than the trapped carrier concentration, an exponential trap distribution, and considering only majority carriers (in our case, holes from the substrate), the current density is[15]

$$J = q^{1-l}\mu_p N_v \left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\frac{\varepsilon_s\varepsilon_0}{N_t}\right)^{l}\frac{V^{l+1}}{d^{2l+1}}. \quad (1)$$

Here, N_t is the trap density, ε_0 is the permittivity of free space, ε_s the dielectric constant, μ_p is the hole mobility, N_v is the density of transport states, d is the sample thickness, and $l=T_t/T$, where T is the measurement temperature and T_t is the characteristic temperature. T_t is related to the characteristic energy of the trap distribution, $E_t=k_BT_t$, where k_B is the Boltzmann constant. Equation (1) predicts a J-V^m dependence, where $m=l+1$. Thus, the slope of a log-log plot of *J-V* directly determines the characteristic temperature and energy.

Figure 3 shows SCLC power law fits to the data of Fig. 2(a) from 280 to 200 K, where the data converges to V_c =17 V and the slopes give the exponent m. The inset shows that m increases linearly as a function of inverse temperature, as predicted by SCLC theory. Here, T_t=1670 K, and E_t =0.14 eV. Below ~200 K, the curves tend to a constant m and the SCLC model does not fit. This is because the thermal

energy is not sufficient to ionize carriers between the traps and the transport states. Carrier transport at these temperatures can occur by hopping conduction.[11,16] In our data at low temperature, the conductance can be shown to follow a $T^{-1/2}$ law, corresponding to variable range hopping with Coulomb interactions.[17]

Equation (1) can be approximated in an Arrenhius form[18]

$$J = \frac{1}{2}\left(\frac{\mu_p N_v q V}{d}\right)\exp\left[-\frac{E_t}{kT}\ln\left(\frac{qN_t d^2}{2\varepsilon_s \varepsilon_0 V}\right)\right], \tag{2}$$

where the activation energy is

$$E_a = \frac{E_t}{k}\ln\left(\frac{qN_t d^2}{2\varepsilon_s \varepsilon_0 V}\right). \tag{3}$$

This relates the slope of the ln*(J)* vs *1/T* curves at constant voltage to the total trap density. An examination of Eq. (2) shows that the current is temperature independent at a "crossover voltage" V_c, where $E_a = 0$ and

$$V_c = \frac{qN_t d^2}{2\varepsilon_s \varepsilon_0}. \tag{4}$$

If the curves of Fig. 2(a) from 300 to 200 K are extrapolated, then it is possible to obtain the crossover voltage V_c. Figure 3 shows this data, with $I \propto V^m$ fits to the data (solid lines) extrapolated to find V_c. Here, $V_c = 17$ V, which gives $N_t = 2.3 \times 10^{17}$ cm^{-3}. In addition, if we plot our data in an Arrenhius plot [ln(I) vs $1/T$], we can directly measure $E_a \sim 200$ meV at a bias of 4 V. This gives $N_t = 2.4 \times 10^{17}$ cm^{-3} [Eq. (3)], which is close to N_t determined from the crossover voltage [Eq. (4)].

Our value of N_t is very similar to the nanocrystal number density, $N_{\mathrm{nc}} \sim 1.2 \times 10^{18}$ cm^{-3}. This suggests that only a few carriers are trapped per nanocrystal. With SCLC, holes are injected from the substrate into the nanocrystal film. A potential well may exist on each nanocrystal, between potential barriers at the nanocrystal surface. Single-electron or quantum confinement effects could then lead to a discrete density of states in the well.[4,8] If the higher charge number states, closer to the top of the potential barrier, were delocalized then only a few localized (trapping) states would exist on a nanocrystal. This would limit the number of carriers trapped in the well and explain our similarity between N_t and N_{nc}. Alternatively, the trapping states may be formed by only a small number of defect states per nanocrystal.

The values of $T_t = 1670$ K (corresponding to $E_t = 0.14$ eV) and $N_t = 2.3 \times 10^{17}$ cm^{-3} can be compared to amorphous Si and to other nanocrystal systems. T_t does not lie in the range observed for bulk amorphous Si ($\sim$300–$\sim$1300 K) or for large ($\sim$150 nm) amorphous Si nanoparticles, and N_t is two orders of magnitude smaller than in amorphous Si.[19,20] Our values of T_t and N_t are more comparable to values observed in CdSe nanocrystals, similar in size to our Si nanocrystals, In CdSe, $T_t \sim 1750$ K, $E_t = 0.15$ eV, and $N_t \sim 10^{16}$–10^{17} cm^{-3}.[13,14] We speculate that our traps may be associated with nanocrystal size. Our ratio $N_{\mathrm{nc}}/N_t \approx 5$ is lower than in CdSe nanocrystals, where a ratio of 100 was observed for deep level traps.[14] This suggests more uniform charging in our Si nanocrystals films.

In conclusion, we investigated the conduction mechanism in 300-nm-thick Si nanocrystal films, with $\sim$8 nm nanocrystals. From 300 to 200 K, we observed SCLC hole transport with an exponential distribution of trapping states, where the trap density was 2.3×10^{17} cm^{-3} and the characteristic trap temperature was 1670 K. The trap density was within an order of magnitude of the nanocrystal number density, suggesting that most nanocrystals trap single or a few carriers at most.

The authors would like to acknowledge useful discussions with Professor H. Ahmed at Corpus Christi College, Cambridge. M.A.R. would like to acknowledge the support of the Cambridge Commonwealth Trust.

[1] K. Yano, T. Ishii, T. Hashimoto, T. Kobauashi, F. Murai, and K. Seki, Appl. Phys. Lett. **67**, 828 (1995).
[2] G. F. Grom, D. J. Lockwood, J. P. McCaffery, N. J. Labbe, P. M. Fauchet, B. White, Jr., J. Diener, D. Kovalev, F. Koch, and L. Tsybeskov, Nature (London) **407**, 358 (2000).
[3] S. Oda and M. Otobe. Mater. Res. Soc. Symp. Proc. **358**, 721 (1995).
[4] T. Kamiya, K. Nakahata, Y. T. Tan, Z. A. K. Durrani, and I. Shimuzu, J. Appl. Phys. **89**, 6265 (2001).
[5] Y. T. Tan, T. Kamiya, Z. A. K. Durrani, and H. Ahmed, J. Appl. Phys. **94**, 633 (2003).
[6] K. Nishiguchi, X. Zhao, and S. Oda, J. Appl. Phys. **92**, 2748 (2002).
[7] Y. Kanemitsu, S. Okamoto, M. Otobe, and S. Oda, Phys. Rev. B **55**, R7375 (1997).
[8] A. Dutta, S. Oda, Y. Fu, and M. Willander, Jpn. J. Appl. Phys., Part 1 **39**, 4647 (2000).
[9] M. A. Lampert and P. Mark, *Current Injection in Solids* (Academic, New York, 1970)
[10] T. A. Burr, A. A. Seraphin, E. Werwa, and K. D. Kolenbrander, Phys. Rev. B **56**, 4818 (1997).
[11] M. Ben-Chorin, F. Moller, and F. Koch, Phys. Rev. B **49**, 2981 (1994).
[12] C. Peng, K. D. Hirschman, and P. M. Fauchet, J. Appl. Phys. **80**, 295 (1996).
[13] D. S. Ginger, and N. C. Greenham, J. Appl. Phys. **87**, 1361 (2000).
[14] R. A. M. Hikmet, D. V. Talapin, and H. Weller, J. Appl. Phys. **93**, 3509 (2002).
[15] P. Mark and W. Helfrich, J. Appl. Phys. **33**, 205 (1962).
[16] D. Yu, C. Wang, B. L. Wehrenberg, and P. Guyot-Sionnest, Phys. Rev. Lett. **92**, 216802 (2004).
[17] B. I. Shklovskii and A. L. Efrose, *Electronic Properties of Doped Semiconductors* (Springer, Berlin, 1984).
[18] V. Kumar, S. C. Jain, A. K. Kapoor, W. Greens, T. Aernauts, J. Poortmans, and R. Mertens, J. Appl. Phys. **94**, 1283 (2003).
[19] Z. Shen, U. Kortshagen, and S. A. Campbell, J. Appl. Phys. **96**, 2204 (2004).