Nanosilicon for single-electron devices

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Abstract

This paper presents a brief overview of the physics of nanosilicon materials for single-electron device applications. We study how a nanosilicon grain and a discrete grain boundary work as a charging island and a tunnel barrier by using a point-contact transistor, which features an extremely short and narrow channel. Single-electron charging phenomena are investigated by comparing as-prepared devices and various oxidized devices. The optimization of grain and grain-boundary structural parameters is discussed for improving the Coulomb blockade characteristics and realizing room temperature device operation.

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1. Introduction—why nanosilicon?

The progress of nanofabrication technologies over the last two decades as allowed us to explore a new research field of single electronics [1]. Single-electron charging or ‘Coulomb blockade (CB)’ phenomena are expected to appear in semiconductor nanostructures and have been adopted as a new principle for manipulating a small number of electrons. Both for memory and logic applications, single-electron devices (SEDs) have been studied intensively to overcome the inherent scalability issue of the conventional CMOS devices. A key building block for SEDs is the multiple tunnel junction (MTJ), which is composed of multiple tunnel barriers and electron islands. As a general guideline, the MTJ should meet the following two requirements to show the CB effects at a temperature $T$:

$$R_t \gg R_Q = \frac{h}{e^2} = 25.6 \text{ k}\Omega,$$

$$E_C = \frac{e^2}{2C_R} \gg k_B T$$

To avoid quantum and thermal smearing of the electronic states confined in the electron islands. In Eqs. (1) and (2) $R_Q$ is the quantum resistance, $R_t$ is the zero-bias tunnel resistance of the (generally nonlinear) current-voltage characteristic of a tunnel junction, $E_C$ is the charging energy, and $C_R$ is an island capacitance.

A number of fabrication methods of MTJs have been reported based on crystalline silicon. These structures may be classified into two groups in terms of the manner of defining electron islands: patterned electron islands and naturally formed ones. A patterned electron island with a lateral size of less than 10 nm has been realized by using a pattern-dependent oxidation (PADOX) technique [2]. This technique utilizes an increase in a band gap due to quantum confinement in an ultranarrow channel and a decrease in a band gap due to compressive stress in the channel after oxidation process.
2. Single-electron charging phenomenon in nanosilicon

The macroscopic properties of the poly-Si film with large Si grains have been studied extensively for the development of thin film transistors and static random access memories, and various process techniques have been established to increase the grain size and to improve carrier mobility. However, the microscopic properties of individual nanoscale grains and discrete GBs have not been studied in detail. In this work, we adopt a point-contact transistor (PC-Tr) [13], which has a channel with both the length $L$ and width $W$ as small as the grain size $L_{\text{grain}}$ of the nano/poly-Si film. The electric characteristics for the PC-Trs must therefore reflect the properties of individual grains and GBs contained in the channel. Fig. 1 shows an SEM image of a PC-Tr fabricated in a 50-nm thick SPC poly-Si film. The inset (a) to Fig. 1 is a SEM image of a Secco-etched poly-Si film that shows the individual grains and GBs. From the SEM observation it was found that $L_{\text{grain}}$ in this particular film ranges from 20 to 150 nm. PC-Trs with $W$ and $L$ from 20 to 50 nm were patterned by high-resolution e-beam lithography and electrically isolated by reactive ion etching. Electrical characterization was performed for both as-prepared PC-Trs and those oxidized at 1000 °C for 15 min in dry O$_2$ ambient. An effective potential barrier height $qV_B$ of GBs was extracted from a temperature dependence of the $I_{\text{ds}}-V_{\text{gs}}$ characteristics at between 200 and 300 K using the thermionic emission model.

The as-prepared PC-Trs [13] did not show any Coulomb oscillation at temperatures above 4.2 K. From the TEM observation of grain structures, the tunnel capacitance $C_{\text{tunnel}}$ between two adjacent grains was estimated to be larger than 80 aF. In addition, the tunnel resistance $R_t$ was evaluated to be similar to $R_Q$. Therefore both $E_C$ and $R_t$ are not sufficiently large to observe the CB effect even at cryogenic temperatures. The barrier height $qV_B$ extracted for the as-prepared PC-Trs, ranges from 30 to 80 meV.

In contrast, most of the oxidized PC-Trs show a clear Coulomb oscillation in the $I_{\text{ds}}-V_{\text{gs}}$ curves and a Coulomb

![Fig. 1. SEM image of an as-prepared PC-Tr. The insets (a) and (b) show the grain structure of the poly-Si film and a blow-up of the channel region, respectively.](image-url)
gap $V_T$ in the $I_{ds}$–$V_{ds}$ characteristics associated with the CB effect [14]: Fig. 2(a) and (b) show the $I_{ds}$–$V_{ds}$ and $I_{ds}$–$V_{gs}$ characteristics for one of the oxidized PC-Trs. In the oxidized PC-Trs, the poly-Si film thickness decreased down to approximately 18 nm after the oxidation process [16]. This leads to a decrease in $C_{\text{tunnel}}$ and consequently increases $E_C$. Although an increase in the mean $qV_B$ was just 5 meV for the oxidised PC-Trs, $R_t$ was found to be by more than two orders of magnitude larger after the oxidation treatment because the GBs were oxidized effectively [17] and converted to suboxide. Both the increased $E_C$ and $R_t$ result in the appearance of the CB effect. The GB tunnel barrier thickness $d$ was estimated to be approximately 3 nm for the oxidized PC-Tr using a tunneling current calculation and observed value of $R_t$. This is consistent with high-resolution TEM observation, which reveals that GBs were oxidized faster than crystalline grains and that some silicon suboxide layers were as thick as 2–3 nm. The lateral dimensions of the grain that acts as the charging island were evaluated to be about 3 nm×10 nm by using a two-dimensional capacitance calculation and the observed $V_T$ and Coulomb oscillation period $\Delta V_{gs}$.

## 3. Material optimisation towards room-temperature nanosilicon single-electron devices

It was found from all the oxidized samples that both the $P/V$ ratio and $V_T$ increase with $R_t$ and that a good $P/V$ ratio is observed when the total zero-bias tunnel resistance of the device is over 1 MΩ [14]. If we assume $L_{\text{grain}} \cdot W \approx 3$ nm and $d \cdot 1$ nm, a simple calculation [15] shows that $qV_B$ should meet the following condition:

$$qV_B \cdot 260 \text{ meV} \cdot (10k_B T).$$

Regarding the grain size, it is apparent that decreasing $L_{\text{grain}}$ further is needed to reduce $C_{\text{t}}$. For this purpose a nc-Si film prepared by a low-temperature VHF PECVD [7] was adopted instead of the SPC poly-Si film. A 20 nm thick nc-Si:H film was prepared from a SiF$_4$:H$_2$:SiH$_4$ gas mixture at temperatures $\leq$300 °C. From TEM observation it was found that the film contains grains with $L_{\text{grain}}$ from 4 to 8 nm uniformly distributed in a-Si:H matrix (Fig. 3(a)).

After defining the PC-Trs in the same manner, a multiple step oxidation process was applied, which was proposed to oxidize the a-Si:H selectively and to convert it to SiO$_x$ ($x < 2$) without increasing $L_{\text{grain}}$ [17,18]. This is low-temperature oxidation (650–750 °C) followed by high-temperature (1000 °C) annealing. A cross-sectional TEM showed that the grains remained the same in size despite the fact that the overall film thickness was reduced by 6 nm due to surface oxide formation. $qV_B$ extracted for the multi-step oxidised nc-Si PC-Tr with $L = W = 20$ nm was as high as 173 meV while that for the as-deposited nc-Si PC-Trs was only about 40 meV.

A clear CB oscillation was observed for the multi-step oxidised nc-Si PC-Trs: the $I_{ds}$–$V_{gs}$ characteristics observed for the device with $L = W = 20$ nm is shown in Fig. 3(b) [19]. The oscillation with an unchanged period persists up to room temperature although the $P/V$ current ratio is gradually decreased as the temperature
increases as shown in the inset to Fig. 4, and that for room temperature is still far too small for any kinds of device application. From a simple capacitance calculation combined with the observed $\Delta V_{gs}$ and $V_T$, $L_{\text{gran}}$ was estimated to be about 8 nm for this nc-Si PC-Tr, which is in good agreement with the TEM observation.

Even further reduction of $L_{\text{gran}}$ is needed for realising room temperature SED operation. To provide a more quantitative guideline, the charging energy $E_C$ and quantum confinement energy $E_K$ were calculated as a function of nc-Si dot diameter. $E_C$ was calculated for a Si sphere embedded in oxide taking account of both self-capacitance and tunnel capacitance \[20\]. $E_K$ was obtained numerically as the energy of the lowest quasi-bound state of an intrinsic Si quantum well with 2-nm-thick oxide barriers: tunnel barrier heights of 3.0 and 0.26 eV (Eq. (3)) were used for SiO$_2$ and SiO$_x$ barriers. Fig. 4 shows the dot diameter dependence of $E_C$ (a light grey solid line), $E_K$ calculated for both SiO$_2$ and SiO$_x$ (dotted lines) barriers and the corresponding total electron addition energies $E_Z$ (black and dark grey solid lines). Because of the finite tunnel barrier heights, $E_K$ approaches its maximum with decreasing dot diameter. A region of a diameter ranging from 4 to 8 nm, which corresponds to the nc-Si film used above, is indicated as a shaded region. Two horizontal broken lines show the energy of 10$k_B T$ with $T = 300 \text{ K}$ and $T = 77 \text{ K}$. These results indicate that $L_{\text{gran}} < 2 \text{ nm}$ is needed to meet $E_Z > 10k_B T$ at room temperature, and to secure SED operation at room temperature, a further development is still needed towards 1-nm-scale size control of nanosilicon dots. However, in this region, the single-electron charging phenomenon in the nanosilicon material can certainly be a way of modulating current substantially at room temperature, and it is then important to develop new device structures that can operate based on the single-electron charging phenomenon combined with other mechanisms of controlling flow of electrons, such as the external electrostatic potential, tailored energy potential barriers \[21\], and energy quantization.

4. Summary

Nanosilicon has been investigated as a promising material for SEDs. We have shown that control of microscopic properties of GBs as a tunnel barrier is essential to improve CB characteristics by comparing as-prepared and oxidised PC-Trs fabricated using the SPC poly-Si film and the PECVD nc-Si film. We have found that $qV_B$ should be as large as $10k_B T$, and $L_{\text{gran}}$ should decrease down to less than 2 nm for any practical device applications at room temperature.

References