Tel. No.: 81-45-924-5357
Fax No.: 81-45-924-5339
e-mail: tkamiya@msl.titech.ac.jp

# Effects of Oxidation and Annealing Temperature on Grain Boundary Properties in Polycrystalline Silicon Probed Using Nanometre-Scale Point-Contact Devices

Toshio Kamiya[1,2,4], Yoshikazu Furuta[2,3], Yong-Tsong Tan[1,3], Z. A. K. Durrani[1,3], Hiroshi Mizuta[2,3] and Haroon Ahmed[1,3]

[1]Microelectronics Research Centre, University of Cambridge, Madingley Road, Cambridge CB3 0HE, United Kingdom

[2]Hitachi-Cambridge Laboratory, University of Cambridge, Madingley Road, Cambridge CB3 0HE, United Kingdom

[3]CREST, JST, 3-13-11 Shibuya, Tokyo 150-0002, Japan

[4]Materials and Structures Laboratory, Tokyo Institute of Technology, 4259 Nagatsuta, Yokohama 226-8503, Japan

**Keywords**: Polycrystalline silicon nanowire, oxide tunnelling barrier, single-electron charging effects, selective oxidation, grain boundary

**Abstract.** We discuss a method to fabricate single-electron transistors targeted at high-temperature operation. Natural nanostructure in polycrystalline silicon was utilised for charging islands and its grain boundaries were modified by a multi-step annealing technique to form grain-boundary tunnelling barriers. The effects of oxidation and annealing temperature on individual grain boundary properties were investigated using point-contact devices. It is found that low temperature oxidation selectively oxidises the grain boundaries but does not affect carrier transport significantly. Subsequent annealing increases the grain-boundary tunnelling barrier height and resistance. In addition, their distribution is narrowed by optimizing the annealing condition.

## Introduction

A single-electron transistor (SET) is a novel device where the on-off states can be formed by a single-electron, without any statistical fluctuation in electron number[1,2,3]. To realize practical single-electron circuits, it is vital to control tunnelling barrier properties. For example, total tunnel resistance ($R_T$) should be less than ~1 GΩ if a single-electron is transferred at 1 GHz at the source-to-drain voltage ($V_{ds}$) of 1 V. In addition, an $R_T$ value should be much larger than the quantum resistance ($h/e^2$=26kΩ) to avoid the quantum smearing[2]. Furuta et al. report that an $R_T$ value > 1 MΩ is required to obtain a large on-off ratio[4]. To suppress a leakage current at room temperature (RT), a charging energy ($E_c$) must be much larger than thermal energy $k_B$T. Saitoh et al. indicate that an $E_c$ value greater than 10 $k_B$T (260 meV at RT) is favourable[5]. If a tunnelling barrier is made of 1-nm-thick $a$-$SiO_2$, this condition corresponds to the cross-section area as small as 3 nm × 3 nm. Tunnel resistance calculation[6] suggested that we have to fabricate a very thin (<

0.6 nm) tunnelling barrier if its height is as large as 3 eV, which is expected for the *c*-Si/*a*-$SiO_2$ junction. Figure 1 indicates that a realistic tunnel barrier may be ~ 1 nm in thickness and 0.26-1.2 eV in height.

It is not easy to form such small charging islands and thin tunnelling barriers by lithography techniques only. A promising idea to overcome these requirements is to use a naturally-formed nanostructure in a material, which includes very thin polycrystalline silicon (poly-Si)[7] and hydrogenated nanocrystalline silicon[8,9], where crystalline silicon grains work as charging islands and GBs work as tunnelling barriers. However, in general, the properties of individual GBs vary significantly, and it is difficult to control GB properties to conform the above guidelines.

This article discusses a method to control GB tunnelling barrier properties in poly-Si. The effects of oxidation and thermal annealing on electrical properties of individual GBs were examined using nanometre-scale point-contact (PC) devices. We propose a multi-step annealing technique, which is consisted of two or more oxidation and subsequent annealing processes. This technique can separate the incorporation of oxygen in GBs and the modification of their properties temporary, providing better controllability for GB properties.

## Experimental

Our poly-Si film was prepared by solid-phase-crystallization of a 50-nm-thick amorphous silicon at 850 $^{o}$C for 30 min[4]. The films were doped *n* type to $10^{20}$ / $cm^3$ using phosphorus ion-implantation. Transmission electron microscopy (TEM) indicated that the grains were columnar with lateral sizes from 20 nm to 150 nm. PC structures (30 nm wide and 40 nm long) with double side-gates were fabricated to investigate the local carrier transport properties (Fig. 2). The PC structures were defined by electron-beam lithography in PMMA resist, followed by reactive-ion-etching in a 1:1 plasma of $SiCl_4$ and $CF_4$[10].

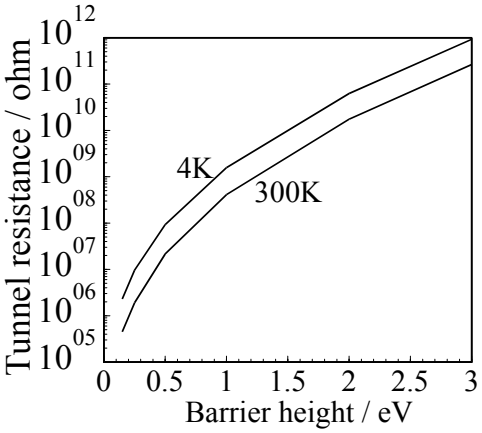


Fig.1: Tunnel resistance as a function of barrier height. Cross-section area is 3nm x 3nm, carrier density is $10^{20}$ /$cm^3$, and barrier thickness is 1 nm.

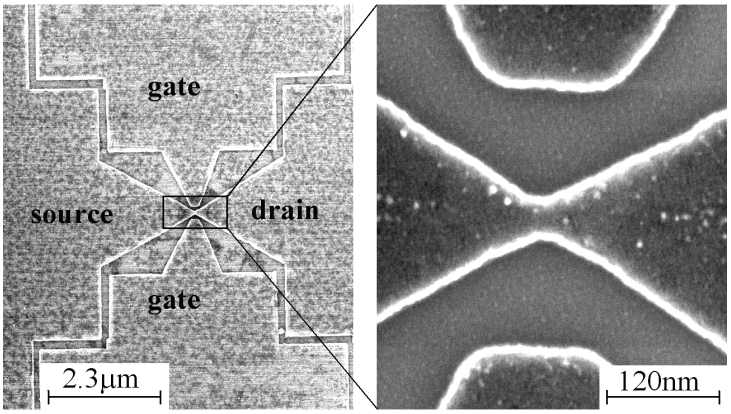


Fig.2: Scanning-electron microscope images of a PC device. Channel size is 30 nm wide and 40 nm long.

As-prepared, oxidised, or oxidised and subsequently thermally annealed (designated as 'oxidised&annealed') PCs were investigated. The thermal treatments were performed after the fabrication of the PC structures. The oxidation was performed in a dry $O_2$ ambient at 650 $^oC$ – 750 $^oC$ for 1 hr, or at 1000 $^oC$ for 15 min. All the samples were dipped in a HF solution before oxidation. The annealing was performed in an argon ambient at 1000 $^oC$ for 15 min after the oxidation. The electrical characteristics were measured at 25 K - 300 K to extract activation energy ($E_a$) and $R_T$ values.

**Results and Discussion**

We found that 30% of as-prepared PCs exhibited non-linear source-to-drain current-voltage ($I_{ds}$-$V_{ds}$) characteristics while rest PCs exhibited linear characteristics in the whole temperature range from 25 K to 300 K. Figures 3(a) show the $I_{ds}$-$V_{ds}$ characteristics of a typical as-prepared PC that exhibits non-linear characteristics. The $I_{ds}$-$V_{ds}$ characteristics agree well with a thermiomic emission model, expressed as eq. (1)[11], if temperature is greater than 120 K.

$$I(V) = 2qn_P\left(\frac{k_BT}{2\pi m^*}\right)^{1/2}\exp\left(-\frac{qV_B}{k_BT}\right)\sinh\left(-\frac{qV}{2nk_BT}\right) \qquad (1)$$

, where $q$ denotes a carrier charge, $m^*$ an effective mass, $k_B$ the Boltzmann constant, $V_B$ a barrier height, $T$ temperature, $n$ number of grain boundaries, and $V$ an applied voltage. At lower temperatures, we can see a significant deviation between the data measured and fitted (see data measured at 25 K). As the conductivity is almost independent of temperature in this low temperature range (Fig. 3(c)) and the poly-Si film is heavily doped, we attribute the carrier transport mechanism to tunnelling.

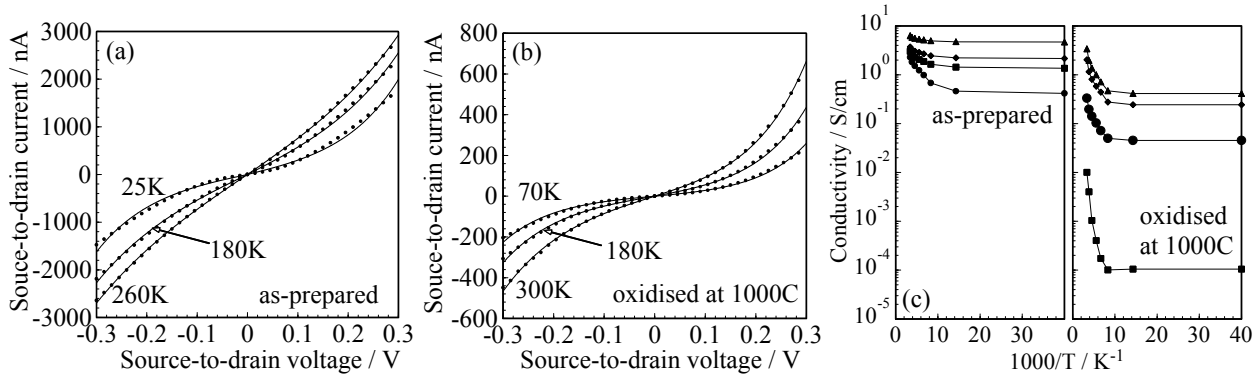


Fig.3: $I_{ds}$-$V_{ds}$ characteristics of as-prepared (a) and oxidised (b) PCs. Oxidation condition was 1000$^o$C for 15 min. Circles show measured data and solid lines show simulation results fitted to eq. (1). Measurement temperatures are indicated. Figure (c) shows the temperature dependence of the device conductivity.

The $I_{ds}$-$V_{ds}$ characteristics of the PCs oxidised at 1000$^o$C also exhibit deviation from eq. (1) at low temperatures less than 260 K (Fig. 3(b)). As we did not observe single-electron charging effects in these devices at > 25 K and the device conductance does not depend on temperature (Fig. 3(c)), this deviation may be attributed to the tunnel conduction through oxidised tunnelling barriers. In

contrast, carrier transport can be explained by the thermiomic emission at > 260 K. The transition temperature tends to be larger for the oxidised PCs than for the as-prepared PCs, probably because the oxidised tunnelling barrier has higher potential barrier.

Some oxidised PCs exhibit single-electron charging effects at 4.2 K. The $I_{ds}$-$V_{ds}$ characteristics has zero-current region at low $V_{ds}$ and is modulated periodically by a gate bias ($V_{gs}$) (Fig. 4(a)), which are the characteristics of single-electron charging phenomena[2]. It is further confirmed from the source-to-drain conductance oscillation observed in the $I_{ds}$-$V_{gs}$ sweep (Fig. 4(b)). We found that the charging island is made of crystalline grains covered by an oxide GB barrier[4].

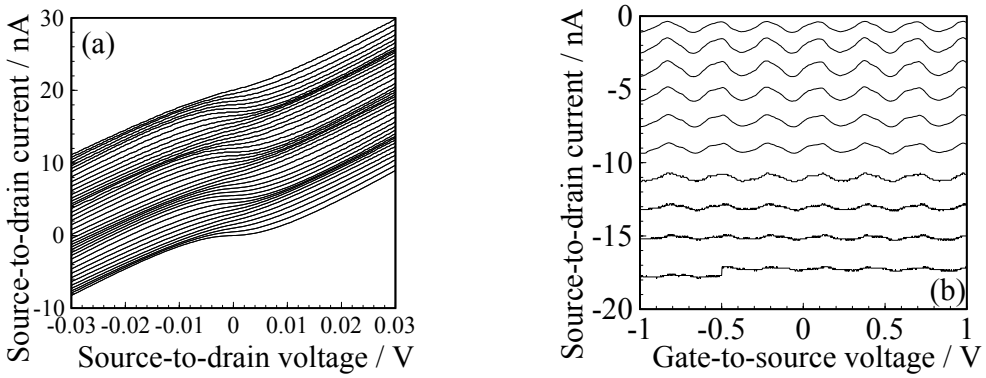


Fig.4: Single-electron charging effects in an oxidised PC measured at 4.2 K. (a) $I_{ds}$-$V_{ds}$ characteristics at $V_{gs}$ ranging from -0.5 V to 0.5 V, and (b) $I_{ds}$-$V_{gs}$ characteristics at $V_{ds}$ ranging from -5 to -50 mV. Oxidation was performed at 1000°C for 15 min.

Equation (1) indicates that we can extract GB potential barrier height ($V_B$) as an activation energy ($E_a$) estimated from the slope of the conductivity in the temperature range where carrier transport is controlled by the thermiomic emission. The $E_a$ value distributes in the range from 6 meV to 20 meV for as-deposited PCs. It is increased to 40-170 meV by the oxidation at 1000°C. We should notice that the typical $E_a$ values in the oxidised PCs, < 60 meV, are too low for a *c*-Si/*a*-$SiO_2$ junction. In addition, such low barriers do not conform our guideline described in introduction.

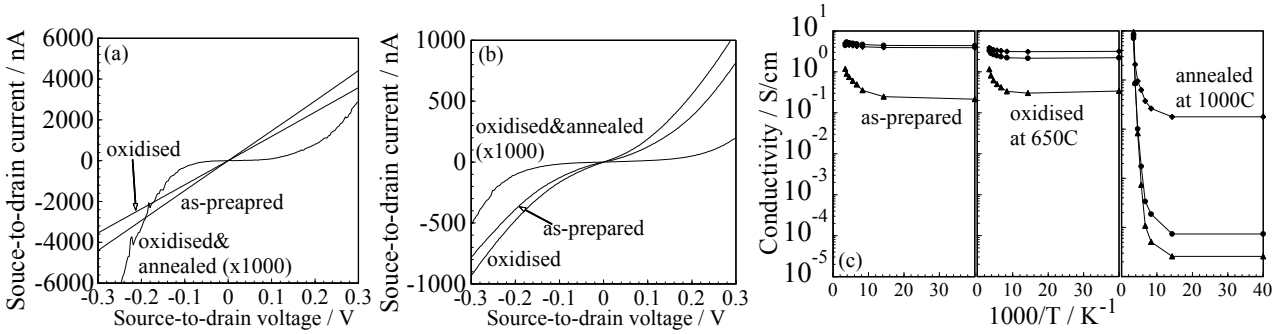


Fig.5: (a,b) $I_{ds}$-$V_{ds}$ characteristics of two typical PCs for as-prepared, oxidised at 650°C, and oxidised&annealing devices, measured at 25 K. (c) shows the temperature dependence of the device conductivity.

Therefore, we surveyed the effects of oxidation and annealing temperature on the electrical properties of PCs. If we oxidise PCs at 650°C, the device conductance is decreased slightly (Fig. 5(a,b)), which can be understood simply that the poly-Si film thickness is reduced by the oxidation

of the superficial silicon layer. In contrast, if the oxidised PCs were annealed at 1000°C, all the PCs exhibit strong non-linear characteristics especially at 25 K. Figure 5(c) shows more clearly that the device conductance is not affected largely by the simple oxidation at 650°C, while it is significantly reduced by the thermal annealing. We can estimate the $R_T$ value from the device resistance at a temperature where the carrier transport is controlled by the tunnelling. Comparing Figs. 3(c) and 5(c), we can see that larger $R_T$ values are obtained for the 650°C-oxidised&annealed PCs than for the 1000°C-oxidised PCs. Note that the $E_a$ and $R_T$ values show a wide distribution.

More advanced multi-step annealing process composed of two-step oxidation and subsequent annealing improves the distribution of GB properties (Fig. 6). Here, PCs were first oxidised at 650°C for 1hr, followed by oxidation at 750°C for 1hr. Similar to the 650°C oxidation case, simple oxidation does not change the electrical characteristics largely. In contrast, the device conductivity is significantly reduced to ~$10^{-8}$ S/cm after the subsequent annealing. It would be noteworthy that the distribution of $E_a$ and $R_T$ values is much narrower than the above cases.

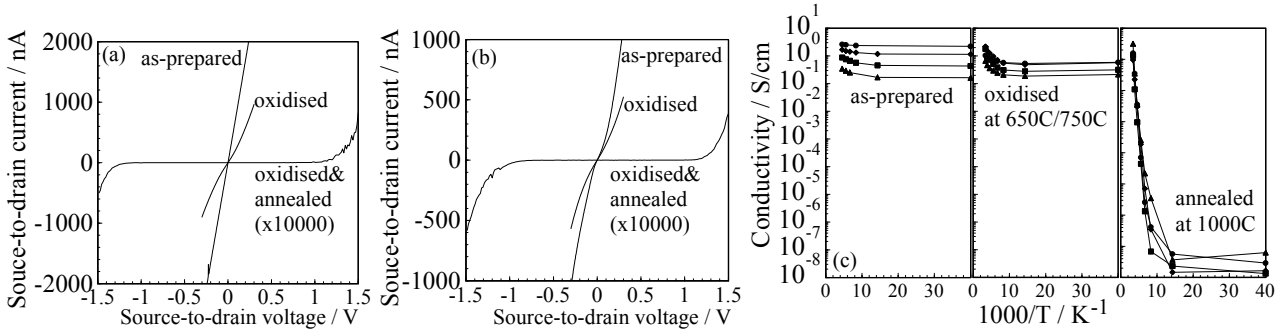


Fig.6: (a,b) $I_{ds}$-$V_{ds}$ characteristics of two typical PCs for as-prepared, two-step oxidised at 650°C and 750°C, and oxidised&annealed devices, measured at 25 K. (c) shows the temperature dependence of the device conductivity.

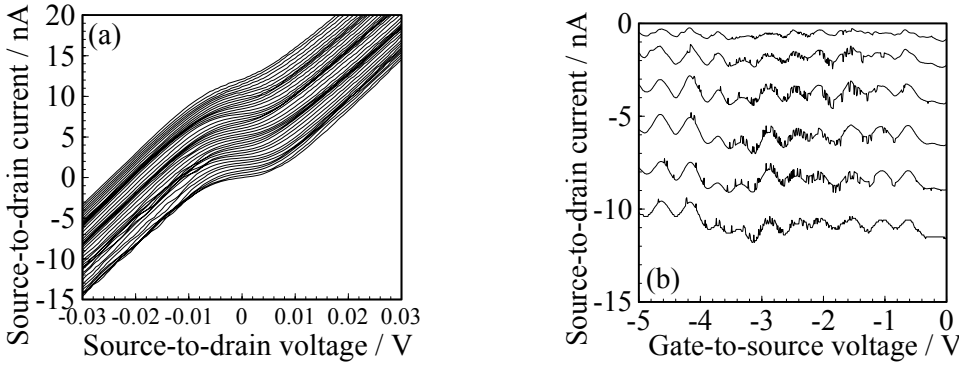


Fig.7: Single-electron charging effects in an oxidised&annealed poly-Si SET at 4.2 K. (a) $I_{ds}$-$V_{ds}$ characteristics at $V_{gs}$ ranging from -2 V to 0 V, and (b) $I_{ds}$-$V_{gs}$ characteristics at $V_{ds}$ ranging from –44 mV to –4 mV. The device was first oxidised at 650°C for 1hr and 750°C for 1hr, followed by thermal annealing at 1000°C for 15 min.

We examined the mechanism of the modification of the GB properties by the multi-step annealing using secondary-ion mass spectroscopy[12]. Simple oxidation diffuses oxygen atoms into the GBs together with the formation of a surface oxide. This does not form silicon oxide at the GBs with a tunnelling barrier high enough to effect conduction. However, subsequent annealing induces local structure reconfiguration in the oxidised GBs as reported in silicon sub-oxide[13], where the high-temperature annealing converts some parts of silicon-rich bonding structure Si-$Si_{4-n}O_n$ (n<4) to

a $Si\text{-}O_4$ tetrahedral structure. Thus the oxidised&annealed GBs would be a mixture of $Si\text{-}O_4$ and silicon-rich structures, which may have moderately high tunnelling barriers if we choose an appropriate annealing condition. It was also confirmed that the oxidation at low temperatures such as 650$^{o}$C improves the selectivity of GB oxidation because the GB oxygen diffusion proceeds relatively faster than the surface oxidation at a lower temperature[12].

The PC device subjected to the multi-step annealing exhibits the single-electron charging effects (Fig. 7), similar to the PC oxidised at 1000$^{o}$C in Fig. 4, demonstrating that the electrons are confined onto charging islands by the tunnelling barriers thus formed.

## Summary

The effects of oxidation and annealing temperature on electrical properties of individual GBs in poly-Si were investigated. Low temperature oxidation selectively oxidises the GBs but does not affect carrier transport significantly. Subsequent annealing increases the potential barrier height and resistance, and narrows their distribution. Single-electron charging effects were observed when PCs were subjected to a multi-step annealing, demonstrating the formation of tunnelling barriers. We expect that the multi-step annealing technique provides a better way to obtain desirable GB properties for poly-Si SETs.

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