Switching of Single-Electron Oscillations in Dual-Gated Nanocrystalline Silicon Point-Contact Transistors

Mohammed A. H. Khalafalla, Hiroshi Mizuta, *Member, IEEE*, and Zahid Ali Khan Durrani

***Abstract*—Switching of single-electron transport is observed in point-contact transistors fabricated in nanocrystalline silicon thin films, where the grain size is ∼10 to 40 nm. The effects may be associated with electrostatic coupling between the grains. At 4.2 K, single-electron oscillations in the device current are switched as a function of the voltages on two separate gates. This is investigated further using single-electron Monte Carlo simulation of a model with two charging grains in parallel and intergrain capacitive coupling. A change in the electron number of a grain occurs due to charging of the other grain by a single electron, causing bistable regions in charge stability versus gate voltage. These effects depend not only on the coupling capacitance but also on the cross capacitances between the grains and the two gates.**

***Index Terms*—Coulomb-blockade, nanocrystalline silicon, quantum dot, single-electron transistor.**

I. Introduction

NANOCRYSTALLINE SILICON (nc-Si) thin films are promising materials for the development of advanced LSI compatible quantum-dot and single-electron charging devices [1]–[3]. The films consist of nanometer-scale grains of crystalline silicon, separated by amorphous silicon or silicon dioxide grain boundaries (GBs) up to a few nanometer thick [4], [5]. The very small size of the grains leads to large electron-confinement and single-electron charging energies [6] and forms naturally a system of quantum-dots (QDs) over a large area without the need for high-resolution lithographic definition of the dots. The small grain size also makes the films extremely promising for the fabrication of quantum-dot and single-electron transistors (SETs) operating at room-temperature [7], [8]. In addition, the local electronic transport properties of the nc-Si at the single grain and GB level are of interest not only for quantum devices but also in improving the performance of scaled thin-film transistors [9].

The close proximity of the grains in nc-Si raises the possibility of strong modulation of the electronic transport by electrostatic coupling and electron wave-function interactions between multiple grains. Similar effects have been investigated in detail at low temperature in double QDs defined lithographically in GaAs/AlGaAs heterostructure material, coupled in series [10], [11] or in parallel [12], [13], and in SiGe double QDs coupled in series [14], [15]. These devices use gate electrodes coupled independently to the QDs, and the electrostatic coupling between the QDs leads to a charge stability diagram with hexagonal regions of constant electron number on the QDs as a function of the two gate voltages [10]. In addition, at mK temperatures, the overlap between the quantum wave-functions of the electrons in the QDs can form covalent molecular-like states [11].

In this paper, we report the observation of intergrain electrostatic coupling effects in single-electron transport through nc-Si. We observe switching of the single-electron current oscillations in nanometer-scale point-contact SETs at 4.2 K, as a function of the voltage applied to two independent gates. These effects can be associated with electrostatic coupling between two dominant grains in the point-contact. Due to the different capacitance between each gate and grain, the electron number of each grain changes differently with the gate voltages, and the effect of electrostatic coupling between the grains is observed in a charge stability diagram. We investigate these effects further using single-electron Monte Carlo simulation and propose a double QD model where a change by even one electron in the charge of a grain near the single-electron transport path switches the electron transport. Regions of bistability exist in the charge stability diagram, where the electron number of both QDs changes within small ranges of gate voltage. We attribute this to the addition of the cross capacitance between each gate and grain to the intergrain coupling capacitance.

II. Fabrication of Point-Contact Set

Our point-contact SETs are defined in a 40-nm thick, heavily doped n-type (phosphorous, with a doping concentration $\sim 1 \times 10^{19}$ cm^{-3}) nc-Si film. The film was deposited using low-pressure plasma-enhanced chemical vapor deposition on a 100-nm-thick SiO_2 layer grown thermally on a Si substrate. The grains are ∼10–40 nm in size and in the film as-deposited, the GBs are thin (∼1 nm) amorphous silicon tissues. The SETs are defined in the film using high-resolution electron-beam lithography and trench isolation by reactive-ion etching of the nc-Si down to the buried oxide [3]. Fig. 1(a) shows a schematic of a point-contact SET. Fig. 1(b) shows a scanning electron micrograph of one of the completed devices (Device 1). The nc-Si grains are visible clearly in the micrograph. The point-contact

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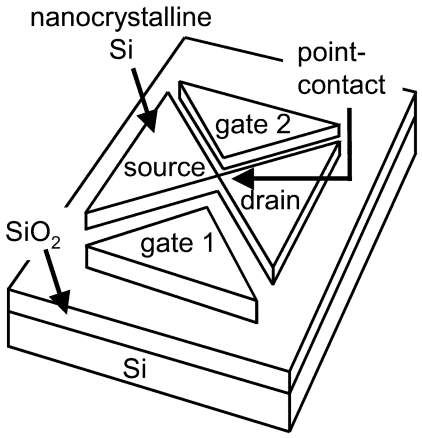

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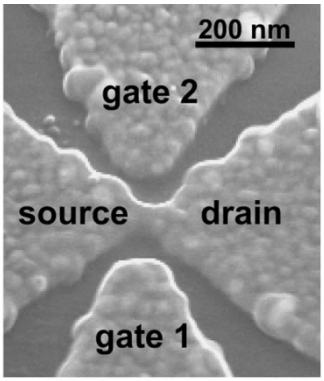


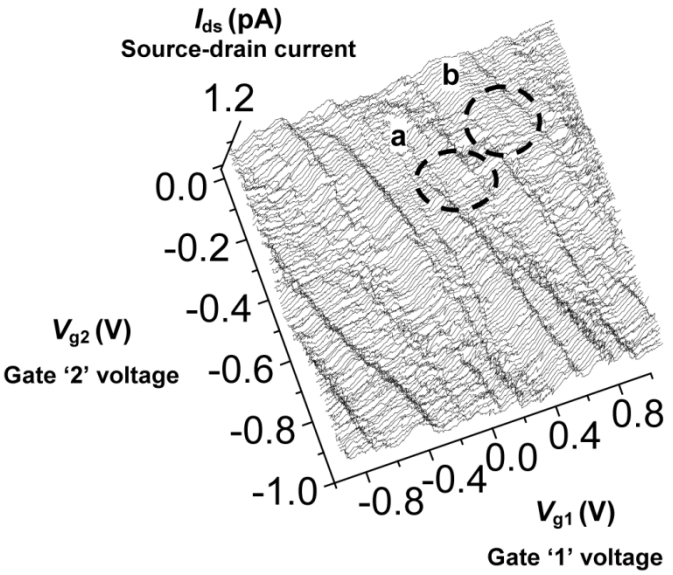
(b)

Fig. 1. (a) Schematic of a dual-gate point contact SET. (b) Scanning electron micrograph of a point-contact SET (Device 1) fabricated in a nanocrystalline silicon thin film.

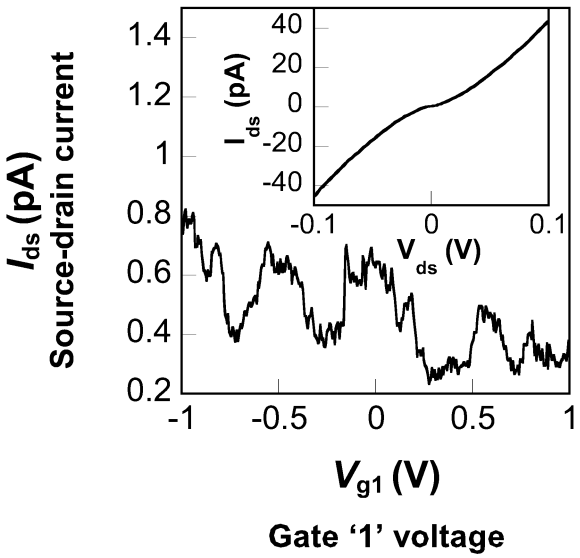
is a $\sim 30 \times 30 \times 40$ nm region between larger source and drain regions, with two in-plane gates on either side. The gates are $\sim$100 nm away from the point-contact centre. Device 1 is oxidised in dry O_2 gas at 750 °C for 1 h and then annealed in Ar gas at 1000 °C for 5 m. The process tends to oxidise selectively the GBs into silicon suboxide, increasing the GB tunnel barrier energy and resistance and improving electron confinement on the grains [5], [8]. Selective oxidation of the GBs depends on the ratio of the rate of oxidation of the amorphous Si GBs to the rate of oxidation of the crystalline Si grains. At temperatures $\sim$ 750 °C or lower, there is greater oxygen diffusion into the lower density amorphous Si GBs, improving this ratio. Longer oxidation times diffuse more oxygen atoms into the GBs.

III. Experimental Characteristics of Point-Contact Sets

Fig. 2(a) shows the drain-source current ($I_{\rm ds}$) at 4.2 K versus the voltage applied to gate 1 (V_{g1}) for Device 1. The drain-source voltage ($V_{\rm ds}$) = 6 mV and voltage on gate 2, V_{g2} = 0V. Single-electron conductance oscillations are observed in $I_{\rm ds}$ with a set of large peaks and finer superimposed peaks. The former may be associated with a dominant charging grain. The fine peaks imply additional energy levels for tunnelling, which may be associated with other grains or with defect states [3]. Qualitatively similar behavior is observed if V_{g1} is held constant



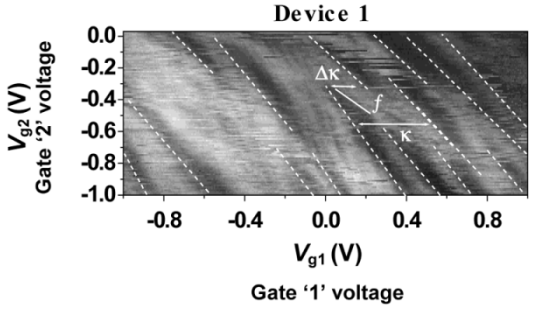
(a)



(b)

Fig. 2. (a) The source-drain current, $I_{\rm ds}$, versus gate 1 voltage, V_{g1}, characteristic. The source drain voltage, $V_{\rm ds}$ = 6 mV, and gate 2 voltage, $V_{g2} = 0$ V. The inset shows the $I_{\rm ds} - V_{\rm ds}$ characteristic at $V_{g1} = V_{g2} = 0$ V. (b) $I_{\rm ds}$ versus V_{g1} and V_{g2} characteristics at $V_{\rm ds}$ = 6 mV and at 4.2 K.

and V_{g2} is swept. The inset shows the corresponding $I_{\rm ds} - V_{\rm ds}$ characteristics at $V_{g1} = V_{g2} = 0$V, where the Coulomb gap is $\sim$30 mV. Fig. 2(b) shows a three-dimensional (3-D) plot of $I_{\rm ds}$ as a function of V_{g1} and V_{g2} for Device 1 at 4.2 K and $V_{\rm ds} = 6$ mVmV. The corresponding grey scale image is shown in Fig. 3(a). The characteristic is obtained by sweeping V_{g1} from -1 V to 1 V in 5 mV steps and incrementing V_{g2} from -1 V to 0.03 V in 10 mV steps. Sweeping both V_{g1} and V_{g2} shifts the oscillation peaks linearly, leading to the dark lines in the plots [marked additionally by white dashed lines in Fig. 3(a)]. There are bistable regions where the oscillations overlap and switch from one line to another, e.g. within the circles labeled "a" and "b" [Fig. 2(b)]. The gradient of the lines is $\sim$2 and the



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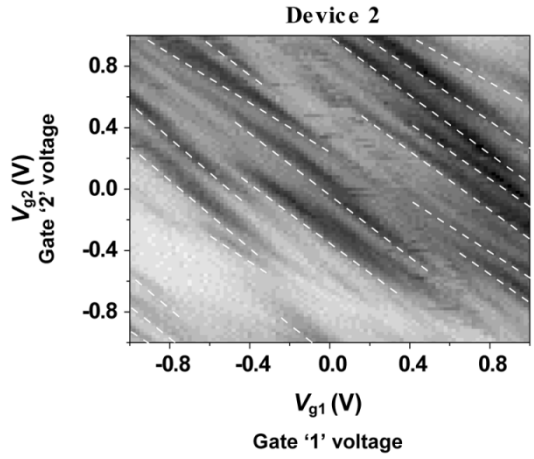


(b)

Fig. 3. (a) Grey scale image of $I_{\rm ds}$ versus V_{g1} and V_{g2}, obtained for Device 1 at $V_{\rm ds} = 6$ mV and at 4.2 K. The maximum current (white region) is 1.2 pA. The dashed lines mark the shift in the Coulomb oscillation lines (b) Equivalent characteristics for Device 2 at $V_{\rm ds} = 2$ mV and at 4.2 K. The maximum current (white region) is 9 pA.

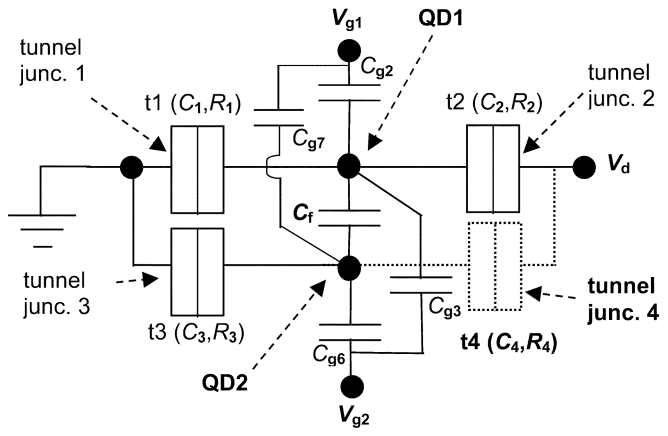
current magnitude varies for different lines. Fig. 3(b) is a similar grey scale image of the $I_{\rm ds}$ versus $V_{g1} - V_{g2}$ characteristics from a second device (Device 2) at 4.2 K and $V_{\rm ds} = 2$ mV. Device 2 is oxidised at lower temperature (650 °C) for shorter time (10 min) and cooled down in Ar gas. We use a lower temperature in an effort to increase the conductivity. Qualitatively similar behavior to Fig. 3 is observed in devices fabricated independently on different samples. We note that at 77 K, only single-period Coulomb oscillations are observed, without strong switching effects. We do not observe room-temperature single-electron charging effects in these devices. This may be compared to our earlier work on 20×20 nm point-contact SETs operating at room-temperature, defined in ∼20 nm thick hydrogenated nc-Si films prepared by VHF PECVD at 300 °C from a $SiF_4 : H_2 : SiH_4$ gas mixture [8]. In these films, the grain size was only 4–8 nm, smaller than the ∼10–40 nm grain size in the devices of our present paper, and the carrier density was an order of magnitude higher ($\sim 1 \times 10^{20}$ cm^{-3}). A combination of smaller device size, smaller grain size and a high tunnel barrier height (∼170 meV) after low-temperature oxidation/high-temperature Ar annealing lead to room-temperature single-electron charging effects. In our present devices, increasing the oxidation time may help to raise the tunnel barrier height and increase the temperature of operation. However, this would reduce the device conductivity even further and an increase in the doping density would be necessary to counter balance this.

The oscillation peak lines in Fig. 3 correspond to resonance between the single-electron charging energy levels $\rm E_{cn}$ in the charging grain along the transport path and the Fermi energy $\rm E_{fs}$ in the source, for the nth line. Sweeping either gate voltage moves the levels $\rm E_{cn}$ past $\rm E_{fs}$ and causes oscillations in $I_{\rm ds}$. The position of $\rm E_{cn}$ relative to $\rm E_{fs}$ depends on the net effect of both V_{g1} and V_{g2} on the grain, e.g. to remain on the same (nth) line, if V_{g2} is reduced, then V_{g1} must be increased in order to maintain $\rm E_{cn} = E_{fs}$.

IV. Theoretical Investigation of a System of Two Parallel Dots

We investigate the *I–V* characteristics of Figs. 2 and 3 using Monte Carlo single-electron circuit simulation. Fig. 4(a) shows our simulation circuit, where two QDs, arranged in parallel, are coupled to each other by a capacitance C_f. QD1 is coupled to the source and drain respectively through similar tunnelling barriers t1, t2 (0.7 aF, 500 kΩ) and QD2 is coupled to the source through the tunnelling barrier t3 (0.3 aF, 1000 kΩ). We call this circuit "A." We also simulate a symmetrical circuit where QD2 is connected additionally to the drain via a tunnelling barrier $\rm t4 = t3$ (dotted circuit). We call this circuit "B." In both circuits, QD1 and QD2 are coupled to the side gates V_{g1}, and V_{g2} by the gate capacitances C_{g2} and C_{g6}, respectively. C_{g3} and C_{g7} are the cross-capacitances between V_{g2} and QD1, and V_{g1} and QD2, respectively. $V_{\rm ds} = 5$ mV and the simulation temperature is 4.2 K.

Fig. 4(b) shows the simulated Coulomb oscillation characteristics as a function of V_{g1} and V_{g2} for $\rm C_f = 1$ aF (circuit "A": main figure, and circuit "B": left inset). In the main figure, the Coulomb oscillation peaks form the dark lines separated by white regions of zero current and stable electron number. The lines shift linearly and switch by ΔV_{f1} with the gate voltages. The peak lines also overlap by 'L' near a switch. The switching and overlap behavior is similar qualitatively to the experimental characteristics of Fig. 3. The peak lines in Fig. 4 define the boundaries of regions of stable electron number on QD1. We also show the boundaries of stable electron number on QD2 (scatter points), which switch by ΔV_{f2}. The electron number on both QDs is stable in the regions bounded by both the peak lines and the scatter points. ΔV_{f1}, ΔV_{f2}, ΔV_1, and ΔV_2 define a charge stability region, analogous to those observed in lithographically defined double QDs [10]–[15]. The numbers in the brackets indicate the electron number (n1, n2) on QD1 and QD2 respectively. Fig. 4, right inset, shows the variation of n1 and n2 at $V_{g2} = -0.59$V, as we vary V_{g1} from −1 V to −0.75 V across a switching region. As V_{g1} varies from −1 V toward less negative values, n1 changes initially from −4 to −3. However, a change in n2 from −4 to −3 can change the electrostatic bias of QD1 and switch n1 back to −4. Further change in V_{g1} such that $V_{g1} > -0.8$ V and lies outside the switching region results in stable values of $\rm n1 = n2 = -3$. Within the switching region, charging one of the QDs by an electron can change the electron number of the other QD and leads to bistability of n1 and n2. Peaks lines occur whenever the single-electron levels $\rm E_{cn1}$ in QD1 and $\rm E_{fs}$ are aligned for a given set of gate voltages and electron number. If the gate voltages are such that n2 also



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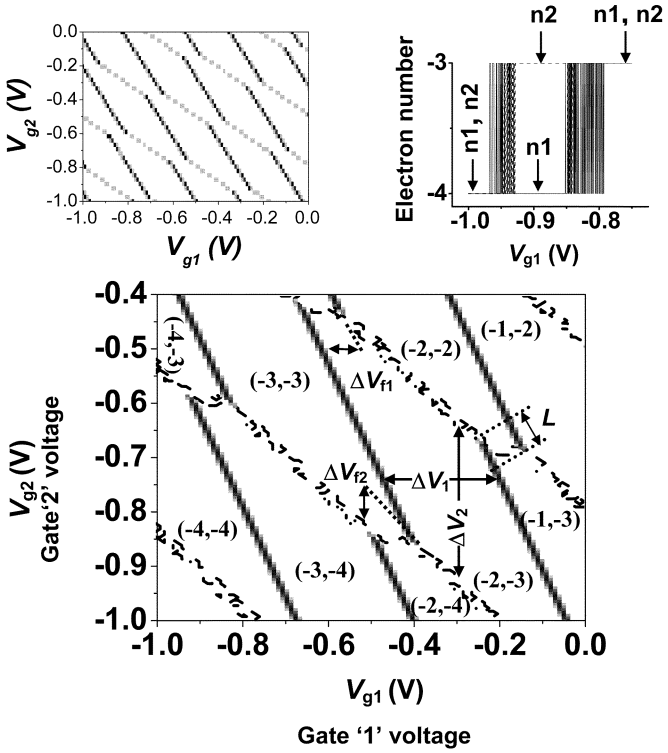
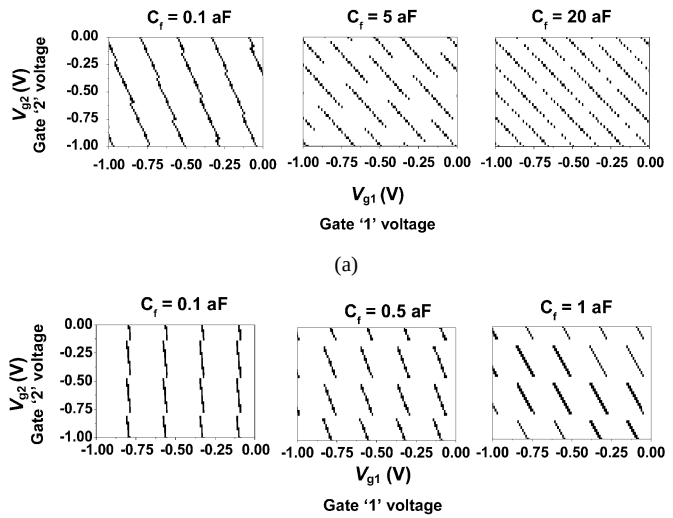


(b)

Fig. 4. (a) Circuits for Monte Carlo simulation. Circuit "A" does not include tunnel junction t4 and circuit "B" is the full circuit, including tunnel junction t4. $C_1 = C_2 = 0.7$ aF, $C_3 = C_4 = 0.3$ aF, $C_{g2} = 0.5$ aF, $C_{g3} = 0.2$ aF, $C_{g6} = 0.5$ aF, $C_{g7} = 0.3$ aF, $R_1 = R_2 = 500\,\mathrm{k}\Omega$, and $R_3 = R_4 = 1\,\mathrm{M}\Omega$. (b) Simulated I_{ds} versus V_{g1} and V_{g2} Coulomb oscillation characteristics for $C_f = 1$ aF. Main figure characteristics are from circuit "A." Solid lines: Coulomb oscillation peaks (maximum current 3 nA). Scatter points: boundaries for regions of stable electron number on QD2. Left inset: I_{ds} versus V_{g1} and V_{g2} for Circuit "B" with $C_f = 1$ aF. Dark lines (maximum current 3 nA) are Coulomb oscillations peaks from QD1. Grey lines (maximum current 0.9 nA) are Coulomb oscillation peaks from QD2. Right inset: variation in electron numbers n1, n2 as a function of V_{g1}, at $V_{g2} = -0.59$V.

changes near the peak line, the change in n2 electrostatically biases QD1 and causes a switch in the peak line position.

In circuit "A," peak oscillations cannot arise from QD2 as there is no conduction from source to drain through QD2. We simulate the effect of conduction via QD2 using circuit "B" by adding tunnel junction t4, forming a more general circuit [16]. Fig. 4(b), left inset, shows the simulated I_{ds} versus V_{g1}, V_{g2} characteristics of circuit "B." This forms a hexagonal pattern in



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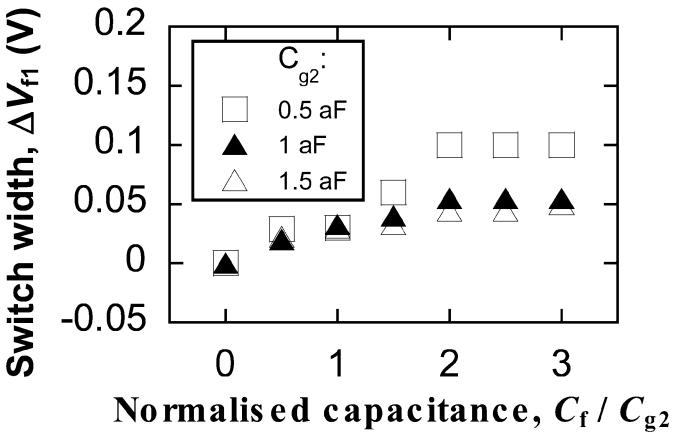

(c)

Fig. 5. Simulated I_{ds} versus V_{g1} and V_{g2} Coulomb oscillation characteristics using circuit "A," with $C_{g2} = 0.7$ aF, $C_{g6} = 0.5$ aF, t2 = t1 (0.7 aF, 500 kΩ), and t3 (0.3 aF, 1000 kΩ). (a) Dependence of characteristics on C_f for nonzero cross capacitances, $C_{g3} = 0.2$ aF and $C_{g7} = 0.3$ aF. (b) Dependence of characteristics on C_f for zero cross capacitances. (c) Switch width ΔV_{f1} as a function of the normalized capacitance C_f/C_{g2} for three values of C_{g2}, 0.5 aF, 1 aF, 1.5 aF.

a manner similar to observations in parallel conducting QDs [12], [13] and oscillation peak lines associated with conduction through both QDs are seen. However, we observe strong peak line overlaps, different from previous work. We will associate these with the cross capacitances in our circuit.

Fig. 5(a) shows the effect of the coupling capacitance C_f, on the I_{ds} versus V_{g1}, V_{g2} characteristics of circuit "A", with cross capacitances, $C_{g3} = 0.2$ aF and $C_{g7} = 0.3$ aF. The switch width ΔV_{f1} and overlap length 'L' increase as C_f increases from 0.1 aF to 20 aF. For small $C_f = 0.1$ aF, there is minimal switching and overlap and the QDs are nearly isolated. As C_f increases to 20 aF, ΔV_{f1} and 'L' increase to an extent that the peak lines join and occur at a period which is approximately half of the period associated with only QD1. In this high coupling regime, the two QDs act as a single large QD and the electron number on both QDs changes simultaneously. However, if we remove the cross capacitances, $C_{g3} = C_{g7} = 0$ aF [Fig. 5(b)], there is no peak line overlap and increasing the coupling only

increases ΔV_{f1} to its maximum value $\sim$ half the period associated with only QD1.

Fig. 5(c) shows the switch width ΔV_{f1} as a function of the normalized capacitance C_f/C_{g2} for circuit "A," for values of C_{g2} of 0.5 aF, 1 aF, and 1.5 aF. ΔV_{f1} increases with coupling as C_f/C_{g2} increases from 0 to 1.5, and saturates at higher values where C_f dominates. This variation is similar for different C_{g2} and depends only on C_f/C_{g2}. ΔV_{f1} saturates when the switching width becomes close to half the oscillation period of QD1 $(0.5\ \mathrm{e}/C_{g2})$.

Analytically, the coupling capacitance can be evaluated from the total electrostatic energy [10] of the simulation circuit

$$C_f = \frac{\frac{\Delta V_{f1}}{\Delta V_1} C_{2\Sigma}}{\left[1 - \left(\frac{C_{g7}\Delta V_{f1}}{e}\right)\right]} = \frac{\frac{\Delta V_{f2}}{\Delta V_2} C_{1\Sigma}}{\left[1 - \left(\frac{C_{g3}\Delta V_{f2}}{e}\right)\right]} \qquad (1)$$

where $C_{1\Sigma}$ and $C_{2\Sigma}$ are the total capacitances of QD1 and QD2, respectively.

Our simulation results were found to be independent of the tunnelling resistance between the two grains and it appears that tunnelling between the grains may not be necessary to explain our observations. We note that if C_f is a tunnelling capacitor, then series coupled QD effects also become possible.

V. Discussion

We now consider further our model (circuit "A") of a QD contributing to the conduction, coupled in parallel to a second "floating" QD. The grain size in our system is $\sim$10 to 40 nm and at minimum only one and at maximum only a few grains can exist within the point-contact. The source-drain current flows across the point-contact along a percolation path through these grains. Due to variation in the grain size and the GB tunnelling barrier resistance, it is possible for a dominant grain to exist along the percolation path, forming QD1. Electrons can also charge grains nearby the percolation path and coupled electrostatically to QD1. Such a grain would act as QD2. At higher temperatures, thermally activated electrons may overcome the GB barrier between the QDs, and electrostatic coupling effects disappear. We note that while series coupled QDs are also possible, we observe higher conductance along the peak lines in comparison to small conductance along the switches at the corners (triple-points) of the hexagonal charge stability regions in the I_{ds} versus $V_{g1} - V_{g2}$ characteristics. This is contrary to the behavior in series-coupled QDs [10], [11] and supports our model of parallel-coupled QDs [12], [13]. We also observe that in previous work on parallel-coupled QDs, long peak oscillation line overlaps were not observed clearly due to low cross capacitance between the QDs and the gates. Our devices have a higher cross-capacitance because the gates can couple to both grains (QDs) via a path through the buried oxide.

In series-coupled QDs in SiGe at 20 mK [15], significant conductance can be observed along the peak lines away from the triple-points, though this is mostly lower than the conductance near the triple points. This is explained by cotunnelling of electrons through the QDs, leading to an observable conductance even though the energy levels in the QDs are not aligned. The peak lines along different sides of the charge stability regions are also of different magnitude, explained by an asymmetry in the cotunnelling processes. We note that even with strong cotunnelling, at 4.2 K the conductance in a series QD system is likely to be higher near the triple points when the QD levels are aligned. In our nc-Si $\sim 30 \times 30 \times 40$ nm point contact SETs, the disordered arrangement of the QDs implies that both series and parallel QD effects may occur. However, our observation of stronger conduction along the peak lines than near the switches supports the possibility of parallel QDs. We also do not observe any peak lines along one set of sides of the charge stability regions [e.g., Fig. 3(a)]. This is explained in our parallel QD model by the lack of conduction via QD2 from the source to the drain.

In contrast to simulation, the various capacitances in the experiment may change with the gate biases, modifying the I_{ds} versus V_{g1}, V_{g2} characteristics from our simulated results. A change in the QD to gate capacitances C_{g2} and C_{g6} would change the slope of the peak lines in our characteristics. This implies that the dashed lines in Fig. 3 will not be parallel. In addition, in Fig. 3, the switch width and overlap length varies at different gate biases and with reference to Fig. 4, this may be attributed to a change in C_f. In Fig. 3(a) we observe clear switches in the range $-0.4\ \mathrm{V} < \mathrm{V}_{g1} < 0.8\ \mathrm{V}$, implying an intermediate coupling regime. Similar behavior is observed in the characteristics of Device 2, Fig. 3(b). We can make an approximate estimate of the average relative coupling capacitance, $C_f/C_{2\Sigma}$, in Device 1 in the intermediate-coupling regime using (1)

$$\frac{C_f}{C_{2\Sigma}} \approx \frac{\Delta\kappa}{\kappa} \approx 0.5.$$

Where $\Delta\kappa$ and κ are the average dimensions along the V_{g1} axis of the stable excess electron region in Fig. 3(a), $C_{2\Sigma}$ is the total capacitance of QD2, and $((C_{g7}\Delta V_{f1})/e) \ll 1$.

We observe that the width of an oscillation line reduces in an overlap region, e.g., along "f" in Fig. 3(a). This may be attributed to the electron number boundary of QD2 crossing the oscillation line with a different gradient. Therefore, "f" lies along a boundary for stable electron number on QD2.

VI. Conclusion

We have fabricated dual-gate point-contact SETs in nanocrystalline silicon thin films. At 4.2 K, we observe switching of single electron current oscillations in the device as a function of the voltage applied to the two gates. These effects are investigated using single-electron Monte Carlo simulation of a model with two charging grains in parallel and intergrain capacitive coupling. We observe a change in the electron number of a grain due to charging of the other grain by a single electron, causing bistable regions in charge stability versus gate voltage. The results are a measure of the local electronic transport properties and intergrain coupling in nanocrystalline silicon thin films.

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