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Single-electron charging phenomena in nano/polycrystalline silicon point contact transistors

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Abstract. This paper gives a review of our recent work investigating the physics of single-electron charging phenomena in nano/polycrystalline silicon nanostructures. We first provide a short overview on the research of silicon-based single-electron devices from the last decade. Various single-electron transistor structures are compared in terms of control of electron islands and tunnel barriers. We then study the single-electron charging phenomena in nano/polycrystalline silicon nanostructures. A novel point-contact transistor is introduced, which features an extremely short and narrow nano/poly-Si nanowire as the transistor's channel. This structure is suitable for studying how a grain smaller than 10 nm in size and a discrete grain boundary work as a charging island and a tunnel barrier, respectively. The relationships between structural and electrical parameters of grains/grain-boundaries and the resulting Coulomb blockade characteristics for the point contact transistors are investigated by applying various passivation processes. Finally, optimisation of grain and grain-boundary structures is discussed for improving the Coulomb blockade characteristics and realizing nano/poly-Si single-electron transistors operating at room temperature.

Introduction

Over the last few decades, the performance of VLSI circuits has been improved steadily by scaling down device dimensions. In dynamic random access memories (DRAMs), for instance, the amount of charge stored per memory cell has been decreased with reduction of the cell area. After the 1 Mbit generation, however, it has become increasingly difficult to keep up such a continuous decrease in the stored charge per bit because the signal becomes less immune to leakage current, internal noise, and soft errors. In microprocessors, power consumption per one MOS transistor has also been reduced due both to miniaturisation and to improved operation conditions. Nevertheless, the total power consumption per microprocessor has gradually been increasing as the number of MOS transistors per chip increases, and the number of electrons used to switch one MOS transistor on and off needs to be reduced further to counter this trend. However, when the number of electrons becomes less than 1000, inherent charge fluctuations cause unacceptable statistical variations in the subthreshold characteristics of the MOS transistors. For both memory and logic applications, how to guarantee future 'scalability' of the devices is a key issue, along with a reduction of the number of electrons. Single- and few-electron devices are expected to overcome these issues by introducing the Coulomb blockade (CB) effect [1],[2] as a new principle for the controlled transfer of a small

number of electrons.

A key building block for single- and few-electron devices are the double tunnel junction (DTJ) and multiple tunnel junction (MTJ) structures shown in Figs. 1(a) and (b), which are composed of a series of islands with tunnel barriers between them. When a single electron enters onto the island, the charging energy E_C of the island increases, and the transfer of even one electron is strongly suppressed (Coulomb blockade) if the charging energy is higher than the thermal energy k_BT. From the device-engineering point of view, the MTJ is more preferable than the simple DTJ since it reduces co-tunnelling [3], which generally leads to unfavourable leakage current. Also the MTJ structure is robust against offset charge effects [4][5], which vary the Coulomb gap and even may break the CB. In general, the tunnel junction (TJ) should meet the following two requirements to show the CB effects at a temperature T:

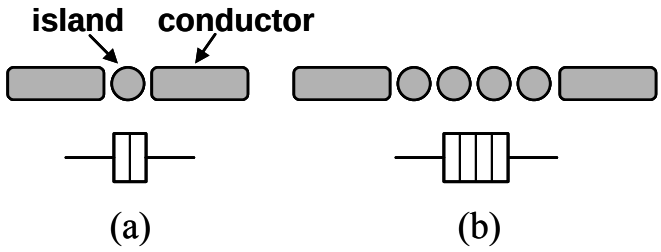

Fig.1: (a) Double tunnel junction and (b) multiple tunnel junction.

$$R_t \gg R_Q = h/e^2 = 25.6\ \mathrm{k\Omega} \quad (1)$$

$$E_C = e^2/2C_\Sigma \gg k_BT \quad (2)$$

to avoid quantum and thermal smearing of the electronic states confined in the islands. In Eqs. (1) and (2) R_Q is the quantum resistance ($\equiv h/e^2$), and R_t and C_Σ are the total tunnel resistance of the TJ and total capacitance of the electron islands, respectively.

A number of fabrication methods for DTJs and MTJs have been reported. These structures may be classified into two groups in terms of the manner of formation of nanoscale electron islands: patterned electron islands and naturally formed ones. A silicon-based patterned island structure has been realized by using a pattern-dependent oxidation (PADOX) technique [6]. This technique utilizes faster oxidation caused by stress at the pattern edge, and a DTJ is formed at the both ends of a Si nanowire (NW). This technique has achieved a single electron island with a lateral size of less than 10 nm. An alternative approach is to use an AFM-based oxidation technique [7]. A NbO_2 DTJ was defined on a Nb NW resulting in a Nb single island with a lateral dimension of a few nm. A step edge cut off (SECO) technique [8] has also been reported to form a metallic MTJ structure.

Naturally formed structures exploit various kinds of local disorder in nanometer-scale structures to form the DTJ or MTJ. In a heavily doped Si NW [9] with a few tens of nanometers in width, randomly distributed dopant atoms cause potential fluctuations, and a linear chain of electron islands are formed when a negative gate bias is applied to a gate electrode placed adjacent to the NW [10]. This is a fairly simple structure and has often been used for making CB memory [11][12] and logic [13] devices. However, the CB oscillation can usually be observed

Table I: Comparison of various methods of single-electron transistor fabrication. Symbols ●, ×, ▲ in the table mean 'Yes', 'No', and 'Partly Yes', respectively.

	Naturally-formed			Patterned		
	Random dopant induced	Rough-ness induced	Defect induced	PADOX based	SPM based	SECO based
Controllability of dot size	×	×	×	●	●	●
Controllability of dot position	×	×	×	●	●	●
Controllability of tunnel barrier thickness	×	×	×	▲	▲	×
Controllability of tunnel barrier height	×	×	×	×	▲	×
Compatibility with Si-ULSI	●	●	●	●	×	×

only at temperatures below 77K as the tunnel barriers are not high enough to confine electrons at high temperatures. A surface roughness induced MTJ has also been reported for a very narrow MOS channel [14]. The CB oscillation was observed at room temperature for this structure. A room temperature CB effect has also been observed very clearly in a carbon nanotube (CNT) in which atomic defects seem to play a role in forming electron islands [15].

These SET structures are summarized in Table 1 from the stand-point of controllability of electron islands and tunnel barriers. The disorder-dependent methods are very useful because CB oscillations can be achieved relatively easily, but it is not possible in these methods to design and control the structural and electrical parameters of MTJs. Among the pattern-controlled methods the PADOX is favorable as the size and position of an electron island can be controlled and it is compatible with Si ULSI technologies. However, key parameters of tunnel barriers such as the barrier height and thickness are not controllable with this method.

Compared with the above technologies, the nano/poly-Si NW structure is very attractive for building CB devices. An ultra thin poly-Si NW has been used to make a single-electron memory device [16] in which both a nanoscale memory node and a sensing channel can be formed naturally. In the poly-Si film, silicon grains and grain boundaries (GBs) between adjacent islands are supposed to act as electron islands and TJs, respectively. Along the GB an electrostatic potential barrier is formed by carriers captured by trap levels in the band gap. The size of the silicon grains can be controlled to a certain extent via a film thickness and/or process conditions for crystallization, and so the poly-Si nanostructures may enable us to go beyond the limit of lithography for realizing 'tailored' electron islands. The macroscopic properties of the poly-Si film have been studied extensively for applications such as thin film transistors (TFTs) and static random access memories (SRAMs), and various techniques have been established to control the grain size and to improve carrier mobility by optimizing passivation conditions. However, the microscopic properties of discrete GBs have not been studied in detail, and there has been no clear guideline to optimize the grains and GBs for high-temperature SET operation. In this work, we examine the structural and electrical properties of the individual grains and GBs as an electron island and a tunnel barrier of a SET by adopting a point-contact transistor (PC-Tr) structure. In addition, we examine the relationship between properties of GB-TJs and the CB characteristics of the PC-Trs by changing the process conditions for achieving room temperature SET operation.

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Our nanometer-scale PC-Tr features a channel with both the length L and width W as small as the grain size L_{grain} of the nano/poly-Si film. The electric characteristics for the PC-Trs must therefore reflect the properties of individual grains and GBs contained in the channel. Figure 2 shows a SEM image of a fabricated PC-Tr. The PC-Trs were fabricated in a 50 nm-thick solid-phase-crystallized (SPC) poly-Si film: a process flow is summarised in Fig.

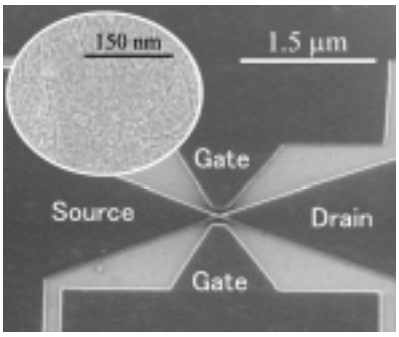

Fig.2: SEM image of an as-prepared point-contact transistor. The inset shows the grain structure of Secco-etched poly-Si film.

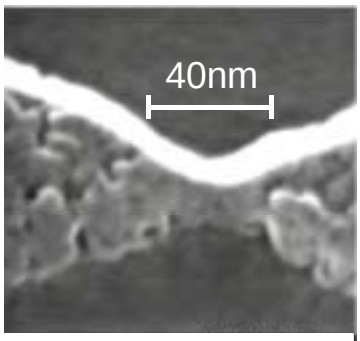

Fig.3: A blow-up of the channel region of the point-contact transistor.

4. The inset to Fig. 2 is a SEM image of a Secco-etched poly-Si film that shows the individual grains and GBs. From the SEM observation over the large area it was found that L_{grain} in this particular film ranges from 20 nm to 150 nm. PC-Trs with a channel width W and length L from 30 nm to 50 nm were patterned by a high-resolution e-beam lithography system and electrically isolated by reactive ion etching (RIE). The channel of these PC-Trs is therefore expected to contain only few grains at most [17]. We fabricated more than sixty PC-Trs using the same process. As shown in Fig. 4, half of the PC-Trs were then oxidized at 1000 ^{o}C for 15 min in dry O_2 ambient to study the effects of oxidation on the grains and GB-TJs [18].

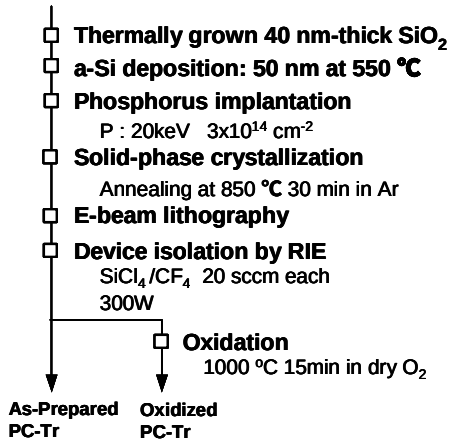

Fig.4: A flow chart of process sequence for point-contact transistors.

Electrical characterization was performed for both as-prepared and oxidized PC-Trs at temperatures down to 4.2K. An effective potential barrier height qV_B of GBs was extracted from a temperature dependence of the I_{ds}-V_{ds} characteristics at between 200K and 300K using the thermionic emission model [19]:

$$J = 2qn\sqrt{\frac{k_B T}{2m^*\pi}}\exp\left(-\frac{qV_B}{k_B T}\right)\sinh\left(\frac{qV_{DS}}{2k_B TN}\right) \qquad (3)$$

where J is the current density, n the electron density, m^* the electron effective mass, qV_B the potential barrier height of GBs, and N the number of GBs in the channel. Structural characterization was also conducted using TEM and SEM. Figures 5(a) and (b) show two typical I_{ds}-V_{ds} characteristics observed for as-prepared PC-Trs. The CB effect was not observed for any of the as-prepared PC-Trs at temperatures above 4.2K. We observed nonlinear I_{ds}-V_{ds} characteristics (Fig. 5(b)) associated with electron thermionic emission current over GBs for approximately one third of the as-prepared PC-Trs. The other devices showed linear I_{ds}-V_{ds} characteristics (Fig. 5(a)). The as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} characteristics would contain a few GBs with a relatively high potential barrier, while those with linear I_{ds}-V_{ds} characteristics would have either no GB or a few GBs with a very low potential barrier [17].

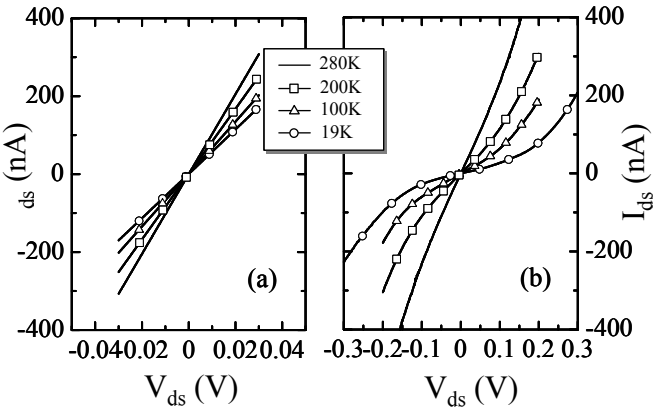

Fig.5: I_{ds}-V_{ds} characteristics of as-prepared point-contact transistors with Width/Length = 40 nm/50 nm: (a) linear and (b) non-linear characteristics

In contrast, most of the oxidized PC-Trs show a clear current oscillation in the I_{ds}-V_{gs} curves and a CB gap in the I_{ds}-V_{ds} characteristics associated with the CB effect V_T: Figs. 6(a) and (b) show typical I_{ds}-V_{gs} characteristics for the oxidized PC-Trs measured at 5K [18]. We found that the CB characteristics for the oxidized PC-Trs can be classified into two groups: the characteristic with a Coulomb gap $V_T < 5$ mV and that with $V_T > 5$ mV. The conductance oscillation periods were quite similar among PC-Trs with the same channel dimensions and $V_T < 5$ mV. On the other hand, the oscillation periods differ largely among oxidized PC-Trs with $V_T > 5$ mV. Peak-to-valley (P/V)

current ratios and tunnel resistances obtained for PC-Trs with V_T > 5 mV were generally much larger than those with V_T < 5 mV.

Figures 7(a) and (b) show TEM images of the as-prepared and the oxidized poly-Si films. Both poly-Si films consist of columnar-shaped grains. Temperature dependences of the resistance are shown in Fig. 8. Regarding the as-prepared PC-Trs, although each GB and grain may act as a tunnel barrier and an electron island, the estimated tunnel capacitance is larger than 80 aF because of the tall columnar grains. Also the tunnel resistance R_t estimated for the as-prepared PC-Trs is just as large as the quantum resistance R_Q of 25.6 kΩ. Therefore, for the as-prepared PC-Trs, both the electron charging energy E_C and the tunnel resistance R_t are not sufficiently large to observe the CB effect even at a cryogenic temperature (see Eqs (1) and (2)). In contrast, in the oxidized PC-Trs, the poly-Si film thickness decreased down to approximately 18 nm after the oxidation process [20]. The reduction of the film thickness leads to a decrease in the tunnel capacitance and consequently increases the charging energy. In addition, the tunnel resistance is increased by more than two orders of magnitude after the oxidation treatment, as shown in Fig. 8. Both the increased charging energy and tunnel resistance result in the appearance of the CB effect as the conditions in Eqs. (1) and (2) are satisfied.

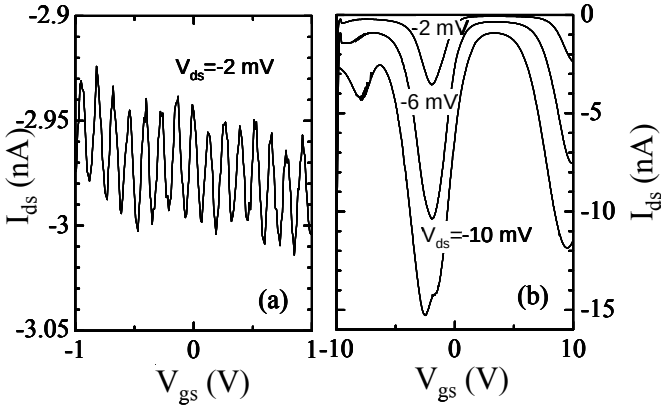

Fig.6: I_{ds}-V_{ds} characteristics for oxidised point-contact transistors with (a) V_T < 5 meV (b) V_T > 5 meV.

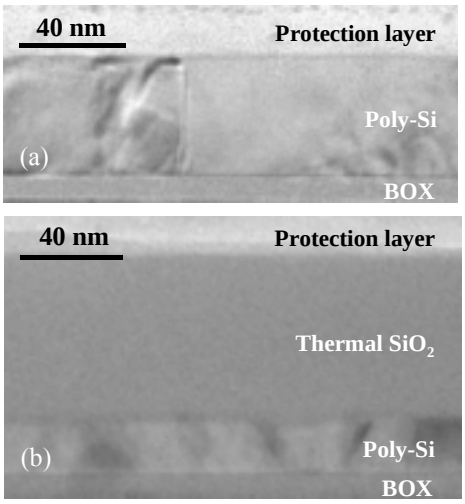

Fig.7: TEM images for (a) as-prepared and (b) oxidized poly-Si films.

Figure 9 presents the distributions of qV_B obtained for (a) the as-prepared and (b) the oxidized PC-Trs. It is found that the mean qV_B increases slightly after the oxidation process. We first note that the oxidized PC-Trs with V_T < 5 mV show a narrow distribution of qV_B (white bars in Fig. 9(b)) which resembles that for the as-prepared linear I_{ds}-V_{ds} PC-Trs (white bars in Fig. 9(a)). On the other hand, qV_B for the oxidized PC-Trs with V_T > 5 mV spreads widely (dark gray bars in Fig. 9(b)), corresponding to the distribution of qV_B for the as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} (dark gray bars in Fig. 9(a)). These distributions represent unoxidized and oxidized GBs in the channel, and qV_B can vary a lot depending on the number and configuration of GBs in the individual devices.

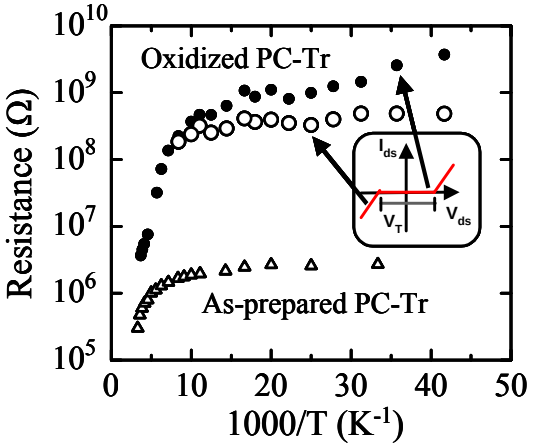

Fig.8: Resistance vs. 1/T for the as-prepared and oxidised point-contact transistors.

As discussed earlier, it is thought for as-prepared PC-Trs with linear I_{ds}-V_{ds} characteristics (Fig. 5(a)), that the device incorporated a grain larger than the size of the NW channel and there was no GB in the channel

to affect the electron transport. All the GBs are contained in the large contact regions and would only show their averaged potential barrier heights. Under these circumstances, the lengthy GBs in the contact regions are not oxidized entirely. Another possibility is that there exist some GBs in the NW channel that do not have many defect states and therefore do not form high potential barriers. The oxidation speed along such low-defect GBs is not very fast and does therefore not have a large effect on their barrier properties. On the other hand, the GBs with larger qV_B obtained for the as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} characteristics are thought to contain large defect densities. These GBs are oxidized effectively [21] and converted to the suboxide tunnel barriers with relatively high barrier heights.

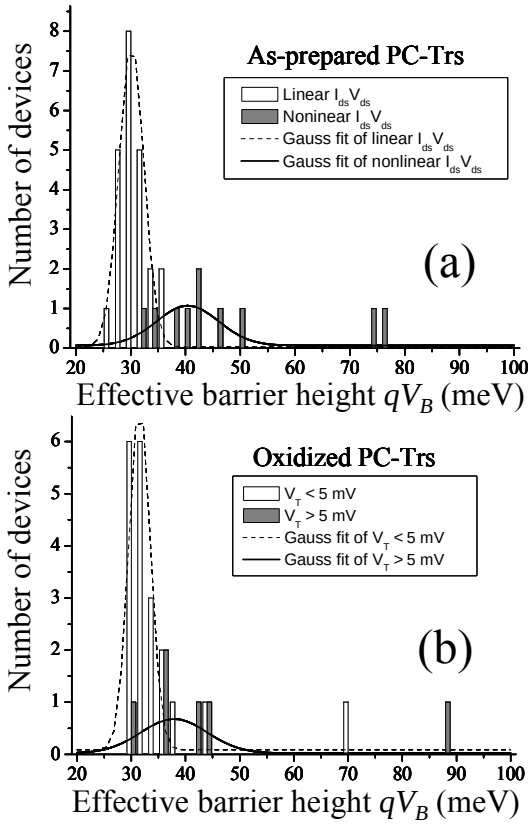

Fig.9: qV_B distributions for (a) as-prepared and (b) oxidized point-contact transistors.

The GB tunnel barrier thickness d was estimated for the oxidized PC-Trs using a tunneling current simulator based on the transfer-matrix method [22]. In the simulation the tunnel barrier was assumed to be a simple rectangular shape with the barrier thickness d and the barrier height obtained as above, and the tunnel resistance of the rectangular barrier was calculated for various values of d. By comparing the observed tunnel resistance with the simulated one, the GB barrier thickness d of approximately 3 nm was obtained for PC-Trs with V_T > 5 mV. This is consistent with high-resolution TEM observation which reveals that GBs were oxidized faster than crystalline grains and that some silicon suboxide layers are as thick as about 3 nm. This result also supports the view that the CB characteristics for PC-Trs with V_T > 5 mV are determined by the selectively oxidized GBs in the channel.

The dimension of the grain that acts as a charging island was evaluated by using a two-dimensional capacitance calculation [23] and the observed Coulomb gap. First, for the oxidized PC-Tr with V_T < 5 mV corresponding to Fig. 6(a), the charging island size was estimated to be about 30 nm; a very similar island size was obtained for all the other PC-Trs with V_T < 5 mV. This figure is similar to the channel dimensions, L and W, and it appears that the entire channel region acts as a charging island in these devices. The DTJ could be formed by the oxidised GBs that are outside the channel but still adjacent to the channel edges. It is, however, more likely that the DTJ is formed by the PADOX-mode oxidation [24]. This scenario is supported by the fact that the CB oscillation periods ΔV_{gs} obtained for the these PC-Trs with V_T < 5 mV are quite uniform among the fabricated devices and also show a dependence on the channel length L: ΔV_{gs} = 0.57 ± 0.1 V for L = 30 nm and ΔV_{gs} = 0.18 ± 0.04 V for L = 40 nm. In contrast, the island size estimated for the oxidized PC-Tr with V_T > 5 mV shown in Fig. 6(b) is as small as about 3 nm. This result is also consistent with the above discussion that few GBs existing in the channel were oxidized, which form very small electron charging islands.

Figure 10 shows the Coulomb gap E_C and the P/V current ratio as a function of the tunnel resistance R_t obtained for the oxidized PC-Trs at 4.2K. It shows that both the P/V ratio and the Coulomb gap increase with increasing tunnel resistance. It can be seen that $R_t > 1$ MΩ is needed to obtain good P/V ratios. The larger Coulomb gap results from an increase in the tunnel resistance and a decrease in the tunnel capacitance due to the formation of thicker GB tunnel barriers with the oxidation process. For improving the CB characteristics of the poly-Si PC-Trs, the structural parameters of GBs, such as qV_B and d, could be optimized further through various oxidation, annealing and passivation treatment as discussed in the next section.

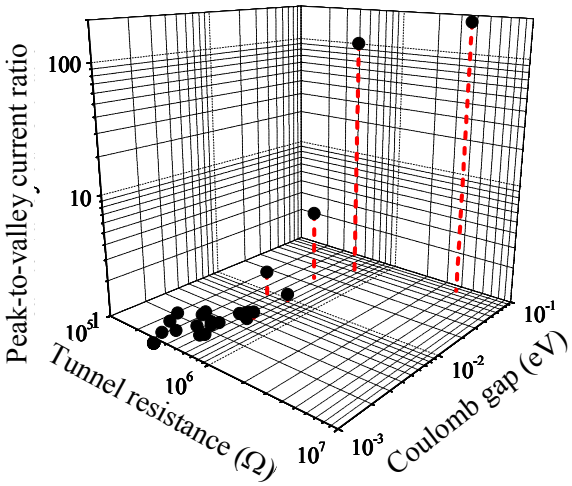

Fig. 10: Coulomb gap and P/V current ratio as a function of tunnel resistance.

Optimisation of grain and grain boundaries towards room-temperature device operation

From the above results, we may have a guideline of optimizing the grain/GB parameters for further improvement of the CB characteristics beyond the general conditions in Eqs. (1) and (2). Regarding the grain size, we found that

$$L_{grain} \lesssim 5 \text{ nm} \qquad (4)$$

is needed for achieving a large P/V current ratio. In addition, we saw that for the tunnel resistance, $R_t > 1$ MΩ should be achieved. If we assume $L_{grain} \simeq 3$ nm and $d \simeq 1$ nm, a simple calculation [25] shows that

$$qV_B \gtrsim 260 \text{ meV } (\simeq 10k_BT). \qquad (5)$$

To reduce L_{grain} overall, a nanocrystalline (nc) Si film prepared by a low-temperature very high frequency (VHF) plasma-enhanced chemical vapor deposition (PECVD) [26][27] was adopted instead of the SPC poly-Si films. A 20nm thick nc-Si:H film was prepared from a SiF_4:H_2:SiH_4 gas mixture at temperatures ≤ 300 °C. The crystalline volume fraction was estimated to be about 70% by using Raman spectroscopy. The films were deposited on a 150 nm thick silicon oxide layer thermally grown on n-type crystalline silicon. The flow rates of the SiF_4, H_2 and SiH_4 were 30, 40, and 0.25 sccm. The VHF frequency was 100 MHz, the VHF power was 40 W, and the reactor

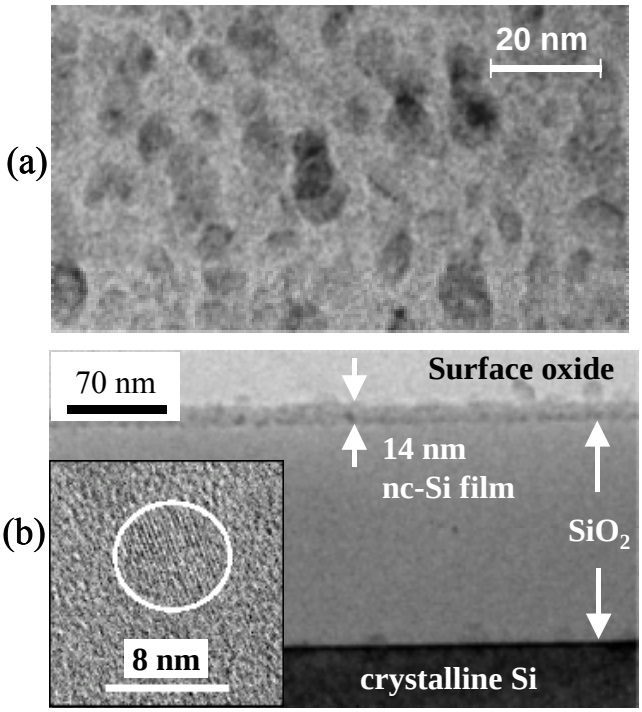

Fig.11: (a) TEM image of the as-deposited nc-Si film and (b) cross-sectional TEM image of the nc-Si film after multi-step oxidation.

pressure was 200 mTorr. As seen in a TEM image in Fig. 11(a), nc-Si grains with L_{grain} from 4 nm to 8 nm are uniformly distributed in an amorphous silicon matrix. PC-Trs were defined in the as-deposited nc-Si film in the same manner as before.

With regard to the condition in Eq. (5) a multiple step oxidation process using low-temperature oxidation (650 °C - 750 °C) followed by high-temperature (1000 °C) annealing was applied after defining the PC-Trs. In the as-deposited nc-Si:H film, the tunnel barriers are formed by the a-Si:H layer between the grains. The multi-step oxidation process was proposed in order to oxidize the a-Si:H selectively and to convert it to SiO_x ($x \ll 2$) without increasing L_{grain} [28][29]. It was found from SIMS depth profile of oxygen concentration [29] that the low temperature oxidation step oxidizes the GBs selectively and the subsequent high-temperature annealing increases qV_B and R_t of the GBs. Also, encapsulation of the grains with the silicon oxide may prevent any grain growth during high-temperature annealing. This was confirmed by a cross-sectional TEM after the multi-step oxidation process: the grains remained the same in lateral size despite the fact that the film thickness was reduced by 6 nm due to surface oxide formation (see Fig. 11(b)).

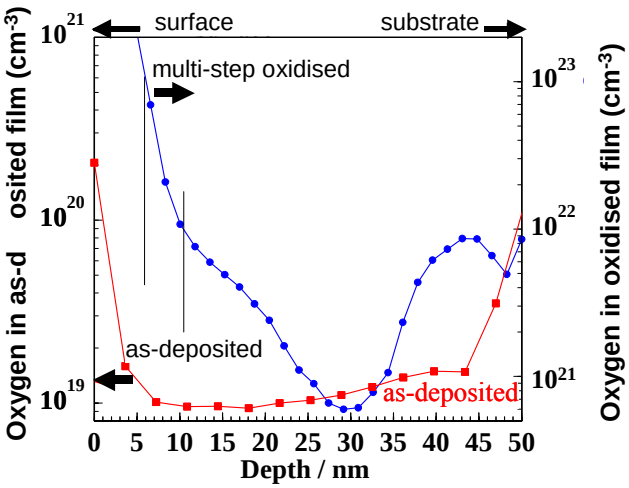

Fig.12: SIMS depth profile of oxygen concentration measured for the as-deposited and multi-step oxidised nc-Si films.

We extracted qV_B for the nc-Si PC-Tr with L = W = 20 nm from a slope of straight lines in the Arrhenius plots of conductivity at a high temperature regime in the same manner as before. While the as-deposited nc-Si PC-Trs showed qV_B of about 40 meV which is as low as those obtained for the SPC PC-Trs, the multi-step oxidized PC-Trs showed qV_B of 173 meV that is now much larger than k_BT although it does not meet the condition of Eq. (5) completely. The mechanism of the tunnel barrier formation in the multi-step oxidized PC-Trs was investigated carefully by using PC-Trs with channel width W from 20 nm to 50nm. It was found that the CB nonlinearity in the I_{ds}-V_{ds} characteristics is much weaker for PC-Trs with a larger W, implying that the oxygen diffusion from the sidewall of the NW channel is supposed to be as important as that from the upper surface. The SIMS depth profiles of oxygen concentration are shown in Fig. 12 for the as-deposited and multi-step oxidized nc-Si:H films [29]. These results show that the minimum oxygen concentration at the bottom of the 20-nm-thick nc-Si:H film is about 2×10^{21} cm^{-3}, so that the value of x in a-SiO_x is estimated to be only about 0.13, assuming that the a-Si:H phases with a volume fraction of 30% were oxidized. If we assume that oxidation also proceeds from both sidewalls and the oxygen concentration is simply given by an addition law, the minimum oxygen concentration at the center of the channel would be 1×10^{22} cm^{-3}, corresponding to $x = 0.67$ [29]. As W is increased, this value decreases gradually, resulting in a lower tunnel barrier at the center of the channel.

Figures 13(a) and (b) show the I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics observed at various temperatures for the multi-step oxidized nc-Si PC-Tr with L = W = 20 nm [30]. A clear CB oscillation is seen in Fig. 13(a) with an unchanged period, and the oscillation persists up to room temperature although the P/V current ratio is gradually decreased as the temperature increases. From a simple capacitance calculation combined with the observed current oscillation period ΔV_{gs} and CB gap E_C, L_{grain} associated with the single-electron charging phenomena for this nc-Si PC-Tr was estimated to be about 8 nm, which is in good agreement with the TEM observation of Fig. 11(b). These results prove that our guideline is correct for raising the operating temperature of the device. In order to

improve the P/V current ratio of the CB oscillation and the uniformity of device characteristics at RT, it is necessary to decrease L_{grain} further as well as increase qV_B by optimizing the multi-step oxidation process [25] to meet the conditions in Eqs. (4) and (5) fully.

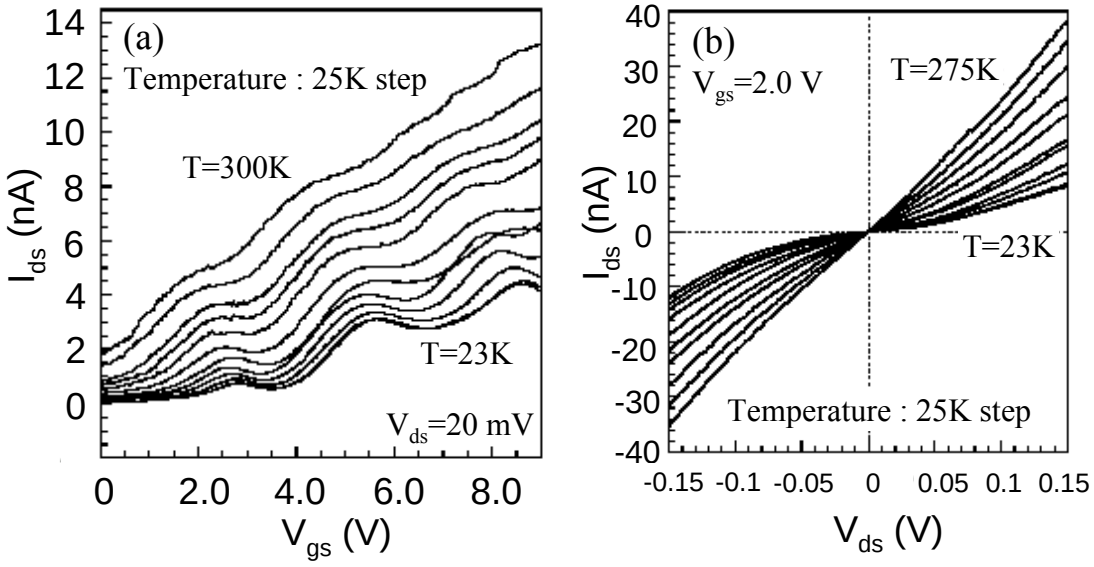

Fig.13: (a) I_{ds}-V_{gs} and (b) I_{ds}-V_{ds} characteristics for the multi-step oxidised nc-Si PC-Tr measured at various temperatures.

Summary

We have presented our recent work on the single-electron charging phenomena in nano/polycrystalline silicon nanostructures using a PC-Tr structure that features a channel as short as the size of Si grains. First, the electrical and structural characterization of discrete GBs has been performed for as-prepared and oxidized PC-Trs fabricated in a 50-nm-thick heavily doped SPC poly-Si film. No CB oscillation has been observed for the as-prepared PC-Trs at T $\geqq$ 4.2K mainly because the tunnel resistance of the GBs was not large enough and the tunnel capacitance was too large. By comparison, PC-Trs oxidized at 1000 ^{o}C for 15 min show CB oscillations at a temperature up to about 40K due both to a reduction of the grain height and an increase in the R_t of the oxidized GBs. The maximum qV_B and d of the oxidized GBs have been found to be 90 meV and approximately 3 nm, respectively. To improve the CB effects, a nc-Si film with 20 nm thickness fabricated by a low-temperature PECVD has been adopted. The nc-Si film contains smaller Si grains with L_{grain} from 4 to 8 nm uniformly distributed in an a-Si matrix. A multi-step oxidation process was applied to the patterned nc-Si PC-Trs to oxidize the GBs more selectively while maintaining L_{grain}. For the multi-step oxidized nc-Si PC-Trs, qV_B was found to be as large as 173 meV, resulting in CB oscillations that persist up to *room temperature*.

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