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# Characterization of Tunnel Barriers in Polycrystalline Silicon Point-Contact Single-Electron Transistors

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Potential barrier properties of grain boundaries in polycrystalline silicon have been studied using nanometer-scale point-contact transistors. The devices, with channel length and width ranging from 30 nm to 50 nm, were fabricated in a 50-nm-thick film. We found that grain boundaries oxidized at 1000°C acted as tunneling barriers, resulting in the appearance of single-electron charging effects. However, potential barrier heights estimated for oxidized grain boundaries are still low, less than 90 meV, and barrier thickness is as large as $\sim$ 4 nm. The grain boundary oxides appear to be silicon sub-oxides which are formed by oxygen diffusion into grain boundaries. [DOI: 10.1143/JJAP.41.2675]

KEYWORDS: polycrystalline silicon film, carrier transport, grain boundary, tunnel barrier, single-electron charging effect

## 1. Introduction

Polycrystalline silicon (poly-Si) is an important material widely used for silicon LSI and thin film transistors for flat-panel displays. It is also used for novel applications such as single-electron transistors (SETs).[1,2] As the grain size of poly-Si films approaches the feature size of the device components in LSI circuits and SETs, it becomes more important to investigate carrier transport properties of crystalline grains and grain boundaries (GBs). Also, we expect that such 'grain boundary engineering' may open novel material and device applications as well as a new scientific field in the nanometer regime.

We have previously studied structural and electrical properties of GBs in an as-prepared, heavily doped poly-Si film using a point-contact transistor (PC-Tr) structure.[3] We have designed both the length and width of the channel to be as small as the grain size in order to investigate electron transport properties via few GBs and have shown that the effective potential barrier height of the GBs ranges from 30 meV to 80 meV. Although these barrier heights appear to be sufficiently high for electron confinement at 4.2 K, no single-electron charging effects (SECE) have been observed.[4] On the other hand, it has been reported that the SECE is observed for 40-nm-wide poly-Si nanowires after oxidation at 1000°C for 15 min. Hence control of grain and GB nanostructures is vital for achieving better performances of the poly-Si devices. However, the properties of individual GBs as a tunnel junction (TJ) have not been studied in detail, and there has been no clear guideline to improve the GB-TJs for high-temperature SET operation.

In this work, we examine the effects of oxidation on structural and electrical properties of GBs using nanometer-scale PC-Trs. Also, we explore the relationship between properties of GB-TJs and the Coulomb blockade (CB) characteristics of the PC-Trs.

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## 2. Fabrication of PC-Trs

We used a 50-nm-thick poly-Si film to fabricate PC-Trs. First, an amorphous silicon (a-Si) layer was deposited on 40-nm-thick $SiO_2$ thermally grown on a crystalline silicon substrate. Then the a-Si layer was subjected to solid-phase crystallization at 850°C for 30 min after phosphorus ion implantation at an energy of 20 keV with a dose of $3 \times 10^{14}/cm^2$.[3] The scanning electron microscope (SEM) image in Fig. 1 shows that the grain size ranges from 20 nm to 150 nm. The transmission electron microscopy (TEM) image reveals columnar grains.[4]

The PC-Trs with two in-plane side-gates were defined in the above poly-Si film using a high-resolution electron beam lithography system with a beam diameter of about 10 nm.[4] The gate-to-channel spacing is approximately 120 nm and the electrical isolation was performed by etching down to the $SiO_2$ layer using the reactive-ion-etching process with a mixture of $SiCl_4$ and $CF_4$. Channel width and length were designed to be from 30 nm to 50 nm. The inset of Fig. 1 shows the PC-Tr with a channel of 30 nm in width and 30 nm in length. The channels in these PC-Trs would contain only three GBs at most.[3] Therefore we may observe current–voltage ($I$–$V$) characteristics that reflect nanoscale GB structures in the

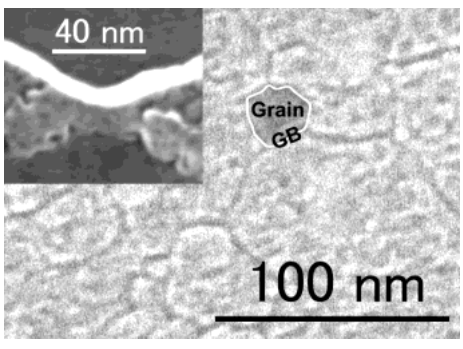


Fig. 1. SEM image of a Secco-etched[5] poly-Si film. Grain boundaries (GB) are clearly delineated. The inset shows a 30-nm-long and 30-nm-wide PC-Tr.

channel.

We fabricated more than 60 PC-Trs using the same process. Half of the PC-Trs were kept as a reference and the rest of the PC-Trs were oxidized at 1000°C for 15 min in dry $O_2$ ambient to improve the electrical properties of the GBs. Source-to-drain current–voltage ($I_{ds}$–$V_{ds}$) characteristics were measured at temperatures between 4.2 K and 300 K. Gate-bias ($V_{gs}$) effects on some devices were also examined.

## 3. Results and Discussion

Regarding as-prepared PC-Trs, approximately one-third of the fabricated PC-Trs exhibited nonlinear $I_{ds}$–$V_{ds}$ characteristics.[3] The measured $I_{ds}$–$V_{ds}$ characteristics fitted well with the hyperbolic sin-formula, which indicates thermionic emission over GB potential barriers[6] with an effective potential barrier height from 30 meV to 80 meV. Although such a potential barrier would work for confining electrons, no CB effects have been observed even at 4.2 K.[4] In contrast, for the oxidized PC-Trs, we observed a zero-current region (Coulomb gap): Figs. 2(a) and 2(b) show $I_{ds}$–$V_{ds}$ and $I_{ds}$–$V_{gs}$ characteristics observed for one of the oxidized PC-Trs, which is referred to as device A hereafter.

SEM and TEM observation showed that the lateral size of small grains in as-prepared PC-Trs is typically about 20 nm, but the grain structure is columnar with a height of 50 nm. The charging energy associated with such big grains is too small to observe SECE even at 4.2 K because of their large tunnel capacitance. We have obtained tunnel resistance from conductance measurements at low temperature (Fig. 3). The tunnel resistance obtained for as-prepared PC-Trs was close to the quantum resistance, but does not meet the required level to observe the SECE.

In the case of the oxidized PC-Trs, the oxidation process reduces film thickness to approximately 18 nm, which decreases the tunnel capacitance and increases the charging energy.[4] For the oxidized PC-Trs, the tunnel resistance was derived from the slope of $I_{ds}$–$V_{ds}$ characteristics at $V_{ds}$ outside the Coulomb gap ($V_T$) (the inset of Fig. 3). Figure 3 shows that the tunnel resistance is increased by more than two orders of magnitude after the oxidation treatment. This increase in the tunnel resistance is sufficiently large to observe the SECE.

Figure 3 also shows that, for both as-prepared and oxidized PC-Trs, the conduction mechanism changes from tunneling (with/without Coulomb blockade effects) at low temperature to thermionic emission at high temperature. Since the conductance at room temperature (RT) is about two orders of magnitude larger than the tunnel conductance, the contribution of the tunnel conduction may be negligible at RT. Thus the conduction in a poly-Si film at RT is attributed to thermal emission of electrons over the GB potential barrier.

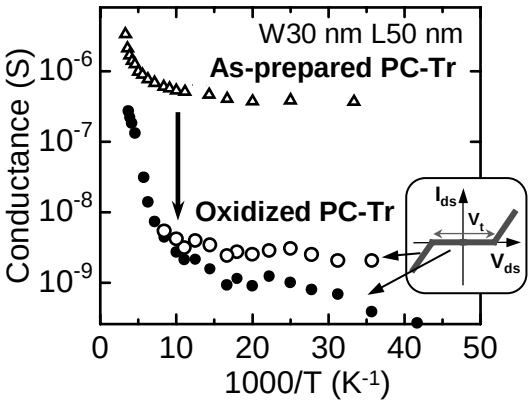


Fig. 3. Arrhenius plot of source-to-drain conductance for 30-nm-wide, 50-nm-long PC-Trs. Triangles and solid circles show the conductance of as-prepared and oxidized PC-Trs, respectively. Open circles show the conductance of the oxidized PC-Tr measured at $V_{ds}$ outside the Coulomb gap ($V_T$).

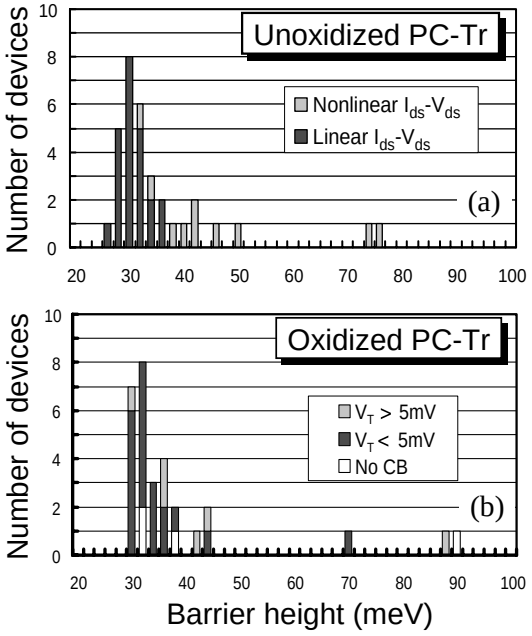


Fig. 4. Distributions of potential barrier height $qV_B$ obtained for (a) as-prepared and (b) oxidized PC-Trs: (a) represent $qV_B$ for as-prepared PC-Trs with linear and nonlinear $I_{ds}$–$V_{ds}$ characteristics, (b) show $qV_B$ for oxidized PC-Trs with no CB, with Coulomb gap ($V_T$) less than 5 mV and with $V_T$ larger than 5 mV.

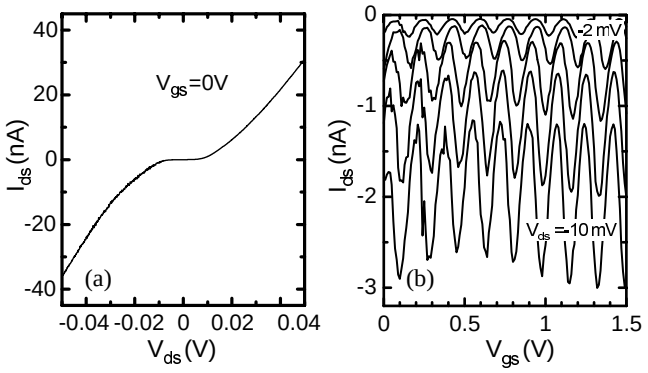


Fig. 2. (a) $I_{ds}$–$V_{ds}$ and (b) $I_{ds}$–$V_{gs}$ characteristics of a PC-Tr of 30 nm width and 30 nm length measured at 9.0 K.

Figure 4 presents the distributions of the GB potential barrier height $qV_B$ obtained from (a) as-prepared and (b) oxidized PC-Trs. Overall, the two distributions appear similar, but the mean barrier height increases by about 5 meV after oxidation. In Fig. 4(a) the contributions from the samples with linear and nonlinear $I_{ds}$–$V_{ds}$ characteristics are shown by dark gray and light gray bars, respectively. As discussed in ref. 3, these were attributed to the devices with no GB and those with

few GBs in the channel, respectively. In Fig. 4(b) the data is shown for the samples with no CB (white bars), those with $V_T < 5\,mV$ (dark gray bars) and those with $V_T > 5\,mV$ (light gray bars). By comparing Figs. 4(a) and 4(b), an interesting trend is observed in which the as-prepared samples with no GB show relatively small Coulomb gaps after oxidation and those with few GBs exhibit larger Coulomb gaps.

As seen in Fig. 4(b), most of the oxidized devices show a CB effect. However, CB properties vary significantly among the oxidized PC-Trs although they were fabricated in the same way. Figure 5 shows the results obtained for another sample of the oxidized PC-Trs that shows a relatively large $V_T$ (this device is referred to as device B hereafter): (a) the $I_{ds}$–$V_{ds}$ and (b) the $I_{ds}$–$V_{gs}$ characteristics. Apparently, device B exhibits a wider Coulomb gap and a larger peak-to-valley (P/V) current ratio than device A. The SECE persists up to approximately 40 K, and the corresponding charging energy, $3k_BT_c$,[7] is estimated to be 10 meV.

Table I shows parameters obtained from the electrical characteristics of devices A and B. Both the P/V current ratio and Coulomb gap of device B are much larger than those of device A because both the effective tunnel barrier height and tunnel resistance are larger for device B. If there are two grains and three tunnel barriers in the channel ,[3] the individual tunnel resistances are estimated to be only $6R_Q$ and $13R_Q$ for devices A and B, respectively, where $R_Q$ is the quantum resistance (25.6 kΩ). Therefore, the smaller P/V current ratio is attributable to this small tunnel resistance. Figure 6 summarizes the distribution of the parameters for all oxidized devices. We observe a trend of improvement in the P/V current ratio and the Coulomb gap with increasing tunnel resistance in Figs. 6(a) and 6(b). Figure 6(a) suggests that a large P/V current ratio requires the tunnel resistance larger than 1 MΩ. The increase in Coulomb gap is attributed to the decrease in tunnel capacitance due to the thicker tunnel barrier formed by the oxidation process.

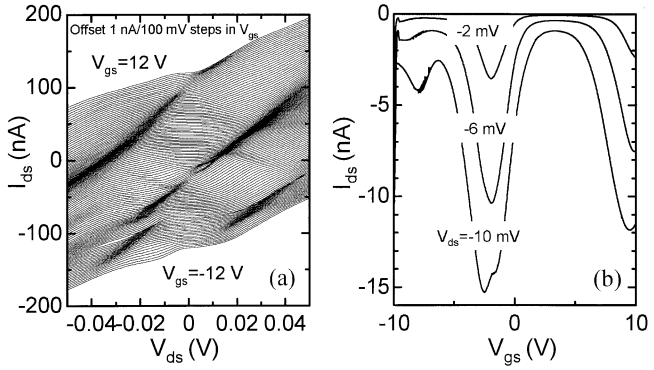


Fig. 5. (a) $I_{ds}$–$V_{ds}$ and (b) $I_{ds}$–$V_{gs}$ characteristics of oxidized PC-Tr of 30 nm width and 30 nm length measured at 9.0 K, clearly exhibiting Coulomb blockade effect. Each $I_{ds}$–$V_{ds}$ curve is offset by 1 nA/100 mV in $V_{gs}$.

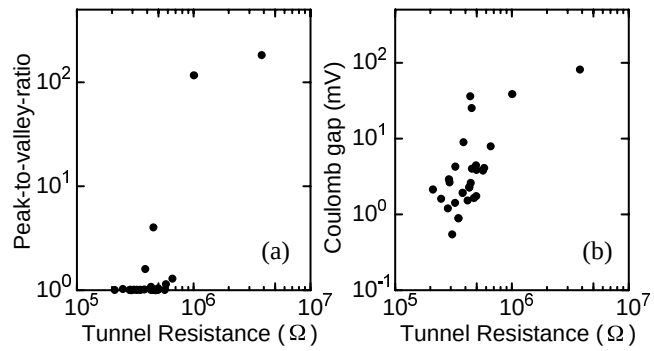


Fig. 6. Tunnel resistance dependence of (a) peak-to-valley current ratio and (b) Coulomb gap measured at 4.2 K.

Table I. Electrical parameters derived from $I_{ds}$–$V_{ds}$ and $I_{ds}$–$V_{gs}$ characteristics of devices A and B measured at 4.2 K. All the data except for tunnel barrier height are extracted at 4.2 K.

| | Device A | Device B |
|---|---|---|
| Coulomb gap (mV) | 29 | 38 |
| P/V current ratio | 4.00 | 116 |
| Tunnel barrier height (meV) | 44.9 | 87.6 |
| Tunnel resistance (Ω) | $4.54 \times 10^5$ | $1.01 \times 10^6$ |
| | $=\sim 17R_Q$ | $=\sim 38R_Q$ |
| Charging energy (meV) | 6 | 10 |
| Barrier thickness (nm) | $\sim 3$ | $\sim 4$ |
| Island size (nm) | 20 | 10 |

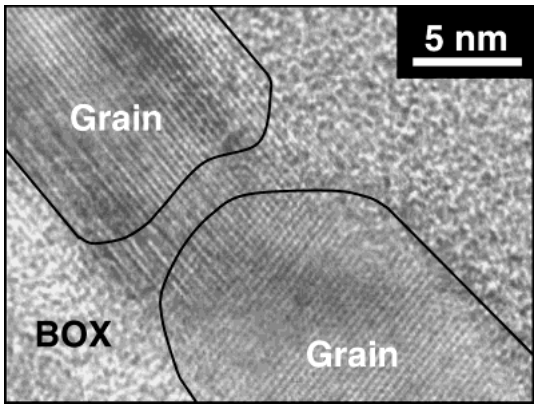


Fig. 7. TEM image of an oxidized poly-Si film. GB is selectively oxidized. Oxidation proceeds from the surface and the buried oxide (BOX) layer. Oxidation along GB from the BOX layer seems to originate from oxygen penetration into the GB without passivating dangling bonds at GB.[10]

GB tunnel barrier thickness and the size of the charging island were also evaluated using a tunneling current calculation based on the transfer-matrix method[8] and two-dimensional capacitance calculation.[9] We assumed a simple rectangular tunnel barrier with the barrier height obtained above. The GB barrier thickness of approximately 3–4 nm was derived from the observed tunnel resistance. A TEM image (Fig. 7) reveals that GBs were oxidized faster than in crystalline grains and that some oxide layers were as thick as 3 nm, which agrees with the above estimation. The charging island size in device A is estimated to be 20 nm from the Coulomb gap, which corresponds to the grain size in the oxidized poly-Si film. This is also the case for the majority of other devices except device B. This supports the idea that the charging islands are crystalline grains and the tunnel barriers are made of oxidized GBs. In contrast, the island size estimated for device B is rather small, 10 nm. It is likely that the oxidation reduces the lateral grain size and produces a very small grain in the channel by chance. Alternatively it is possible that oxidation in some PC-Trs resulted in pattern-dependent oxidation (PADOX)[2] in the chan-

nel, forming small charging islands.

A secondary ion mass spectrometry (SIMS) depth profile shows that oxygen concentration near a substrate-film interface is $3 \times 10^{21}/\mathrm{cm}^3$. If a 2-nm-thick superficial layer with grains 20 nm in diameter is oxidized, the oxygen concentration in the GBs would be only 17%. There are many factors in the oxidation process of nanowires that are not expected to occur in a bulk film, such as oxidation from sidewalls of the nanowires, PADOX mode oxidation, and retardation of the lateral oxidation rate.[4] Thus the oxygen concentration in the GBs can be larger than the above value, depending on the oxidation conditions and its sequence. The electrical characteristics and barrier properties obtained in this work appear consistent if we assume the GB potential barriers in the oxidized PC-Trs are composed of silicon sub-oxide because the bandgap of sub-oxide $SiO_x$ increases linearly with $x$ for small $x$.[11] A similar result has also been reported for nanocrystalline silicon.[12]

We can explain the mechanism of forming such a thick, low GB barrier in the following way: oxygen molecules diffuse faster along GBs than in crystalline grains during oxidation, which results in a higher oxygen concentration along GBs than in grains. Oxidation also proceeds from GBs into crystalline grains, but the total amount of oxygen atoms is limited by oxygen diffusion into GBs. Thus the oxidation depth increases with oxidation temperature and time while the oxygen concentration is kept low.

SETs operating at RT require a potential barrier and charging energy higher than $10k_BT$ ($\sim$ 260 meV at RT).[7] We found that employing low-temperature oxidation followed by high-temperature thermal annealing increased the GB potential barrier height, and that the combination of a nanocrystalline silicon film and two-step oxidation process made it possible for us to observe SECE at RT.[12]

## 4. Conclusions

The electrical and structural properties of GB barriers in a heavily doped poly-Si film have been investigated using a novel PC-Tr structure. We have observed SECE only for oxidized PC-Trs. It is found that selectively oxidized GB barriers act as tunnel barriers and are responsible for SET performance. The potential barrier heights and barrier thickness of oxidized PC-Trs were found to be less than 90 meV and approximately 4 nm, respectively. GB oxides appear to be silicon sub-oxide with a low oxygen concentration, and the oxide formation is limited by oxygen diffusion into GBs.

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